Electrical and structural characteristics of yttrium oxide films deposited by rf-magnetron sputtering on *n*-Si

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Yttrium oxide dielectric films were grown by rf-magnetron sputtering on n-Si(100) substrates and annealed in vacuum at temperatures ranging from 400 to 600 °C. The main aim of this work was the investigation of the interface between the dielectric film and silicon. Both structural (x-ray diffraction and transmission electron microscopy) and electrical characterization were used for this purpose. No structural change was observed on the interfacial native oxide layer after annealing at 600 °C for 1 h. Metal–oxide–semiconductor structures defined by the evaporation of Al electrodes show low leakage currents, moderate dielectric constant (around 14), and high densities of positive charges trapped in the oxide. Hysteresis effects in capacitance–voltage ($C-V$) curves reduce with the annealing temperature. Another interesting observation is the parallel shift of the $C-V$ curves along the voltage axis with frequency. An insulator trap model is proposed to explain this behavior.
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I. INTRODUCTION

The enormous growth and the significant progress of information technology in the modern world are based to a very large extent on the SiO_2/Si interface properties. The industry's demand for greater integrated circuit functionality and performance at lower cost requires an increased circuit density, which is translated into a higher density of transistors on a wafer. Currently, this need is satisfied by introducing advanced materials in the gate of the transistors. By employing nitride/oxynitride gate stacks, functional complementary metal–oxide–semiconductor (CMOS) transistors with physical gate thicknesses <4 nm[1,2] have been demonstrated. Unfortunately, although Si microelectronic devices will be manufactured with SiO_2 and Si–O–N for the foreseeable future, continued scaling of integrated circuit devices will necessitate the introduction of an alternate gate dielectric once the SiO_2 gate dielectric thickness approaches ~1.5 nm. Indeed, the extremely small physical thickness typically required for the gate dielectric results in large leakage current, which is expected to increase power consumption. Excessive gate leakage may be avoided by using high-k[1–3] gate dielectrics (instead of SiO_2), which can provide low equivalent oxide thickness (EOT<1 nm) at relatively large (typically>4 nm) physical thickness.

Among the various extrinsic dielectrics Ta_2O_5, HfO_2, ZrO_2, TiO_2, $SrTiO_3$, $BaSrTiO_3$ (BST), and Y_2O_3 have been investigated extensively. A number of detailed reviews and articles on the subject have been published recently.[1–4] Despite some prerequisites having been met by these dielectrics, their device fabrication and performance potential has not yet been fully realized.

Yttrium oxide deposited on silicon by rf-magnetron sputtering,[5–7] electron-beam evaporation,[8–10] laser ablation and ion beam sputtering,[11,12] as well as by means of epitaxy[13,14] has been proposed as a candidate oxide to replace SiO_2. The low lattice mismatch between the Si lattice parameter $[a_0(\mathrm{Si})\times 2=1.086\ \mathrm{nm}]$ and that of the Y_2O_3 (1.064 nm), the high thermodynamic compatibility,[15] and the relatively high conduction band offset (~2.3 eV)[16] with Si are among the interesting properties of this material. Although amorphous or polycrystalline Y_2O_3 exhibit good electrical characteristics, epitaxial Y_2O_3 is not of adequate structural and electrical quality yet.[17]

A major problem for the use of these oxides is the extremely poor electrical characteristics of the interface between the extrinsic dielectrics and the silicon substrate. Another one is the high density of defects in the extrinsic dielectrics. In many cases the interface defects arise from an interfacial silicon oxide (SiO_x) layer, which grows unintentionally due to oxygen diffusion during the deposition of the oxide and also during postanneal or further postprocessing. This high transport of oxygen is also responsible for the high density of oxygen vacancies in the bulk of some oxides (e.g., ZrO_2 and HfO_2) that leads to an increased amount of positive trapped charge. To overcome these problems, attempts have been made to reduce the randomly occurring microdefect density in the bulk dielectric by improving the oxide stoichiometry using postdeposition oxygen annealing. In another approach, a bilayer dielectric structure consisting of a thin SiO_2 layer at the interface between the extrinsic dielectric and Si was found to be extremely effective in improving the dielectric strength and reducing the leakage currents.[3] The effect of this interfacial layer on the electrical properties of various alternative gate dielectrics has been studied extensively during the last few years.[3,4,18] In a recent publication

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on electron-beam evaporated ultrathin Y_2O_3 films[17], it has been reported that annealing in vacuum can eliminate the interfacial native oxide layer leading to good structural and electrical properties.

In the present work, we report on the electrical and structural studies of thick (340 nm) Y_2O_3 films grown by rf-magnetron sputtering and subjected to postannealing treatment at 400, 500, and 600 °C for 1 h in vacuum. The electrical results are correlated to the structural results from x-ray diffraction (XRD) and transmission electron microscopy (TEM) measurements and show that annealing in vacuum can indeed be used in order to avoid the formation of a thick SiO_x layer. In addition we studied the effect of uniformly distributed bulk oxide traps on the measured high frequency capacitance–voltage ($C-V$) curves.

II. EXPERIMENTAL DETAILS

For this investigation, Y_2O_3 films were deposited by rf magnetron sputtering in argon atmosphere using two independent custom-built sputtering systems. The pregrowth chamber base pressure was nominally 2.0×10^{-7} mbar and during deposition the substrate temperature and argon pressure were maintained at approximately 190 °C and 3 mbar, respectively. The films were deposited onto 100 nm diameter *n*-type Si (100) single crystal substrate of nominal resistivity 1–5 Ω cm. During deposition the wafers were rotated to insure uniform film growth. Prior to deposition, the substrates were prebaked for 20 min at 700 °C. Deposition plasma is created by applying 120 W rf power to the 7.5 cm diameter target positioned 15 cm away from the substrate. The source material is a Y_2O_3 solid target with a nominal purity of 99.9% manufactured by Cerac Inc. Postdeposition annealing at 400, 500, and 600 °C for 60 min was also performed in the same chamber and in vacuum under 2.0×10^{-7} mbar using a substrate heater. In order to maintain minimum growth tolerance between different annealed samples, the 100 mm wafers were cleaved to halves or quarters and each piece annealed individually.

The microstructure and crystalline nature of as-deposited and annealed films were studied by transmission electron microscopy (TEM) performed in a LEO 992 Ω microscope equipped with a Ω-type in column energy filter operated at 200 kV. In order to reduce ion beam induced surface amorphization, the Ar^+ ion energy was kept as low as 3.5 keV. A 10 eV wide and zero loss peak centered slit was used to exclude the contributions from plasmon losses ($\Delta E > 5$ eV).

X-ray diffraction was performed on a system equipped with a position sensitive detector able to collect data over 120° at the same time. The radiation source was an x-ray tube operating at 1.2 kW and equipped with a multilayer monochromator able to select a parallel beam of Cu $K\alpha$ radiation. Diffractograms were collected in both grazing incidence and Bragg–Brentano (θ–2θ) geometry.

Metal–insulator–semiconductor (MIS) diodes were formed by the thermal evaporation of aluminum (Al) electrical contacts on the surface of the thin film. Approximately 200 nm thick Al was evaporated in vacuum under 1 $\times10^{-6}$ mbar through an appropriate mask to delineate a circular contact area of 0.785 mm^2. The top contacts were deposited immediately after annealing. Ohmic back contact was also made by thermal evaporation of 300 nm thick Al.

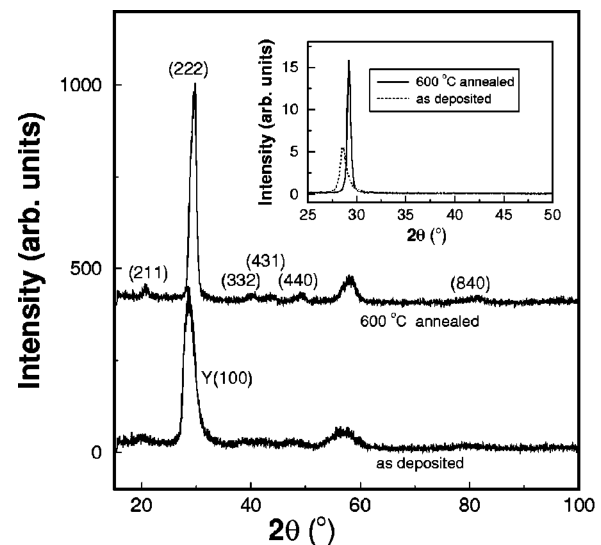

FIG. 1. Grazing incidence XRD patterns of the Y_2O_3 films. The corresponding Bragg–Bentano analysis is shown in the inset.

The $C-V$ measurements were performed in a probe station using a HP 4284A *LCR* meter. $I-V$ curves were also taken in the same probe station using a HP 4140B picoammeter.

III. RESULTS AND DISCUSSION

A. X-ray diffraction (XRD)

X-ray diffraction data of the as-deposited and 600 °C annealed samples are presented in Fig. 1. The diffractograms taken at grazing incidence (angle of incidence $\theta = 0.5°$) show the presence of peaks for both the annealed and as-deposited samples. The increase of the scattered intensity at $2\theta \sim 57°$ is related to the (311) Bragg reflection of the (100) silicon substrate that starts to be excited at such a low angle. In the as-deposited sample, one broad peak is found around $2\theta = 30°$ and several features are present at 20°, 40°, and 47° suggesting a polycrystalline nature for this sample. The peak can be indexed as belonging to the (100) reflection of hexagonal yttrium (REF: PDF33-1458). The position of the peak is shifted as compared to the bulk values suggesting a distortion of the hexagonal lattice. This distortion can be related to either oxygen inclusions in the yttrium lattice or to ordered Y_2O_3 crystallites causing the diffraction pattern to be actually related to the superposition of the reflections of yttrium and of Y_2O_3 in agreement with the presence of the other features. In the 600 °C annealed sample, peaks are found at 20°, 30°, 40°, 45°, and 50°. These peaks are sharper than the ones found in the as-deposited sample suggesting a better crystallization of the sample. The reflections are identified as belonging to the Y_2O_3 cubic phase (REF: PDF 25-1200) and correspond to a polycrystalline sample. The analysis in Bragg–Brentano geometry is presented in the inset of Fig. 1. Only one peak is found in the analyzed 2θ range for both

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as-deposited and annealed samples. This suggests a preferential orientation of the crystallites with the (100) planes of hexagonal yttrium and the (222) planes of cubic Y_2O_3 parallel to the substrate. The samples annealed at the intermediate temperatures of 400 and 500 °C were also analyzed by grazing incidence diffraction. Their diffraction patterns (not shown here) present just one peak related to the Y_2O_3 (222) reflection. The position and the full width at half maximum of this peak are between the two extreme cases presented in Fig. 1 for the as-deposited sample and the sample annealed at the higher temperature.

Fukumoto *et al.*[19] deposited Y_2O_3 films on a Si (100) substrate at a temperature $T_d = 800\,°C$ by electron-beam evaporation from Y_2O_3 grains in oxygen atmosphere. Their XRD results indicated that Y_2O_3 has (222) preferentially oriented planes parallel to the Si(100) plane. However, Harada *et al.*[20] reported that Y_2O_3 films deposited at $T_d = 820\,°C$ also by electron-beam evaporation on clean Si(100) have preferentially oriented the (110) planes, in accordance with the results of Choi *et al.*[21] who deposited their films by the reactive ionized cluster beam deposition technique. Both groups try to explain this difference by means of the existence of a native SiO_2 layer.

In another approach Dimoulas *et al.*[10,17] have reported the growth of thin Y_2O_3 films by electron-beam evaporation directly on Si (100) substrates in a molecular beam epitaxy system under UHV conditions. Depending on the deposition temperature they observe the appearance of both (110) and (111) preferential orientations. At low temperature the (111) orientation prevails, at medium (around 300 °C) temperatures they coexist, while at higher temperatures only peaks corresponding to the (110) planes are present. The authors do not attempt to correlate their findings to any specific deposition conditions, as the parameters involved are many and complicated.

Finally in an earlier work by Horng *et al.*[6] on thick (200–300 nm) Y_2O_3 films grown on p^+ type (100) substrates by rf magnetron sputtering, the same diffused peak appears for the as-deposited films. After annealing though, both (111) and (100) planes appear especially after rapid thermal annealing at 850 °C.

In any case the ideal ''cube on cube'' growth seems to be a difficult task. This is also the situation in this work, which shows evidence of the (111) growth direction with a pronounced mosaic texture in good agreement with several recent works devoted to the Y_2O_3 thin-film deposition on Si substrates. One explanation is the fact that the (111) plane of the Y_2O_3 is the cleavage plane of this structure and therefore the lowest surface energy plane. The interfacial layer of amorphous SiO_2 on top of the Si substrate is often invoked to explain this growth direction, based on a minimization of surface energy.[22]

B. Transmission electron microscopy

As one of the most critical issues for the usefulness of the alternative gate dielectrics is the oxide/Si interface, TEM measurements are often used to investigate the quality of this interface. Out of the four examined films, we show in Figs. 2 and 3 the Si (110) cross-sectional bright field images of the as-deposited and the 600 °C annealed films. The latter was chosen as it showed the best electrical characteristics (as discussed later in Sec. III C). The films were polycrystalline with columnar structure and a thickness around 340 nm. From the diffraction patterns it can be deduced that the grains in the annealed films are bigger. An interfacial amorphous layer is present on both images with an average thickness of 1.4 nm. This corresponds to the native silicon oxide, which was not removed prior to the deposition of the yttrium oxide layer. However, it is interesting to notice that the thickness of this layer does not alter significantly after annealing in vacuum. Recently Dimoulas *et al.*[17] reported on the effects of the annealing process in vacuum of ultrathin Y_2O_3 films grown epitaxially on Si. In some cases it was even possible to eliminate this native oxide film after annealing. Our re-

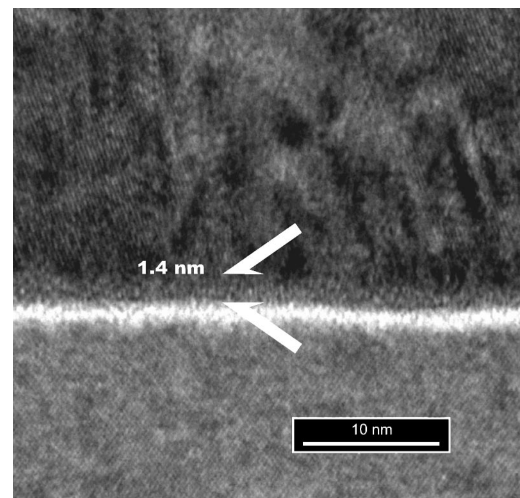

FIG. 2. HRTEM picture of the as-deposited film. The thickness of the native oxide is estimated around 1.4 nm.

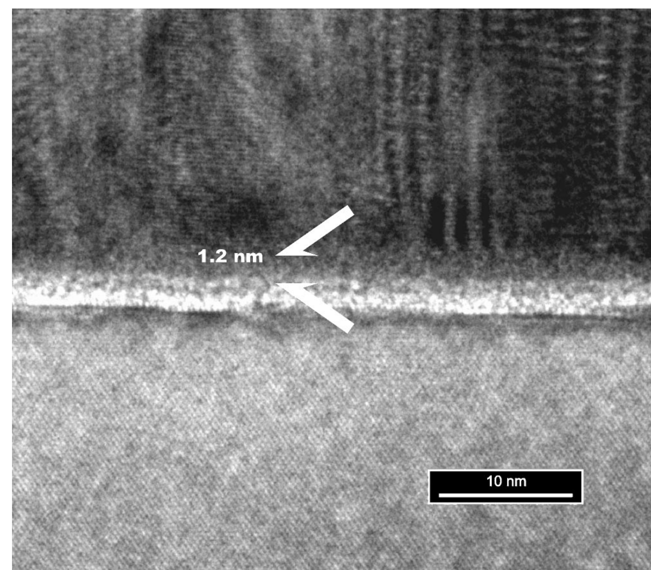

FIG. 3. HRTEM picture of the film annealed at 600 °C. The Y_2O_3/SiO_2 interface seems smoother with respect to the as deposited. The thickness of the native oxide is estimated around 1.2 nm.

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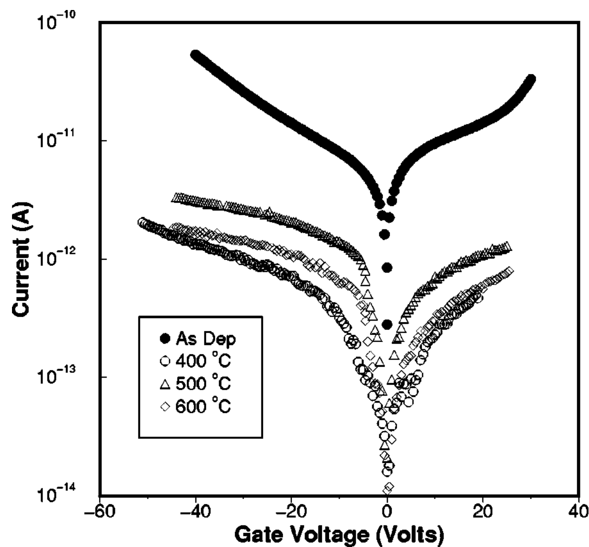

FIG. 4. Log(I)$-V$ characteristics of Al/Y_2O_3/Si diodes. Films annealed at 400 °C showed the smallest leakage currents. A linear plot shows the ohmic behavior of the $I-V$ curves.

sults support their findings in the sense that although the as-deposited films are polycrystalline with a lot of grain boundaries and very thick, after annealing for 60 min in vacuum there is no formation of a thicker silicon oxide interfacial layer. We suppose that it was very difficult to eliminate it due to the thickness of the yttrium oxide layer. But if the diffusion of oxygen through the dielectric is enhanced due to the presence of the grain boundaries one might expect the amorphous silicon oxide interfacial layer to become thicker. A number of works can be found in the literature supporting this oxygen diffusion.[21,23] Such an increase of the interfacial layer of the lower dielectric constant is highly unfavorable for the modern CMOS technology. Therefore our results are interesting as they indicate that the formation of this layer can be avoided after annealing in vacuum. In addition, it allows us to investigate the electrical characteristics of the Si/Y_2O_3 interfaces without the additional problems introduced by a lower-k SiO_x layer grown in an uncontrolled way.

C. Electrical characterization

1. Current density measurements

The effect of crystallization and subsequent annealing of the as-deposited insulating Y_2O_3 films on the current leakage through the MIS structure is depicted in Fig. 4. The $I-V$ curves are almost identical irrespectively of the polarity of the gate voltage. This implies that the conduction mechanism is bulk limited. An interesting result is that the leakage current of the as-deposited film is much higher than that of the annealed films. In addition a dependence of the leakage current with the annealing temperature is evident, with the film annealed at 400 °C giving the best results. This behavior has also been reported on Y_2O_3 films of various thicknesses grown by a variety of techniques.[6,8,9,17,23] Generally it is attributed to the different crystallinity of the films. It was usually accepted that due to the increased roughness of the surface as well as of the interface, greater leakage currents are expected. The reason for this is the appearance of weak spots at the contacts, which act as high-field regions and induce increased current conduction. However, a number of recent publications on alternative high-k dielectrics[3,10,24] show that even for very thin films this is not always true and some polycrystalline films show considerably lower leakage currents than the amorphous or epitaxial films. One possible explanation of the effect is related to the different conduction mechanisms involved. For the annealed films, it was found that the main conduction mechanism is that of electronic hopping conduction as can be deduced from the linear form of the $I-V$ curves (not shown in Fig. 4 for clarity reasons). One possible reason is that the local field is not high enough for the activation of the Poole–Frenkel mechanism (as, for example, in Ref. 8).

It should be mentioned here that the corresponding fields of the voltage values shown in Fig. 4 are up to 1 $MV\,cm^{-1}$. No breakdown has been observed up to field values as high as 2 $MV\,cm^{-1}$ as it was expected for the thick films we studied.

2. Capacitance–voltage measurements

The high frequency (1 MHz) capacitance vs voltage ($C-V$) characteristics are depicted in Fig. 5(a). In all cases the behavior of a typical MIS device was observed for voltage sweeps from inversion to accumulation, while sweep rates of 200 $mV\,s^{-1}$ approximately have been used. The as-deposited films show a pronounced stretchout effect on the $C-V$ curves, which is also observed on the films annealed at 400 °C, while the corresponding conductance–voltage ($G-V$) curves [Fig. 5(b)] are very broad. The dielectric constant is also higher (15) for the as-deposited samples while for the annealed samples this value reduces to 14. The dispersion of the capacitance values at inversion is probably due to defects at the interfaces, as from the TEM measurements we do not find any notable change of the thickness of the oxide. Therefore we could obtain accurate values for the doping concentration of the Si substrates (around 3×10^{15} cm^{-3}) only for the films annealed at 500 and 600 °C.

We would like to point out here that no quasistatic curves could be obtained mainly due to the high density of interface states as we explain in the next paragraphs. Therefore our analysis was based on the high frequency $C-V$ characteristics.

The flatband voltage (V_{FB}) in a $C-V$ curve is generally determined by the metal semiconductor work function difference ϕ_{ms} and the various oxide charges through the relation:

$$V_{FB}=\phi_{ms}-\frac{Q_f}{C_{ox}}-\frac{Q_{it}(\phi_s)}{C_{ox}}, \quad (1)$$

where Q_f is used to account for the fixed charge located very near the Si/SiO_2 interface as well as for the mobile and oxide charges.[25,26] Moreover, charges due to the interface traps (Q_{it}) can also contribute to a shift of the corresponding flatband voltage. It is therefore usual to acquire the $C-V$ curve of a MOS diode at frequencies sufficiently high so that the interface traps do not respond. Thus the last term in Eq. (1) is

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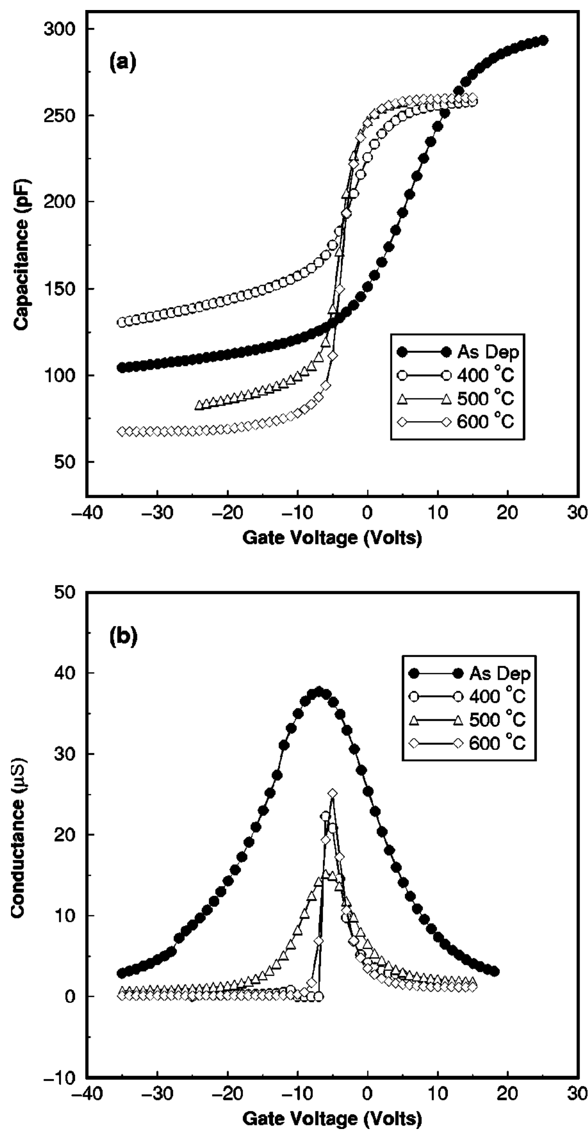

FIG. 5. High frequency (a) $C-V$ and (b) $G-V$ curves of the MOS capacitors. The flatband voltage shifts towards negative values after annealing.

omitted and the amount of fixed charge can be obtained. The 1 MHz frequency used in our experiments was not sufficient in the case of the as-deposited film and the film annealed at 400 °C. The relevant $C-V$ curves are "stretched out" and this can only be attributed to the high concentration of interface traps. Therefore the amount of trapped charge within the oxide layer was calculated only for the films annealed at 500 and 600 °C (Table I), where a negligible contribution from the interface traps is assumed.

TABLE I. Electrical parameters of the $Al/Y_2O_3/Si$ diodes.

Ta (°C)	ε	D_{it} ($\times 10^{12}$ eV^{-1} cm^{-2})	V_{Fb} (V)	Q_f ($\times 10^{11}$ cm^{-2})
	14.5	3.7	+11	
400	13.5	1.8	−1	
500	13.5	0.65	−3	0.2
600	13.5	0.70	−2.5	3

Considerable displacement of the V_{FB} values is observed in the dielectrics before and after annealing. The origin of the positive charges in the Y_2O_3 dielectric is attributed to the inclusion of a large density of defects primarily from oxygen vacancies and broken bonds. It seems though that an annealing temperature of around 500 °C represents a threshold of oxygen intake in the Y_2O_3 film, which reduces considerably the oxygen-related defects and restores compositional homogeneity of the Y_2O_3 dielectric, resulting in reduction of the positive charge density. This result seems to be independent of the growth technique used as it has been also reported in the past for electron-beam deposited films.[8–10]

The corresponding conductance vs voltage ($G-V$) curves at 100 KHz are shown in Fig. 5(b). The interface state densities D_{it} were calculated from the $C-V$ and $G-V$ plots [Figs. 5(a) and 5(b)] using the following relation of Hill's method:[27]

$$D_{it}=\frac{2}{qA}\left(\frac{G_{max}}{\omega}\right)\left[\left(\frac{G_{max}}{\omega C_{ox}}\right)^2+\left(1-\frac{C_{max}}{C_{ox}}\right)^2\right]^{-1}, \tag{2}$$

where D_{it} is the interface state density, A is the area of the capacitor, q the electronic charge, and C_{ox} is the capacitance in accumulation. G_{max} is the peak value of the conductance (obtained from the $G-V$ curves) and C_{max} is the capacitance corresponding to G_{max}. The $C-V$ and $G-V$ plots at 100 KHz have been chosen so that no correction was required on both C and G measured values [Fig. 5(b)]. Thus the minimum D_{it} values calculated were in the order of 10^{12} eV^{-1} cm^{-2}. Recently, the Terman's[25,26] method gained some attention for the study of high-k oxides, as in most cases the observed density of interface states is greater than 10^{11} eV^{-1} cm^{-2}. From the analysis of the high frequency $C-V$ curves according to this method we obtained consistently higher D_{it} values than the Hill's method for all samples, but always in the range of $(2-8)\times 10^{12}$ eV^{-1} cm^{-2}. This high density of interface states is probably the main reason that we were not able to obtain quasistatic $C-V$ plots. Therefore, at this stage, we have an indication of high D_{it} values for the studied structures although for real applications these values have to be evaluated after proper annealing in forming gas.

3. Hysteresis effects

A significant effect of annealing is the change of the direction of the hysteresis loop. Hysteresis is measured by first driving the MIS diode from strong inversion to accumulation and backwards. The rate of the voltage ramp was always around 200 mV s^{-1}. Normalized C/C_{ox} versus gate voltage curves of the diodes containing the as-deposited and the film annealed at 600 °C are illustrated in Fig. 6. It is interesting to point out that only the as-deposited films as well as the films annealed at 400 °C show a notable hysteresis curve ($\Delta V_H > 3$ V in the case of the as-deposited films). The film annealed at 400 °C is the only one showing clockwise direction of the hysteresis curve which could be attributed to electron injection in accumulation. On the other hand, the relevant shifts ΔV_H are <0.20 and <0.10 V for the films annealed at 500 and 600 °C, respectively.

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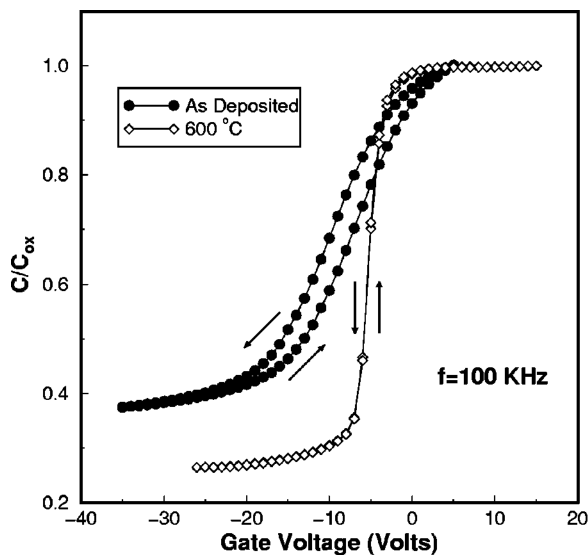

FIG. 6. $C-V$ curves showing hysteresis effects. Hysteresis of the films annealed at 600 °C is small (<100 mV) as compared to the as-deposited films (>3 V).

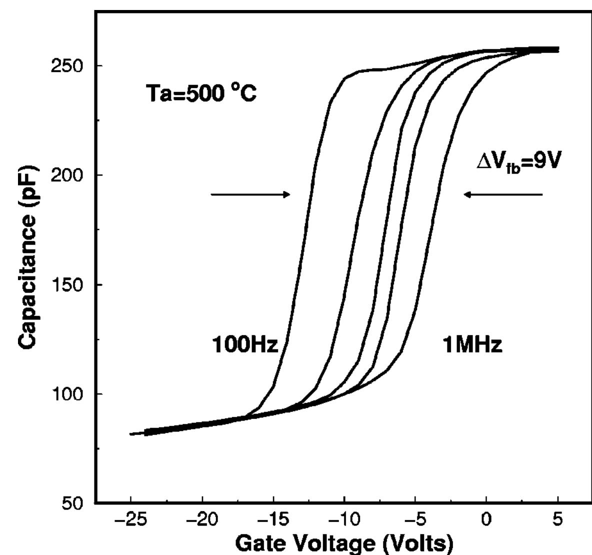

FIG. 7. Shift of the $C-V$ curves with frequency for the films annealed at 500 °C. The flatband voltage shift ΔV_{FB} marked in the figure is greater than 30 V for the as-deposited films and reduces considerably with the annealing temperature.

From the preceding analysis and the D_{it} and Q_f values reported in Table I, the hysteresis results can be directly related to the amount of defects present in the oxide as well as at the Y_2O_3/SiO_2 interface. The origin of this effect is still unclear. Nevertheless, it is anticipated that the observed counterclockwise loops may be due to a polarization in the Y_2O_3/SiO_2 interface, which introduces a sheet of positive charge. The magnitude of this charge is expected to be dependent on the field strength in the film.[28] Indeed, a change of the voltage ramp or the maximum voltage in accumulation results in observable changes in the relevant ΔV_H values. In addition, the higher annealing temperature leads to a better, from the electrical point of view, Y_2O_3/SiO_2 interface so the effect almost disappears. On the other hand, the high density of defects present within the oxide may also give rise to this enhanced hysteresis effect. It has been reported that this hysteresis is related to oxygen deficiency and is also thickness dependent.[29] Therefore in addition to the above-mentioned Y_2O_3/SiO_2 interface charge we assume that it is also the reduction in bulk oxygen-related defects that contributes towards the minimization of hysteresis with the annealing temperature.

An important implication of the inherent formation of electron traps at the high-k oxide/SiO_2 interface is that they capture the injected electrons and as a result a reduced leakage current in MIS diodes with bilayer dielectric has been reported.[18,30] Indeed the large reduction in the leakage current conduction through the c-Y_2O_3/Si structures observed after annealing at 400 °C (Fig. 4) is understood on this basis.

Finally, we would like to stress that a very interesting outcome from the preceding analysis is that the defects present in our films are located close to the silicon interface within the bulk of the oxide and reduce considerably after annealing at 600 °C in vacuum. This will be used as a starting point for the analysis of the $C-V$ shifts with frequency in the next section.

4. Frequency dependence of the C–V curves

An interesting feature of the diodes is that the flatband voltage shifts towards more positive values with increasing frequency of the applied ac signal. In Fig. 7 this effect is illustrated for the films annealed at 500 °C. The transition from inversion to accumulation is sharp and the capacitance in both inversion and accumulation regimes (C_{acc} and C_{inv}) is almost identical for all measured frequencies. The effect is clearly observed in all films but is more profound for the as-deposited films leading to a flatband voltage shift ΔV_{FB} >35 V where we define ΔV_{FB} as

$$\Delta V_{FB} = V_{FB}(100\ \text{Hz}) - V_{FB}(1\ \text{MHz}).$$

These characteristics are difficult to explain on the basis of the interface model developed for the Si/SiO_2 interface.[25,26] If a large density of interface states is present at the interface, then the $C-V$ curves are "stretched out" with frequency. The capacitance in inversion is not affected but a small dispersion in C_{acc} may arise. In some extreme cases ($D_{it} > 10^{13}\ \text{eV}^{-1}\ \text{cm}^{-2}$) a greater dispersion in C_{acc} values has been reported[31] together with a clear shift of V_{FB} with increasing frequency. However, the use of Si (111) substrate is probably the main cause for this elevated density of interface states in this rather old work. During the last two decades the quality of SiO_2 films and the corresponding Si/SiO_2 interface have improved considerably. The presence of any interface states lead to $C-V$ curves which are "stretched out" at lower frequencies and become abrupt at high (0.1–1 MHz) frequencies. Therefore a number of techniques have been developed[25,26] to translate this change in slope of the $C-V$ curves in the depletion region to a graph of D_{it} as a function of the applied gate voltage V_g (or surface potential ϕ_s or energy in Si band gap). An additional parallel shift of the $C-V$ curves occurs when a fixed charge is trapped (Q_f) in the oxide. The amount of fixed charge can be

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related to the measured V_{FB} by Eq. (1). In the present work though, the $C-V$ plot is shifted along the voltage axis with frequency but not stretched.

To the best of our knowledge only a few works have been reported in the past[14,31–34] showing a parallel shift of measured $C-V$'s with frequency. An interesting common feature in these works is that all of them report on interfaces between silicon and poor dielectric materials [e.g., ZnS:Mn (Ref. 32) or amorphous carbon (Ref. 33)]. In the case of Refs. 32 and 34, the authors do not make an attempt to explain the effect. On the other hand Khan *et al.*[33] do explain their results using a model based on carrier tunneling into insulator states.[35] In their case though, V_{FB} shifts towards more negative voltages with increasing frequency and a very low (around 60 Hz) frequency is needed in order to obtain near ideal high frequency $C-V$ curves. Nevertheless, their results can be directly related to ours in the sense that the corresponding V_{FB} shifts towards accumulation with increasing frequency.

We therefore propose a model to elucidate our results based on the same earlier theoretical work by Heiman and Warfield.[35] The concept of this model is that a number of defects (states) introduced uniformly into the bulk of the oxide and close to the interface with silicon have an exponential distribution of time constants with depth in the insulator. At a given frequency all traps with time constants shorter than the reciprocal of the frequency are able to follow the ac signal, thus the flatband condition is reached at a certain gate voltage. If now the frequency of the measurement is increased, slower traps will not be able to respond to the measuring signal and will stay (negatively) charged; hence flatband conditions will be met at more positive gate voltages. Work is currently under progress to fit this model to the experimental conductance vs frequency ($Gp/\omega-\omega$) data.

Therefore according to this model we can conclude from the present work that the amount of oxide traps reduces considerably with the annealing temperatures as implied from the reduction of ΔV_{FB} with the annealing temperature. Indeed, ΔV_{FB} values greater than 30 V were observed on the as-deposited films but reduce to 6 V for the films annealed at 600 °C.

In an attempt to comment on the origin of these defects we believe that they are related to the oxygen vacancies in the oxide and/or states at the interface between native oxide and Y_2O_3. We believe that the existence of discrete level oxygen vacancies with uniform spatial distribution fits better to the proposed model but a definite answer will be given only after studying an oxide/Si interface free from the native oxide interfacial layer.

IV. CONCLUSIONS

The main aim of this work was to study the interface properties of rf-magnetron sputtered yttrium oxide films on n-Si(100) subjected to postdeposition annealing at temperatures in the range 400–600 °C in vacuum. For this purpose rather thick films (around 340 nm) have been deposited in order to obtain extremely low leakage currents.

X-ray diffraction analysis revealed a mixture of yttrium suboxides and cubic Y_2O_3 in the as-grown film. Upon annealing the Y_2O_3 cubic phase crystallites are bigger and strongly oriented with the (111) planes parallel to substrate. A thin native oxide layer is present both in the as-deposited and the annealed films. HRTEM pictures show clearly that this interfacial layer remains almost constant even after annealing at 600 °C.

The dielectric constant of the annealed films was around 13.5 and did not change with the annealing temperature. The electrical characterization of the corresponding MOS devices revealed a mixture of interface and bulk oxygen related defects that give rise to an enhanced shift of the $C-V$ curves along the voltage axis with frequency. An attempt to explain this effect was given based on the response of these defects to the ac signal. The D_{it} values are obviously too high for the devices to be considered as potential alternatives to the current silicon oxide based CMOS technology. A different annealing procedure is needed if this material is to be used as an alternative gate dielectric. On the other hand, if the effects of the bulk oxide defects are thickness dependent they are not expected to cause significant problems on more realistic CMOS applications ($t_{ox}\sim 5$ nm). In any case, the study of these defects in films of variable thickness is needed in order to understand their origin and suggest possible ways of elimination.

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