INCREASING THE PERFORMANCE OF THIN FILM ELECTROLUMINESCENT (TFEL) DEVICES

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Abstract

Novel laterally emitting thin film electroluminescent (LETFEL) devices have been deposited, fabricated and characterised. The new device utilises $BaTiO_3$ thin film insulators, exhibiting a higher dielectric constant over previously reported Y_2O_3 thin film insulators. A study into the effect of the deposition and post deposition annealing conditions on the characteristics exhibited by the $BaTiO_3$ thin films is presented. This study has shown that the optimum growth conditions for $BaTiO_3$ thin films deposited by RF magnetron sputtering are a substrate temperature of 200 °C in an atmosphere of 30 % oxygen in argon at 7 mT at 2.62 Wcm^{-2} with a post-deposition anneal at 700 °C for 1 hour. These deposition conditions produce a film with a dielectric constant of 26, a refractive index of 2.1, a breakdown strength of 2.5 $MV\ cm^{-1}$ and a charge storage capacity of 5.5 μC cm^{-2}. LETFEL devices were characterised and exhibited a maximum luminance of 270,000 fL (driven with a 250 V ground to peak 5 KHz sine wave), this is, to the author's knowledge, the highest reported luminance for any thin film AC TFEL device. The improvement in luminance has been shown to be related to the increase in light confinement achieved by increasing the thickness of the cladding (insulator) in the device structure. An optical model for this improvement is presented.

Finally, the fabrication route for the LETFEL device has been updated to reduce miss-alignment and delivery delays and to allow the shaping of the aperture utilising ion milling.

Acknowledgements

List of Publications

Characterisation of the $BaTiO_3/p$-Si interface and applications. Evangelou, E, Knonofas, N, Craven, MR, Cranton, WM and Thomas, CB; To be published in Applied Surface Science (2000)

The effects of KrF pulsed laser and thermal annealing on the crystallinity and surface morphology of radiofrequency magnetron sputtered ZnS:Mn thin films deposited on Si. Mastio, EA, Craven, MR, Cranton, WM, Thomas, CB, Robino, M, and Fogarassy, E; Journal of Applied Physics 86 (5) 1 (1999).

Characterisation of $BaTiO_3$ thin films deposited by RF magnetron sputtering for use in AC TFEL devices. Craven, MR, Cranton, WM, Toal, S and Reehal, HS; Semiconductor Science and Technology 13 404 (1998).

Does lateral emission in a ZnS:Mn TFEL devices have potential for "laser" printing ? Craven, MR, Cranton, WM, Stevens, R and Thomas, CB; 1998 Extended abstracts from the Fourth International Conference on the Science and Technology of Display Phosphors. September 1998 (Oregon).

Thin Film Phosphor Thermography. Ranson, RM, Thomas, CB and Craven, MR; Measurement and Science Technology 9 1947 (1998).

Laterally emitting thin film electroluminescent devices for head mounted displays. Cranton, WM, Thomas, CB, Stevens, R, Craven, MR, Barros, SO, Mastio, E and Theng, PS; 1997 Proceedings of Electronics Information Displays Conference.

Etching of AC Thin Film Electroluminescent Devices. Stevens, R, McClean, I P, and Craven, M R; IEEE Transactions on Semiconductor Manufacturing, 9, 241 (1996).

Improving the Efficiency of Thin Film Electroluminescent Displays. Cranton, W M, Stevens, R, Thomas, C B, Abdullah, A H, and Craven, M R; Proceedings of IEE Materials for Displays Conference, London. 7/1 (1995).

Laterally Emitting TFEL Display Devices. Thomas, CB, Stevens, R, Cranton, WM, McClean, IP, Craven, MR, and Abdullah, AH; Society for Information Display Digest, Vol 25, 887 (1995).

Statement of Original Work

The programme of research detailed in this thesis represents the authors contribution to the ongoing programme at The Nottingham Trent University. The overall programme is to develop and understand the laterally emitting thin film electroluminescent (LETFEL) device. The goal is to produce a high resolution, high intensity light source for use in head mounted displays (HMD's) and other applications.

The author deposited and characterised all of the thin films required in this programme of research, further responsibility was extended to the deposition of thin films for other aspects of the groups research. The author also commissioned, maintained, and made any required upgrades to the sputter deposition systems. During this programme of research over 350 thin film depositions occurred, Appendix 1 details all of these depositions. Resulting from this programme was the optimisation of $BaTiO_3$ thin films and the fabrication route to produce an increase in the luminance from a LETFEL device.

All of the fabrication required for the test LETFEL devices presented in this thesis was carried out by the author, including the deposition, photolithographic patterning and etching procedures.

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List of Thin Film Depositions

Abbreviations

ACEL	Alternating Current Electroluminescence
Al	Aluminium
Al_2O_3	Aluminium Oxide
AMEL	Active Matrix Electroluminescent Device
AMLCD	Active Matrix Liquid Crystal Display
Ar	Argon
ASIC	Semi-custom Integrated Circuit
$BaTiO_3$	Barium Titanate
BPZT	Barium Lead Zirconate Titanate
BST	Barium Strontium Titanate
CCD	Charge Coupled Device
CF_4	Freon 14
CHF_3	Freon 23
CRT	Cathode Ray Tube
DC	Direct Current
DRAM	Dynamic Random Access Memory
E-Beam	Electron Beam
EL	Electroluminescence
FED	Field Emission Device
FPD	Flat Panel Display
HMD	Head/Helmet Mounted Display
HUD	Head Up Display

ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LEP	Light Emitting Polymer
LETFEL	Laterally Emitting Thin Film Electroluminescent Device
Mn	Manganese
MOCVD	Metal Organic Chemical Vapour Deposition
N_2	Nitrogen
N_2O	Nitrous Oxide
NH_3	Ammonia
NMRC	National Micro-electronics Research Centre
NTU	The Nottingham Trent University
O_2	Oxygen
OEIC	Optoelectronic Integrated Circuit
PCB	Printed Circuit Board
PDP	Plasma Display Panel
PECVD	Plasma Enhanced Chemical Vapour Deposition
PLT	Lead Lanthanum Titanate
PLZT	Lead Lanthanum Zirconate Titanate
PMT	Photon Multiplier Tube
PZT	Lead Zirconate Titanate
RF	Radio Frequency
R.I.	Refractive Index

RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
Si	Silicon
$SiCl_4$	Silicon Tetrachloride
SID	Society of Information Displays
SiH_4	Silane
SiO_2	Silicon Dioxide
SiO_xN_y	Silicon Oxinitride
Si_3N_4	Silicon Nitride
Ta_2O_5	Tantalum Oxide
Ti/W	Titanium Tungsten
TFEL	Thin Film Electroluminescence
Y_2O_3	Yttrium Oxide
ZnMgS:Mn	Zinc Magnesium Sulphide doped with Manganese
ZnS	Zinc Sulphide
ZnS:Mn	Zinc Sulphide doped with Manganese
$ZnS:TbF_3$	Zinc Sulphide doped with Terbium Fluoride

Symbols and Variables

Å	Angstrom
A	Area
α	Attenuation Coefficient
C	Capacitance
C_{INS}	Insulator Capacitance
cm	Centimeter
C_{PHOS}	Phosphor Capacitance
CSC	Charge Storage Capacity
C_T	Total Capacitance
CV	Capacitance-Voltage Characteristic
d	Thickness
d_I	Thickness of the Insulator
d_Z	Thickness of the Phosphor
ε_{BATIO3}	Relative Dielectric Constant of $BaTiO_3$
ε_I	Relative Dielectric Constant of the Insulator
ε_Z	Relative Dielectric Constant of the Phosphor
εr	Relative Dielectric Constant
E_{th}	Threshold Field
ε_{Y2O3}	Relative Dielectric Constant of Y_2O_3
hr	Hour
KHz	Kilo-Hertz
λ	Wavelength

L	Luminance
m	Mode Number
MHz	Mega-Hertz
mm	Millimeter
mT	Milli-Torr
MV	Mega-Volt
π	PI
n	Refractive Index
n_1	Refractive Index of layer 1
n_2	Refractive Index of layer 2
nm	Nanometer
P	Pressure
T_a	Annealing Temperature
θ_c	Critical Angle
θ_i	Angle of Incidence
θ_r	Angle of Reflection
TE	Transverse Electric
T_s	Substrate Temperature
μC	Micro-Coulomb
V	Voltage
V_{th}	Threshold Voltage
x	Distance

Chapter 1 Introduction

1.1 Introduction

With an ever increasing reliance on technology, the need for electronic information display systems is becoming more and more varied. Electronic display devices can be defined as "electronic devices that form a so-called man-machine interface, transmitting data from a machine so that a human user can visually recognise it" [1]. Displays of all ranges in size from large airport information systems down to head mounted displays (HMD's) for the leisure industry are now required. Electronic image sources for other applications are also required, these include high resolution sources for electrophotographic (laser type) printers and fax machines.

Since 1989 The Nottingham Trent University Display Research group has been actively developing high luminance Thin Film Electroluminescent (TFEL) devices. The original devices were aimed towards electrophotographic printing applications, but the technology has now expanded to encompass Head Mounted Display (HMD) applications.

Past research by the group has included the characterisation and the deposition of suitable insulator and phosphor materials and the determination of a full fabrication route, for high resolution, high intensity thin film devices. The research detailed in this programme of research has been concerned with

enhancing the existing technology and processing techniques towards the ultimate goal of producing a display suitable for use as a head mounted display (HMD). This has taken the form of determining an alternative insulator for the device and to optimise the existing fabrication route.

1.2 Flat Panel Displays

Traditionally the Cathode Ray Tube (CRT) has been used for graphic information displays. The CRT has many disadvantages, these include the size, weight and susceptibility to magnetic fields as well as the need for high voltages[2]. This makes them undesirable for head mounted displays due to safety and their bulk. However, at the current time, the high resolution and high brightness available with miniature CRT's make them the preferred choice for high specification systems[3]. As an alternative, research has been undertaken into many different types of flat panel displays (FPD's). Broadly speaking FPD's can be categorised into two distinct groups. These groups are Active (emissive) or Passive (non-emissive). For example, electroluminescent displays are emissive, whereas liquid crystal displays are non-emissive devices. The aim of this section is not to give a full detailed evaluation of the different types of display under development, rather a short summary into the advantages and disadvantages of some types of FPD. Table 1.1 shows a summary of the characteristics of each type of display with their relative merits and drawbacks.

Technology	Type	Merits	Drawbacks	Reference
Active Matrix Electroluminescence (AMEL)	Active	$50 - 100$ cdm^{-2}. Good temperature range. Full video. 64 Gray levels. Contrast >100:1 Low Power. EMC friendly.	Low brightness, only suitable for closed ocular systems. No bright full colour yet.	4,5
Active Matrix Liquid Crystal Display (AMLCD)	Passive	Bright, depends on light source. Full colour. Up to 4096-bit Gray scale. Contrast 100:1	Poor transmission. Poor temperature range or high power if integral heaters used.	6
Plasma Display Panel (PDP)	Active	$75 - 300$ cdm^{-2}. Large panels available. Good for direct view.	High power. Unsuitable for HMD's due to low efficiency and large cost of manufacture.	4,5,6
Field Emission Displays (FED)	Active	100 cdm^{-2}	High voltage. Currently low resolution, uniformity and consistency of emission. No production displays on the market.	4,5,6
Light Emitting Polymers (LEP)	Active	Bright	Still in R & D phase.	4
Light Emitting Diodes (LED)	Active	Can be very bright. Can be used as a source for other technology. Eg Backlight for LCD's.	Resolution is not suitable for video rates. High power.	5
Virtual Retinal Displays (VRD)	Active	80 cdm^{-2}. Contrast 51:1. 6-bit Gray scale	Health worries if a laser is used as the source. Still needs miniaturisation for use as HMD.	7
Organic Electroluminescence	Active	1000 cdm^{-2}. Green.	Still in R & D phase.	8

Table 1.1 Comparison of emerging technologies for use in head mounted display application.

1.3 Electroluminescence

Electroluminescence encompasses any process in which electrical energy is converted into light energy.

More specifically the term EL can be used to define the process of High Field Electroluminescence. It is this phenomena of High Field EL which is utilised in the TFEL device.

This phenomena was discovered accidentally, initially by Destriau in 1936[9]. At the time Destriau was investigating the scintillation properties of a ZnS based phosphor for the detection of alpha particles. Early research into ACEL was geared towards large area displays, but by the end of the 1960's the inherent unreliability and short lifetimes observed by the ACEL powder displays led to the halt of the research[10]. It was not until Inoguchi et Al. from Sharp Co. presented research at the 1974 Society for Information Display (SID) [11] conference that the interest in thin film EL was renewed. Their work was based on the structure in figure 1.1, first presented by Russ and Kennedy [12]. The structure sandwiches the thin film phosphor between two insulating thin films. This allows an AC electric field to be coupled capacitively to the phosphor and hence produce EL. The insulators improve stability over earlier EL devices by providing the necessary current limitation to avoid catastrophic breakdown.
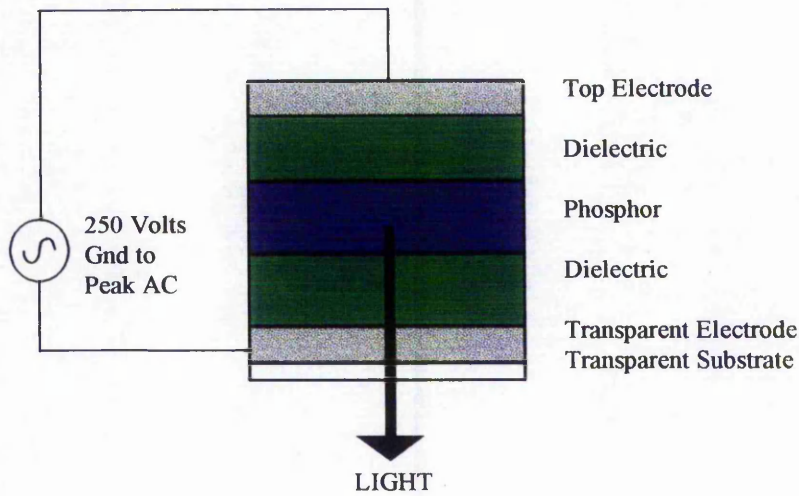
LIGHT

Figure 1.1 Typical structure of an AC TFEL device showing light viewed through a transparent substrate, after Inoguchi[11].

1.4 Physics of High Field Electroluminescence - EL

The main characteristic of operation of an ACEL device is the L-V response. If the luminance of the device, L, is plotted as a function of the applied voltage, the resultant L-V response is of the form shown in figure 1.2. The three main points of interest of this response are:

(A) Vth, The threshold voltage.

(B) The sharp rise in luminance beyond Vth.

(C) The saturation region, typically at Vth + 50 V.
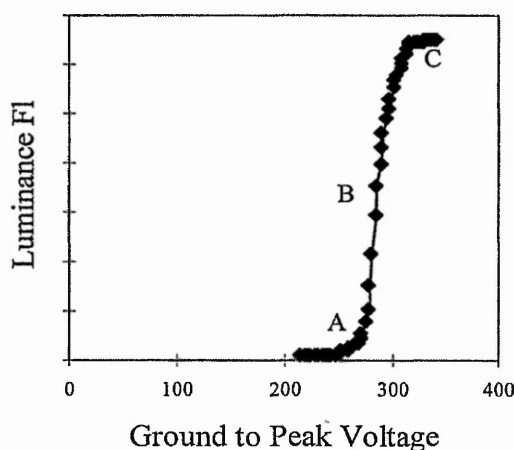
Figure 1.2 Typical Luminance - Voltage characteristic of an AC TFEL device driven by a 5 KHz sine wave

The threshold voltage, Vth, of the device is dependent on the thickness of the films, due to the capacitive structure of the device. It corresponds to the threshold field Eth for operation. Control of Vth is thus possible by varying the device geometry. In general a value of Vth of 200 to 230 volts is desirable. The voltage required to "turn on" the device, i.e. raise the luminance from Vth to saturation, is known as the switching voltage. A low value of switching voltage is desirable, since it increases the viability of direct integration of the device with integrated circuit technology, to produce an Optoelectronic Integrated Circuit, OEIC [13].

Figure 1.3 shows the process of light generation. At the boundary of the phosphor and the insulators, interface states provide the source of electrons. On the application of a high field (i.e. a voltage higher than Vth) these electrons may tunnel from the interface states into the conduction band of the phosphor (A). They are then accelerated by the same field and become "Hot Electrons" (B). During the acceleration some of these electrons will have gained 2.4 eV of

energy. This level of energy is sufficient to excite the Mn ions in the phosphor by impact excitation (C) [14]. These electrons then continue across to the other interface. Luminance is observed when the Mn ions decay radiatively back to their ground state (D). The luminance produced has a peak wavelength of 585 nm, which is close to the maximum photopic response of the eye, and hence is ideal for display applications. This process of electron injection, acceleration and luminance occurs under both polarities of the drive voltage due to the symmetrical nature of the device structure.
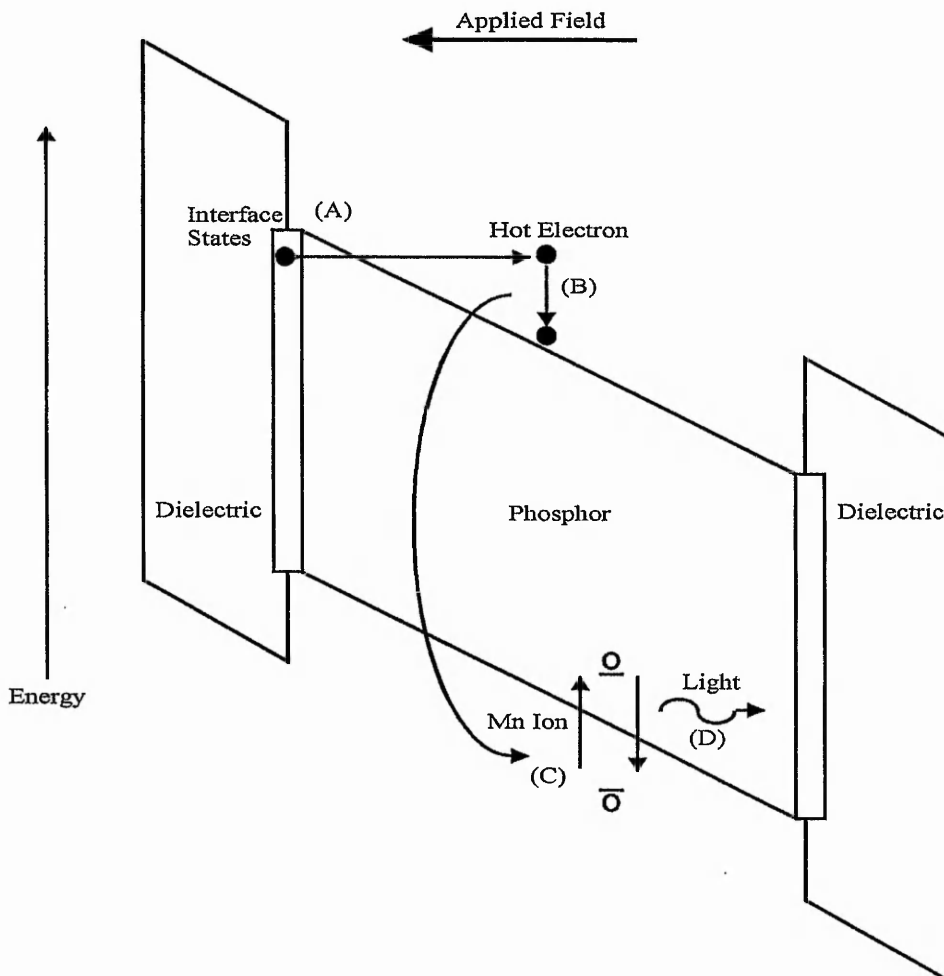
Figure 1.3 The process of light emission from an AC TFEL device

1.5   Lateral Emission And The Waveguiding Effect

Light emission from the typical TFEL device structure of figure 1.1 is viewed through the glass substrate [11].   As an alternative, a novel structure of TFEL device has been developed by the research group at Nottingham Trent University. It utilises lateral emission from the device, reflected vertically by micro-mirrors (Figure 1.4), hence it is known as a Laterally Emitting TFEL (LETFEL) device. The LETFEL device structure has been shown to exhibit a luminance of up to two orders of magnitude brighter over the more typical TFEL device structure [15]. This effect can be attributed to a combination of two effects.

1) The increase in volume of active material.

2) The inherent waveguiding structure of the LETFEL device.
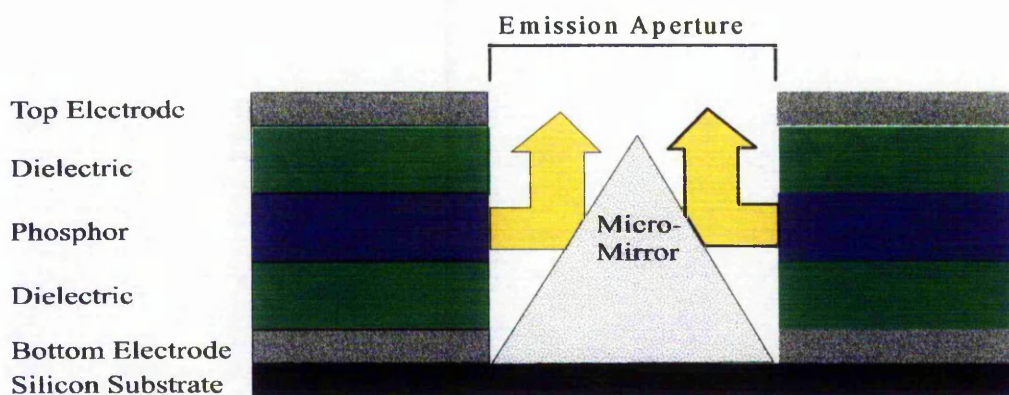
Figure 1.4 Laterally emitting TFEL device structure utilising micro-mirrors to reflect the lateral light enhancing the luminance emission

1.5.1 Volume of Active Material

It is easily understood that the maximum luminous output from an AC TFEL device is reliant on the number of emitting centres. Hence the more emitting centres, the higher the emitted luminance, provided all of the emitted light is out coupled from the device. In the standard TFEL device the volume of material, and hence the number of emitting centres, is dependant on the thickness of phosphor material. In the standard TFEL device this thickness is usually limited to around 800 nm. For a LETFEL device the volume of material is limited by the length of the device not the phosphor thickness. Hence, a greater volume of active material is contributing to the emission. There is a limiting factor in the LETFEL device and this is due to the attenuation of the structure. Theoretically, an increase in device length will lead to an increase in the observed luminance. This does prove to be true up to a certain length. Above this length no increase in luminance is observed, see figure 1.5. This length is known as the attenuation length of the device. Practically it means that the extra light generated at a distance further from the aperture than the attenuation length is lost in the device structure. These losses can be attributed to absorption, scattering and evanescent losses.
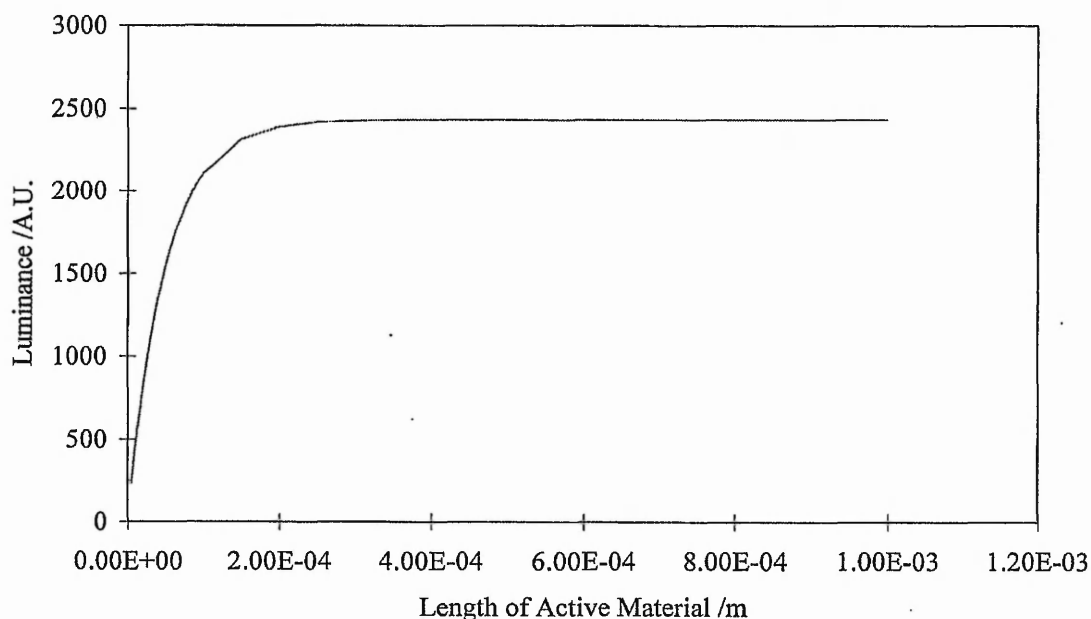
Figure 1.5 Increase in observed luminance with an increase length of active material (device length). Taken from section 3.5.2.

1.5.2. The Inherent Waveguiding Effect

The waveguiding effect can be explained by considering the refractive index profile of a LETFEL device. When the lateral emission is employed, the inherent lightguiding of the structure is utilised. For such lightguiding to occur the refractive index of the phosphor must be greater than that of the insulator so that optically the structure of the LETFEL device is that of a step-index waveguide. A step-index waveguide may support a number of TE modes. The number of modes is dependent on the thickness of the phosphor and the difference in the refractive indices of the phosphor and dielectric. However, since the cladding thickness, typically ~ 300 nm, is smaller than the wavelength of the emitted light (585 nm for ZnS:Mn phosphor), light energy may be lost via evanescent coupling out of the waveguide. Shown in figure 1.6 is the predicted decay of this evanescent

wave as a function of cladding thickness for each of the four TE modes that may

be theoretically supported by a guide layer of 800 nm thickness, which is typical

for a LETFEL device. The decay factor is determined by [16]:-

$$F(y) = \exp\left\{\frac{-2\pi n_2}{\lambda_0}\left[\left(\frac{n_1}{n_2}\right)^2 \sin^2\theta_i - 1\right]^{1/2} y\right\} \qquad (1)$$

Where F(y) is the decay factor, n_1 = guiding layer and n_2 = cladding layer

refractive indices (for our devices n_1=2.35 [ZnS:Mn] and n_2=1.9 [Y_2O_3]), θ_i is the

angle of incidence of the light and λ_0 is the wavelength in a vacuum. Hence for a

typical cladding thickness of 300 nm, significant energy loss may occur for the

higher modes

Therefore, if an increase in cladding thickness could be achieved a corresponding

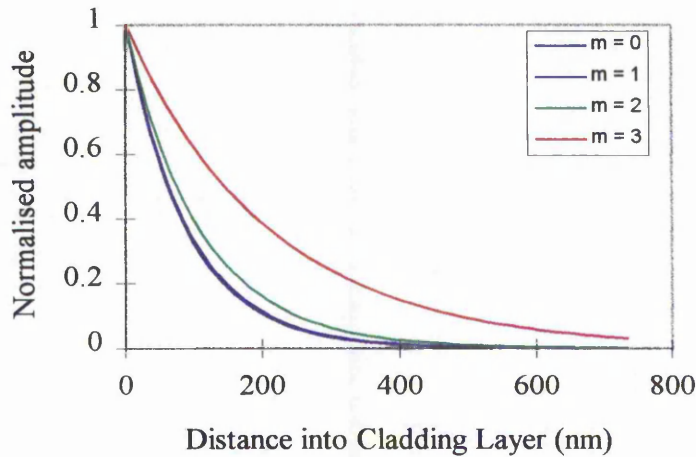increase in luminance would be expected.

Figure 1.6 Decay of the four TE modes of the evanescent wave in a 800 nm thick
ZnS:Mn guide layer with Y_2O_3 cladding

Prior to this investigation Yttrium Oxide (Y_2O_3) with $\varepsilon_r = 16$ was used as the cladding for the devices fabricated at Nottingham Trent University[17]. The thickness of these layers cannot be increased without an increase in Vth, due to the dielectric constant of the material. However, if a different material with a higher dielectric constant is used, the cladding thickness could be increased.

1.6 Overview of Insulator Materials

Y_2O_3 is currently employed as the insulator in the LETFEL device structure [17]. As discussed in section 1.5, if the thickness of the insulating films in the device is increased, an increase in both the threshold and the drive voltage would result. However, a beneficial increase in the light confinement should also occur. This increase in confinement would thus lead to an increase in observed luminance, since more light would reach the emitting aperture due to an increase in the effective attenuation length. With regards to the overall performance of the device an increase in drive voltage would be detrimental. This is due to the fact that higher voltage drive electronics would be required and hence an increase in the overall system cost would result. Consequently, a new material with a higher dielectric constant needs to be utilised to facilitate increasing the insulator thickness. To determine such a replacement dielectric for Y_2O_3, not only the properties of the dielectric need to be suitable for use in a LETFEL device, but also compatibility with the rest of the LETFEL device structure, including the

processing required to fabricate that device must be considered. The three critical parameters of the dielectric material are :-

1) A high dielectric constant, ε_r. For improvement in device performance $\varepsilon_r > 16$, which is the dielectric constant of Y_2O_3.

2) A refractive index, n < 2.35. 2.35 is the refractive index of the phosphor, ZnS:Mn. If n > 2.35 the device will not exhibit the characteristics of a waveguide.

3) A high breakdown strength, E_{bd}. This must be in the order of MV cm^{-1} to avoid catastrophic breakdown of the device.

To quantify the dielectric properties it has been shown that the charge storage capacity (CSC = $\varepsilon_r\varepsilon_0 E_{bd}$) of the insulator films needs to be at least three times that of the phosphor [18]. Typically, this charge storage capacity must exceed 3μCcm^{-2}.

For example in the case of Y_2O_3[19] :-

$$C.S.C. = 16 \times (8.854e^{-14}) \times (3.85e^{6}) \ \mu C \ cm^{-2}$$

$$= 5.55 \ \mu C \ cm^{-2}.$$

5.55 μC cm^{-2} is higher than the required typical value of 3 μC cm^{-2} and therefore Y_2O_3 exhibiting the above characteristics theoretically is suitable for use in LETFEL devices.

The integration of a new dielectric into the LETFEL device and fabrication process is as important as the required characteristics detailed above. In summary, the dielectric material needs to adhere to the silicon substrate, the phosphor, the Al electrode and finally the SiO_2 micro-mirrors. It also has to be unaffected by the other fabrication techniques including the deposition, annealing and etching of the additional layers. The current fabrication route is described in detail in chapter 4. Briefly, the Y_2O_3 and ZnS:Mn films are deposited at 200 °C by RF Magnetron Sputtering in an Ar atmosphere, then annealed at 700 °C. An Al electrode is deposited by DC Magnetron Sputtering at room temperature in an Ar atmosphere. A passivation layer is deposited by PECVD at 300 °C and all etching is carried out by Reactive Ion Etching (RIE) in mixtures of various gases including, Oxygen, Freon 14 and 23, Argon and Silicon TetraChloride, depending on which material is being etched.

This section gives details of some of the other insulator materials currently used as insulators in TFEL devices. Of course the use of thin film insulators is not limited to AC TFEL devices. Other applications include miniature capacitors and improving DRAM[20,21]. The materials used for these applications have to have very high dielectric constants to reduce the size of the devices to a minimum. The group of materials used for these devices has therefore been studied to determine

which materials currently used in the semiconductor industry may be suitable for LETFEL devices.

1.6.1 Insulator Materials for TFEL Devices

There are many groups around the world developing AC TFEL devices. Each group has different aims for their final devices. These include flat panel displays for computers and other applications, a replacement source to be used in electrophotographic printing and miniature devices for either head up displays (HUD's) or helmet mounted displays (HMD's).

Within these areas different aspects of the device structure are being investigated. These include the overall luminance of the device, the reliability, the breakdown processes and full colour capability. Investigations are also being carried out into optimising the phosphor material and composition, the effect on the type of and length of annealing and the effect of the insulator material.

For this investigation, the main area of interest is the insulating material used in TFEL devices. Table 1.2 summarises the range of insulating materials typically used in TFEL devices.

Insulator		Phosphor		Threshold Voltage Vth /Volts	Drive Frequency /Hz	Max. Luminance /fL	Reference
Material	Thickness /nm	Material	Thickness /nm				
Y_2O_3	300	ZnS:Mn	800	200	5000	5000	17
$BaTiO_3$ Ceramic Sheet	200,000	ZnS:Mn	400	100	5000	1800	22
SiO_2 / Si_3N_4		ZnMgS:Mn	700		100	97	23
Ta_2O_5	350	$ZnS:TbF_3$	700	135	1000	85	24
SiO_2 / Ta_2O_5	700	ZnS:Mn	720	190	-	290	25

Table 1.2 Comparison of AC TFEL devices utilising different insulator materials

1.6.2 Alternative Dielectric Materials

A dielectric material used for LETFEL devices as an alternative to Y_2O_3 must exhibit characteristics of $\varepsilon_r > 16$ and $n < 2.35$ as well as compatibility with the thin film deposition and device fabrication processes. Table 1.3 shows details of eight potential high ε_r materials which have been utilised in thin film form for various applications. These materials have primarily been chosen for review here due to their high dielectric constants and fabrication procedures, which show promise for integration into the current LETFEL device fabrication route.

Material	Dielectric Constant ε_r	R.I. n	Deposition Temp Ts /°c	Annealing Temp Ta /°c	Deposition Method	References
Barium Titanate	10-7000	1.9-2.34	0-930	0-1200	RF Mag. Sputtering	26-34
Lead Titanate	100-150		460-560	0-750	RF Mag. Sputtering	35,36
Strontium Titanate	250-300		400-600	500	RF Mag. Sputtering	37,38
BST	250-320		500-550		RF Mag. Sputtering	39,40
PZT	780-1180		0-800	600	RF Mag. Sputtering	41,42
PLT	290-1216		160-620	750	DC and RF Mag. Sputtering	43,44
BPZT	550		200	0-250	RF Mag. Sputtering	45
PLZT	600		300-580	700-800	RF Mag. Sputtering	46

Table 1.3 Summary of prospective thin film insulator materials for use in LETFEL devices

Key
R.I. = Refractive Index
BST :- Barium Strontium Titanate   PZT :- Lead Zirconate Titanate
PLT :- Lead Lanthanum Titanate   BPZT :- Barium Lead Zirconate Titanate
PLZT :- Lead Lanthanum Zirconate Titanate

From table 1.3 it can be seen that all of the materials exhibit suitably high dielectric constants to be considered for use in a LETFEL device.

However, it is not only the dielectric constant that is crucial in the choice of a new material. The refractive index of the dielectric is critical to produce the waveguide structure of the device. Specifically, the refractive index, n, must be less than that of the phosphor, 2.35. For most of the materials listed in table 1.3 the values of refractive index were unavailable. Also from table 1.3 Lead

Titanate, Strontium Titanate, BST and PLZT can be disregarded due to the high deposition temperatures, which makes them incompatible with the deposition of the phosphor thin film.

Barium Titanate seems to be the most suitable as both the dielectric constant and the refractive index can be controlled by the method of deposition and post deposition processing. LETFEL devices are typically deposited at 200 °C and annealed at 700 °C, for maximum luminance and reliability. Hence, the deposition and annealing of $BaTiO_3$ thin films reported here are within these fabrication parameters. This suggests that integration may be possible. A more detailed review of $BaTiO_3$ thin films was undertaken and is summarised in table 1.4. Most of the work previously published dealt with either the dielectric constant of the films or the refractive index, not both. For a LETFEL device it is both of these characteristics in addition to the dielectric breakdown strength which determine the suitability of the material. Therefore a detailed investigation into these parameters is required.

Reference	Dielectric Constant ε_r	R.I. n	Deposition Temp Ts /°C	Annealing Temp Ta /°C	Power /W	Gas Mixture %O$_2$ in Ar	Growth Rate nm/min
26			0		300	0	3-11
27		1.9-2.1	200		200	20	0.9-2.4
28		1.9-2.1	27-227			0	
29	15-20		350		150	20	2.8
30	43	2.06	6-7		100	0,20,40	0.5-0.7
31	16-300		23-500	0-500			10
32	15-250	2.34	105-650	1000	200	0,5	8
33	50-100		350		150	20	2.8
34	10-7000		340-930	935-1200	400	0,5,10	5.5

Table 1.4 Summary of the characteristics of BaTiO$_3$ thin films deposited by RF sputtering

1.7 Scope and Structure of Thesis

Significant progress has been made to date in the field of the LETFEL device. There is however much research to be done to move this technology towards the ultimate goal of achieving the high specification requirements for use in HMD's, namely a display exhibiting high resolution (> 600 dpi), high luminance (> 3000 fL), high contrast ratio, high reliability and a long lifetime (>10,000 hrs). The overall aim of the research presented in this thesis is thus to increase the performance of the LETFEL display. Hence, the individual objectives of the research presented here are as follows :

1.7.1 Objectives

(i)　To investigate the deposition of, and characterise a replacement dielectric material for use as the insulator material in the LETFEL structure in order to enhance the emitted luminance.

(ii)　Examine the deposition and characterisation of test LETFEL devices utilising the replacement dielectric material.

(iii)　Develop a theoretical model for the LETFEL device based on the theory of the planar dielectric waveguide structure.

(iv)　Optimise the LETFEL fabrication route.

1.7.2　Structure of the Thesis

Chapter 2 describes the research into RF Magnetron sputter deposition of $BaTiO_3$ thin films for use in LETFEL devices.

Chapter 3 details the investigation into the test LETFEL devices utilising $BaTiO_3$ thin film insulators. The effect of the insulator thickness is investigated with respect to the observed luminance, drive voltage and the attenuation coefficient. Also presented is the development of a first order geometric model of the LETFEL device structure to explain the optical behaviour.

Chapter 4 details the optimisation of the fabrication route.

Finally, chapter 5 includes the conclusions of this thesis and a summary of ongoing research. Suggestions for the solutions of remaining problems are also proposed along with proposals for the future enhancement of the LETFEL device.

1.8 References

1   S. Matsumoto, *Electronic Display Devices*, (Wiley, New York) 1984.

2   L. Tannas, *Flat Panel Displays and CRT's,* Van Nostrand Reinhold Co. (New York) 1985.

3   H. Bohm, S. Haisch, H.Warnatz and M. Dupuis, *Helmet and Head Mounted Displays III (SPIE),* 3362 1998 p32.

4   J. Arthur and T. Bland, *The Electronic Information Displays Conference,* 1 1997 p1-4.

5   C.T. Bartlett, *Image Sciences and Display Technologies (SPIE),* 2949 1996 p112-124.

6   A. Silzars, *The New Displays: Technologies, Markets, Applications (Photonics West 2000)*, SPIE Jan 2000.

7   C. Waldelof, T. Lindblad, N. Friberg and D. Boestad, *Helmet and Head Mounted Displays III (SPIE),* 3362 1998 p302-310.

8   J. H. Burroughes, *Extended abstracts from the Fourth International Conference on the Science and Technology of Display Phosphors.* September 1998 (Oregon). p 133 – 136.

9   G. Destriau, *Jnl de Chimie Physique et de Physico-Chimie Biologiques,* 33, 1936. 587

10   L. Tannas, *Flat Panel Displays and CRT's,* Van Nostrand Reinhold Co. (New York) 1985. Chap. 8 p237.

11   T. Inoguchi, M. Takeda, Y. Kakihara, Y. Nakata and M. Yoshida, *SID 74 Digest* 84 1974 84

12   M.J. Russ and D.O. Kennedy, *J. Electrochem Soc.*, 114 1967 p1066

13   C. B. Thomas, I. P. McClean, R. Stevens and W. M. Cranton, *IEE Electronics Letters,* 30 16 1994 p1350.

14   E. Bringuier, *Jnl. Appl. Phys.,* 75 9 1994 p4291.

15   R. Stevens, C. B. Thomas and W. M. Cranton, *IEEEE Electron Device Letters,* 15 3 1994 p97

16   J. Wilson and J.F.B. Hawkes; *Optoelectronics :- An Introduction,* (Prentice Hall, London, 2nd Edition) (1988) P 307.

17   W. M. Cranton, C. B. Thomas, R. Stevens, M.R. Craven, S. O. Barros, E. Mastio and P. S. Theng, *The Electronic Information Displays Conference,* 1 1997 p10-15.

18   D. M. Alt, D. B. Dove and W. E. Howard, *J. Appl. Phys.,* 53 1982 p5186.

19   W.M. Cranton PhD. Thesis University of Bradford 1995.

20   T.B. Wu, C.M. Wu and M.L. Chen,*Appl. Phys. Lett.,* 69(18), 1996 p2659.

21   J-H. Joo, Y-C. Jeon, J-M. Seon, K-Y. Oh, J-S. Roh and J-J. Kim, *Jpn. J. Appl. Phys. 36 1997 p4382.*

22   H. Nanto, T. Minami, S. Murakami and S. Takata, *Thin Solid Films,* 164 1988 p363.

23   M. Noma, K. Tanaka, A. Mikami and M. Yoshida, *J. Appl. Phys.,* 84(11) 1998 p6321.

24   C-T. Hsu, Y-K. Su and M. Yokoyama, *Optical Engineering,* 32(8) 1993 p1803

25   J. Miat, M. Koizumi, H. Kanno, T. Hayashi, Y. Sekido, I. Abiko and K. Nihei, *Jap. Jnl. Appl. Phys.* I26 (5) (1987) p L541.

26   N.M. Abuhadba and C.R. Aita, *Jnl. Appl. Phys.* **71** (1992) p3045.

27   A. Mansingh and C.V.R. Vasanta Kumar, *Jnl. Mat. Sci. Lett.*, **7** (1988) p1104.

28   M. Wöhlecke, V. Marrello and A.Onton, *Jnl. Appl. Phys.* **48**(4) (1977) p 1748.

29   H. Venghaus, D. Theis, H. Oppolzer and S. Schild, *Jnl. Appl. Phys.* **53**(6) (1982) p 4146.

30   K. Screenivas and A. Mansingh, *Jnl. Appl. Phys.* **62**(11) (1987) pp 4475.

31   I.H. Pratt and S. Firestone, *Jnl. Vac. Sci. & Tech.* **8**(1) (1971) pp 256.

32   C.A.T. Salama and E. Siciunas, *Jnl. Vac. Sci. & Tech*, **9**(1) pp 91.

33   A. Yamanashi, K. Tanaka, T. Nagatomo and O. Omoto, *Jap. Jnl. Appl. Phys.* Part 1   **9B** (1993) pp 4179.

34   T.L. Rose, E.M. Kellier, A.N. Scoville and S.E. Stone, *Jnl. Appl. Phys.* **55**(10) (1984) pp 3706.

35   A. Pignolet, P.E. Schmid, L. Wang and F. Lévy, *Jnl. Phys. D: Appl. Phys.*, **24** (1991) p 619.

36   H. Maiwa, N. Ichinose and K. Okazaki, *Jap. Jnl. Appl. Phys.*, **31** (1992) p3029.

37   K. Abe and S. Komatsu, *Jap. Jnl. Appl. Phys.*, **31** (1992) pp 2985.

38   T. Kuroiwa, T. Honda, H. Watarai and K. Sato, *Jap. Jnl. Appl. Phys.*, **31** (1992) pp 3025.

39   T.S. Kim, M.H. Oh and C.H. Kim, *Thin Solid Films*, **254** (1995) pp 273.

40   S.G. Yoon and A. Safari, *Thin Solid Films*, **254** (1995) pp 211.

41   K. Torii, T. Kaga, K. Kushida, H. Takeuchi and E. Takeda, *Jap. Jnl. Appl. Phys.*, **30**(12B) (1991) pp 3562.

42   K. Hirata, N. Hosokawa, T. Hase, T. Sakuma and Y. Miyasake, *Jap. Jnl. Appl. Phys.*, **31**(9B) (1992) pp 3021.

43   H.H. Kim, K.S. Sohn, L.M. Casas, R.L. Pfeffer and R.T. Lareau, *Jnl. Electrochemical Society*, **142** (1995) pp1640.

44   K. Komaki, T. Kamada, S. Hayashi, M. Kitagawa, R. Takayama and T. Hirao, *Jap. Jnl. Appl. Phys.*, **33**(3B) 1994) pp L443.

45   K. Torii, T. Kaga and E. Takeda, *Jap. Jnl. Appl. Phys.*, **31**(9B) (1992) pp 2989.

46   E.S. Ramakrishnan and W.Y. Howng, *Jnl. Vac. Sci. & Tech.*, **10**(1) (1992) pp 69.

Chapter 2 The Growth and Characterisation of Barium Titanate Thin Films

2.1 - Introduction

Need exists for the optimisation of the insulator layers in the LETFEL device structure. The structure described in section 1.5 is that of a step index waveguide. Shown in figure 2.1 is the propagation of the energy in each of the four TE modes supported by the Y_2O_3 (300 nm) / ZnS:Mn (800 nm) / Y_2O_3 (300 nm) LETFEL device structure. A full description of how this figure was determined is given in section 3.3. Since the thickness of the insulators, 300 nm, is less than the wavelength of the emitted light, 585 nm, an amount of energy may be lost due to evanescent coupling out of the waveguide. This light energy will propagate outside the device structure where it may be lost due to absorption in the Si substrate or Al electrode. It may be concluded that if the thickness of the insulator layers can be increased, more of the light generated in the device would be confined in the device structure. Therefore, an improvement should be seen in the light guiding properties of the structure. This improvement should in turn decrease the losses in the device structure and hence an increase in luminance should be observed.
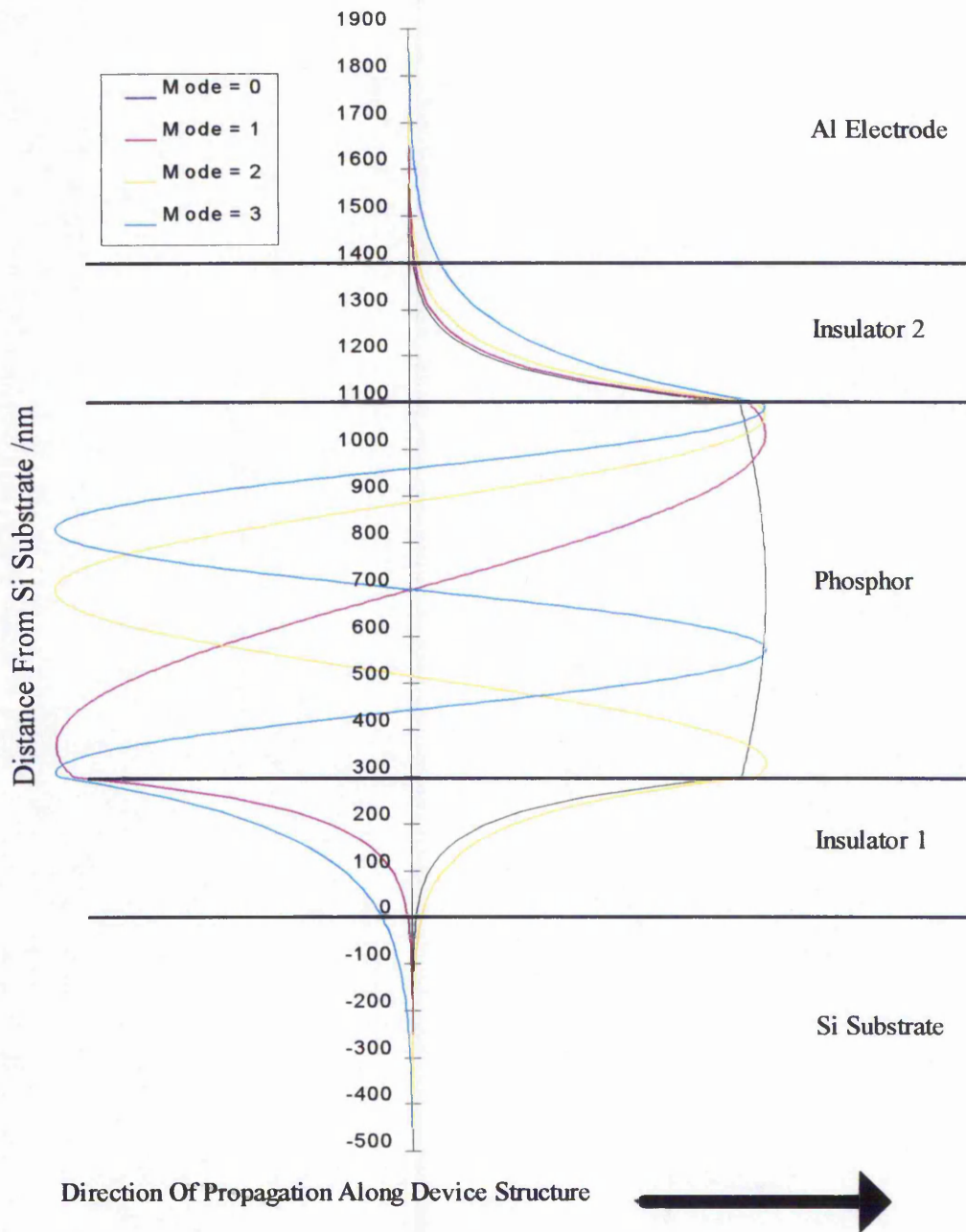
Figure 2.1 Energy profile of light propagating through a Y_2O_3 based LETFEL device. The light propagating in the Si or Al may be lost as it is outside the waveguide. The structure shown is :-

$$Si/Y_2O_3(300 \text{ nm})/ZnS:Mn(800 \text{ nm})/Y_2O_3(300 \text{ nm})/Al.$$

If the evanescent losses are indeed reducing the light output from LETFEL devices, improvement should be achieved by increasing the thickness of the insulating layers. However, to do this with no subsequent increase in the drive voltage, a material with a dielectric constant greater than that of the presently utilised Y_2O_3 ($\varepsilon_r = 16$) must be used. In addition, any material utilised as an insulator in a LETFEL device must also exhibit a refractive index, n, less than that of ZnS:Mn (n=2.35) to enable waveguiding and also a high breakdown strength. Specifically, from the review of insulator materials utilised in TFEL devices presented in section 1.6, it may be concluded that $BaTiO_3$ thin films have the potential for use as insulators in a LETFEL device. Specifically, the requirements are a high dielectric constant, $\varepsilon_r > 16$, a refractive index, n< 2.35, and a breakdown strength, E_{bd}, of at least 1 MV/cm. To quantify these properties it has been shown that the charge storage capacity, Eq. 2.1., of the insulator needs to be at least three times that of the phosphor. Typically, this charge storage capacity must exceed 3 μCcm^{-2}[1].

$$\text{Charge Storage Capacity, C.S.C.} = \varepsilon_r \varepsilon_0 E_{bd} \qquad \text{Eq. 2.1}$$

For example in the case of Y_2O_3, C.S.C. = 5.55 $\mu C\ cm^{-2}$[2] :

$BaTiO_3$ thin films under certain deposition and post deposition annealing conditions can exhibit the characteristics required for the insulators in LETFEL devices. These include a dielectric constant ranging from 10 to 7000, a refractive index in the range of 1.9 to 2.51 and a breakdown field of 1.5 to 6 $MVcm^{-1}$ [3-11].

However, these characteristics are highly dependant on the deposition technique. Required therefore is a detailed investigation into the deposition and post deposition processing of BaTiO$_3$ thin films, with specific emphasis on compatibility with LETFEL device fabrication.

This chapter details the choice of deposition technique, the commissioning of a deposition system and the results from the full investigation into BaTiO$_3$ thin film deposition specifically for use in LETFEL devices.

2.2 - Deposition of Barium Titanate Thin Films

There are two primary methods of thin film deposition, 1) Physical vapour deposition and 2) Chemical vapour deposition. The reader is directed to Vossen and Kern for a comprehensive list of available techniques[12].

The method of deposition and any post deposition processing will have a marked effect on the properties of the thin film deposited. For example the deposition of BaTiO$_3$ thin films has been reported by many methods. These include Metal Organic Chemical Vapour Deposition (MOCVD) [13], The Sol - Gel method [14] and Sputter deposition [7] to mention a few. The reported values of the dielectric constant range from 10 to 7000, a refractive index in the range of 1.9 to 2.51 and a breakdown field of 1.5 to 6 MVcm^{-1} [3-11]. The high degree of variation in these characteristics is due to the deposition and post deposition procedures.

Consequently, the choice of deposition and post deposition treatment is very important, when the objective is to obtain a thin film exhibiting characteristics within specific limits. RF magnetron sputtering has been chosen as the method of deposition for this investigation, for the following reasons. From the review in section 1.6 it can be seen that when RF magnetron sputtering is employed, the characteristics of the resultant $BaTiO_3$ thin films exhibit suitable characteristics for use in LETFEL devices. That is a high dielectric constant, >16, a refractive index less than 2.35 and a breakdown strength in the order of $MVcm^{-1}$. By the variation of the RF magnetron sputter conditions a level of control over the characteristics of the thin films can be achieved. This in turn allows the optimisation of these conditions to produce the required values of dielectric constant, refractive index and breakdown strength for thin films to be utilised in LETFEL devices. For example, it has been reported that the dielectric constant can be increased from 12 to 43 with the increase of oxygen concentration from 0 % to 40 % in the sputter atmosphere [7]. Also shown by previous work is that dielectric constants of 110 to 300 have been produced by varying the deposition temperature from 610 to 700 °C[15]. Post deposition annealing also has a marked effect on dielectric constant with a variation from $\varepsilon_r = 16$ to $\varepsilon_r = 300$ with an increase in post deposition annealing temperature from 0 to 500°C [8]. In terms of the refractive index of $BaTiO_3$ thin films, this has been reported to rise from 1.9 to 2.1 with an increase in deposition temperature from 27 to 227 °C[5]. Further considerations are that successful TFEL devices have been reported utilising both thin films of $BaTiO_3$ and $BaTiO_3$ ceramic substrates[16,17].

Finally, RF magnetron sputtering is the method presently used to deposit both Y_2O_3 and ZnS:Mn thin films in the LETFEL device at NTU. Consequently, there is a valuable resource of knowledge and experience in this deposition technique within the displays group at NTU.

2.2.1 - Sputtering

To sputter is to *"deposit by using ions to eject particles of material from a target"*[18]. Sputtering is a physical method of deposition, which has been developed over many years since it was first discovered by Frans Penning in 1936[19]. Sputter deposition is generally classified by the technique used to apply the electrical power to the target, i.e. either as DC sputtering or RF sputtering. DC sputtering is commonly used for the deposition of conductors, RF sputtering is utilised for the deposition of insulators. As $BaTiO_3$ is an insulator, RF sputtering is of interest here.

A basic RF sputter deposition system is shown in figure 2.2. The target forms the cathode of the system and the substrate may be electrically grounded, biased or left floating. Initially, the system is evacuated to a base pressure of the order of 1 $\times$ 10^{-7} bar. This may be achieved by utilising a number of pumping methods including a turbo pump, a cryo pump, or a mechanically backed diffusion pump. An AC voltage is capacitively coupled to the target via a water cooled metal back

plate. At a suitable gas pressure and applied RF power, electron emission from the target excites the sputter gas and a self-sustained glow discharge, or plasma, results. For non-reactive sputtering, an inert gas such as argon is used at a pressure of between 3 mT and 100 mT. Although the applied bias is alternating the target typically becomes the cathode of the system by acquiring a net negative potential. This occurs due to electrons being more mobile than the positive ions in the plasma. During the positive half cycle of the RF voltage more electrons are thus attracted to the target than positive ions during the negative half cycle. Hence the target acquires a negative potential. The ions produced, bombard the target surface and their incident energy is sufficient to eject the atoms of the target material. The kinetic energy of the ejected atoms is converted into heat and adhesion forces on impacting the surfaces in the chamber. Hence, to obtain growth of a thin film on a substrate, the surface requiring deposition must be positioned facing the target. Care must be taken in the design of the chamber so that any other surfaces, upon which thin film deposition occurs would be undesirable, are adequately shielded; for example, the rear of the substrate, the heater element and any view ports.

2.2.2 - RF Magnetron Sputtering

For this investigation RF magnetron sputtering has been utilised for all thin film deposition. RF magnetron sputtering has many advantages over RF sputtering. During RF sputter deposition, damage to the substrate, and hence to the depositing film, may occur. This is due to electron bombardment from the

plasma. Figure 2.3a shows a RF planar electrode. It can be seen that there is no containment of the plasma and hence electron bombardment of the substrate can occur.

An improvement to this design is to utilise RF magnetron sputtering. The difference is the inclusion of a series of magnets behind the surface of the target. Figure 2.3b shows the inclusion of the magnets in the electrode design. The magnets may be either permanent or electromagnets. The use of electromagnets allows the utilisation of either magnetron or planar sputter deposition. This is at the cost of simplicity. The need to electrically address the magnets increases the complexity of the electrode design.

The magnetic field produced by the magnetron electrode causes the plasma to be confined close to the target surface. This has two main advantages over the non-magnetron configuration: Firstly, the ionisation efficiency of the gas within the plasma is increased. This in turn leads to a decrease in the gas pressure required to sustain the plasma. This decrease in deposition pressure can be beneficial since the mean free path of the sputtered atoms is increased leading to an increase in deposition rate.

Secondly, the confinement of the plasma away from the substrate reduces the electron bombardment of the substrate. This reduces the damage to the depositing film and hence an increase in film quality will be observed.
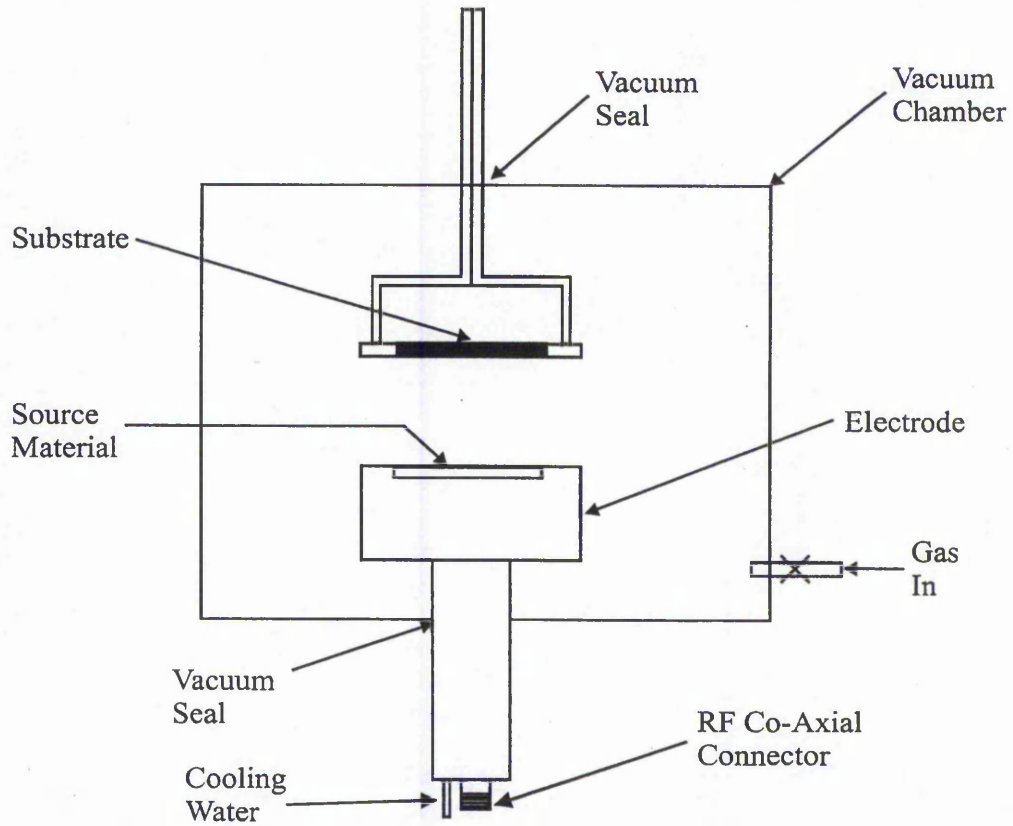
Figure 2.2 A basic sputter deposition system
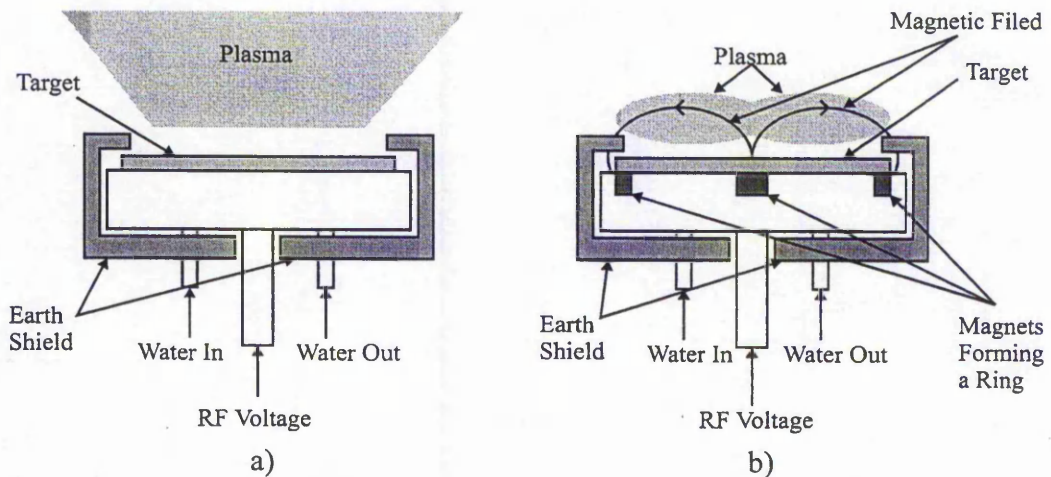
Figure 2.3 a) Planar Electrode and b) Planar Magnetron Electrode. Note the containment of the plasma in b)

2.3 - System Design

Prior to the use of $BaTiO_3$ thin films, all LETFEL device thin film deposition was performed in a custom built cluster magnetron system shown schematically in figure 2.4. Reported by others is that the deposition of $BaTiO_3$ thin films with the addition of oxygen to the sputtering atmosphere improves the dielectric characteristics of the resultant $BaTiO_3$ thin films[7]. However, for this investigation, the addition of oxygen to the LETFEL deposition system would have two detrimental effects. Firstly, the luminescent efficiency of the phosphor thin film has previously been reduced by the use of oxygen in the process chamber[2] and secondly the substrate heater coil is degraded by the presence of oxygen [20]. The latter effect is due to the material of the heating element, which is a carbon composite material, being oxidised in the presence of oxygen at high temperatures. For these reasons, therefore, the $BaTiO_3$ and LETFEL thin film growth could not occur in the same chamber, hence a secondary chamber was commissioned as part of this programme. This additional chamber was designed to mount alongside the LETFEL deposition chamber, linked via a gate valve. This facilitated the deposition of any future LETFEL devices utilising $BaTiO_3$ insulator layers without the need for removal of the substrate from vacuum. A magnetically coupled loading arm enables the insertion, transfer between and removal of the substrates from the chambers.

The secondary chamber initially consisted of an 18 inch diameter chamber, a single vertical electrode and no substrate heating facility as shown in figure 2.5.

Hence, major improvements to this had to be carried out before the thin films could be deposited. Required was a substrate heating assembly and conversion to a multi electrode system. Specifically, the addition of a substrate heating assembly was required, with sufficient manipulation of the substrate cradle to allow the transfer of substrates between the two chambers and the load lock. In addition, for increased flexibility, the chamber was adapted to accommodate up to four electrodes.

This decision is based on the configuration of the LETFEL deposition chamber, as shown in figure 2.4, which includes four RF magnetron electrodes orientated at 45° to the substrate. This allows the deposition of four different materials in the same chamber without the requirement of changing targets or deposition chambers. It has also been shown that thin films deposited from electrodes at this angle are uniform in thickness to ± 2 % across the 4" substrate[2]. Therefore to increase the flexibility of the dual chamber system it was decided to install three electrodes at the same 45° orientation in the secondary chamber with a spare port for future upgrade to a four electrode system. The new electrodes were 3" Torus 3M magnetron electrodes from Kurt Lesker Ltd.
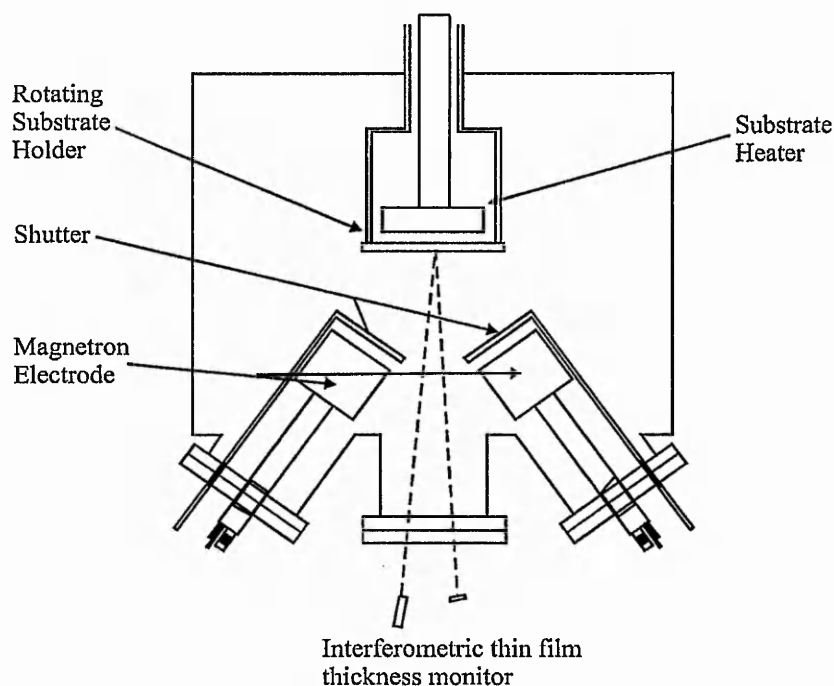
Figure 2.4 Schematic cross section of the chamber used for the deposition of LETFEL thin films
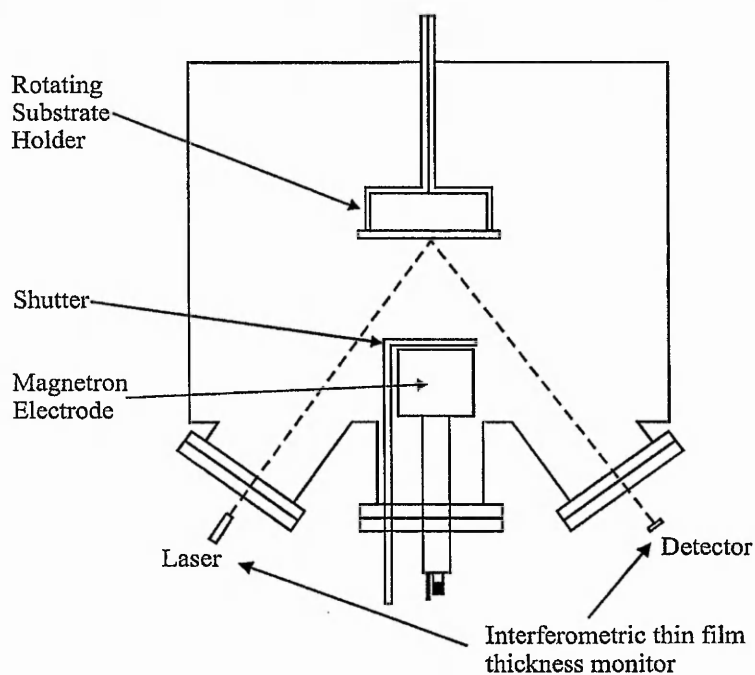
Figure 2.5 Schematic cross section of the initial configuration of the BaTiO₃ deposition chamber

2.3.1 - Substrate Heater Design

Substrate heating during the deposition is known to increase the dielectric constant of BaTiO$_3$ thin films from 110 to 300 with an increase from 610 to 700 °C[15] . Furthermore, substrate heating during deposition has been shown to reduce the amount of sputter gas entrapment in the depositing film. This in turn leads to a more uniform, higher quality film[21]. Therefore, a heater assembly was installed in the BaTiO$_3$ deposition chamber. However, budget limitations and the requirement for oxygen in the sputter atmosphere prevented the purchase of an identical heater unit as in the LETFEL deposition chamber. Therefore a new assembly had to be designed. The major design considerations for this heater assembly were:-

1) Good temperature uniformity ± 5 % across the substrate. Non-uniformity could potentially lead to a non-uniform deposition rate, dielectric constant and / or refractive index across the substrate.

2) A deposition substrate temperature of at least 200 °C. From previously reported work, BaTiO$_3$, thin films deposited at a substrate temperature of 105 °C have yielded a dielectric constant of 18 with a breakdown strength of 3.2 MV/cm[9]. Higher substrate temperatures produce increased dielectric constants, but with a reduction in breakdown strength. For example, deposition of BaTiO$_3$ thin films at a substrate temperature of 650 °C have been reported to yield a

dielectric constant of 180, but with a breakdown field of 1 MV/cm which is only just acceptable for use in LETFEL devices[9]. Ideally, a variation in substrate temperature of up to 600 °C would be investigated, but limitations on the substrate heater assembly design, particularly the use of oxygen, restrict achievable substrate temperatures to 200 °C. However, as seen by previously reported work, this temperature would be expected to provide BaTiO$_3$ thin films with $\varepsilon_r \geq 20$ and a breakdown strength of > 1 MV/cm, hence facilitating the investigation of thicker insulator films in LETFEL devices. In addition, 200 °C is also the temperature at which the ZnS:Mn and Y$_2$O$_3$ thin films are deposited. Hence, with all of the thin films deposited at the same temperature thermal stresses are minimised. For high temperature annealing of the BaTiO$_3$ thin films the heater unit in the LETFEL deposition chamber would be used.

The other factors to be considered in the design of the heater assembly are :

        3) Vertical movement to allow the insertion and removal of substrates

        4) A shield to prevent thin film deposition on the reverse of the substrate.

and,   5) Resistance to oxygen.

Initially a four bulb heater array was used, as shown in figure 2.6. The unit was suspended above the rotating substrate. It satisfied three of the five constraints, i.e. it reached 200 °C, the substrate holder could be move to allow the substrate changes and it was resistant to oxygen. Unfortunately, the uniformity of substrate heating was only ±15 % at best and thin film deposition on the rear of the substrate occurred, due to lack of shielding, see figures 2.7 and 2.8.
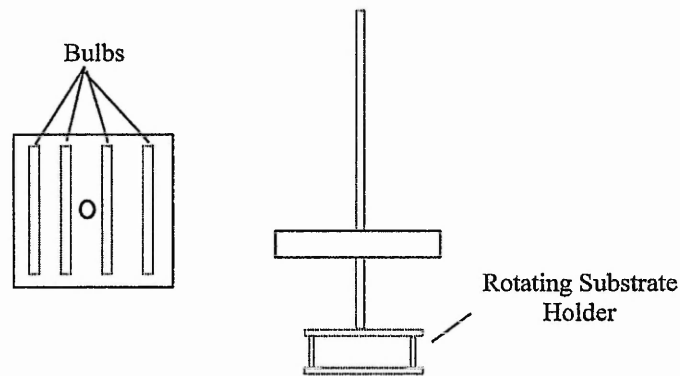
Figure 2.6 Underside view of four bulb array heater and side view
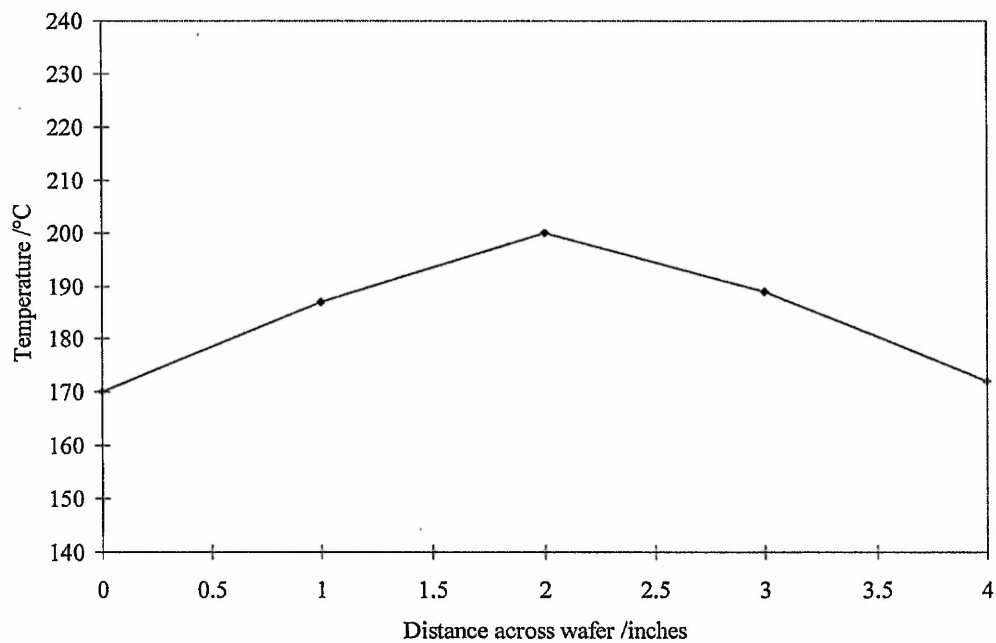
Figure 2.7 Temperature profile across a 4" substrate using the heater in figure 2.6.
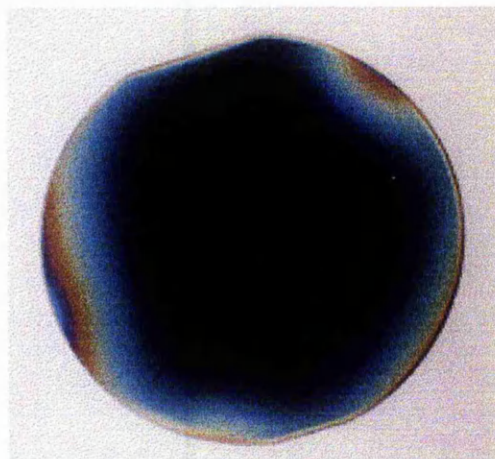
Figure 2.8 Photograph of deposition on the rear of the substrate during deposition using the heater in figure 2.6.

To address these deficiencies in substrate heating an improved system was designed and built as shown in figure 2.9. The main component is a large Aluminium plate, which can be raised and lowered to allow insertion and removal of the substrates. A heating coil was clamped onto the reverse of the plate and the integral shield on the bottom prevents deposition on the back face of the substrate. The heating coil is used to heat the aluminium plate and shield, thus radiating heat uniformly to the substrate. This configuration worked very well for two months, it was uniform to within ± 5 % at 200 °C running at 50 % applied power, 1500 watts, see figures 2.10 and 2.11. Calibration was carried out by attaching a series of thermocouples to the substrate and comparing the temperature readings with a thermocouple permanently attached to the heater unit. See figure 2.11 for the calibration curve. The main disadvantage of this set-up was that it took 45 minutes for the substrate to heat up, but otherwise this assembly worked sufficiently. However, following two months of use, the heating coil failed. After inspection it was discovered that the heating coil had fractured at some of

clamping points. This was due to expansion and contraction during heating and

cooling.
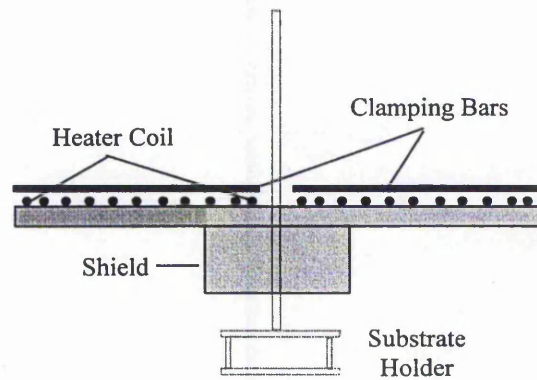
Figure 2.9 Heater assembly retrofitted to BaTiO$_3$ deposition chamber. During deposition the Aluminium plate is lowered to encase the substrate holder. This prevents deposition on the back face of the substrate.
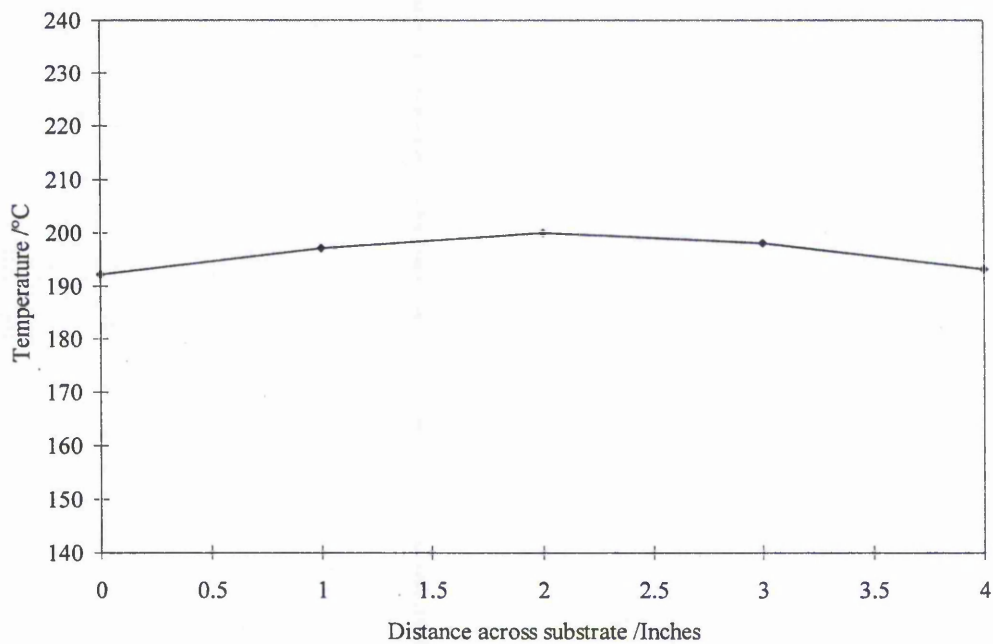

Figure 2.10 Temperature profile across a 4" substrate using the heater in figure 2.9
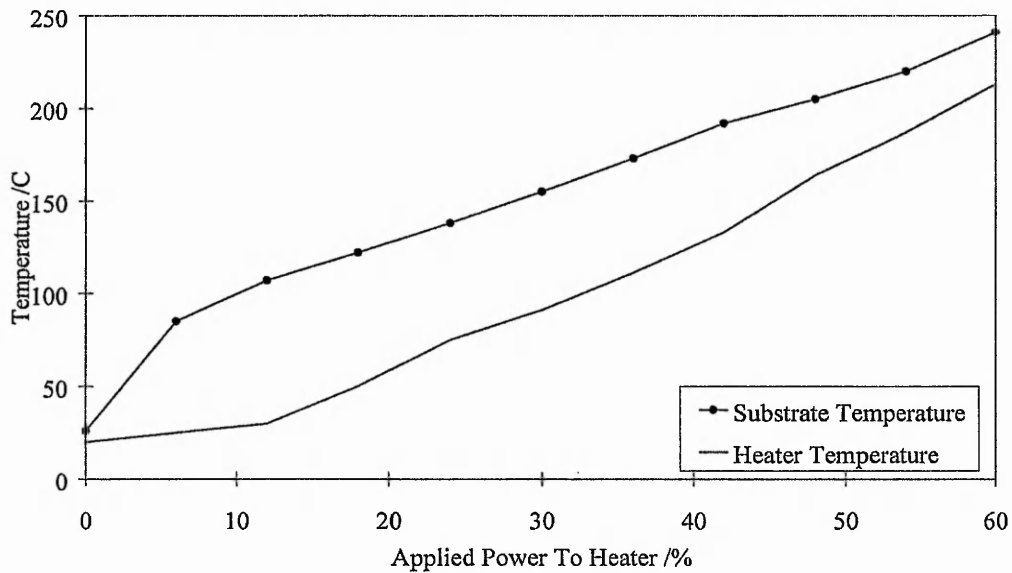
Figure 2.11 Calibration of substrate temperature compared with the heater temperature for the heater configuration in figure 2.9

Due to the problems with the clamping of the heating coil, a modification to the design was required. If the heating element was brought nearer to the substrate the heating up time would reduce. This in turn would also reduce the power consumption and should therefore increase the lifetime of the heater element. It was also decided to keep the heater on continuously to help prolong it's life and maintain temperature stability in the chamber. The new coil was smaller and was wound more tightly. This enabled it to be suspended inside the shield by tantalum wire. Power consumption was reduced to 240 watts to maintain a substrate temperature of 200 °C. Figure 2.12 shows the calibration curve for this new heater configuration. The necessity of clamping was eliminated and the uniformity of heating was determined to be ± 4 % across the substrate, as shown in figure 2.13. This new heater assembly, shown in figures 2.14 and 2.15, was in

use for over 2 years, during which all of the thin film deposition, characterisation and test device fabrication for this programme was undertaken.
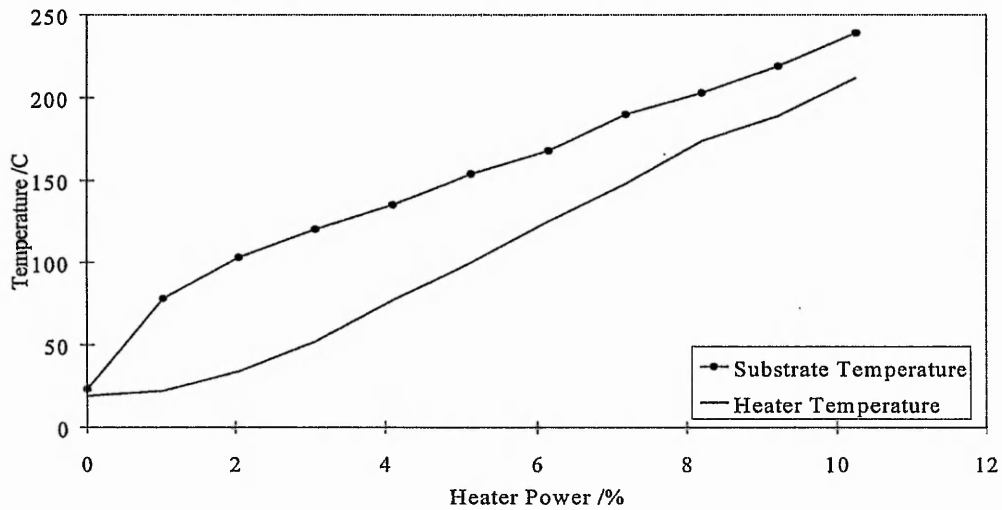
Figure 2.12 Calibration of substrate temperature compared with the heater temperature for the heater configuration in figure 2.14
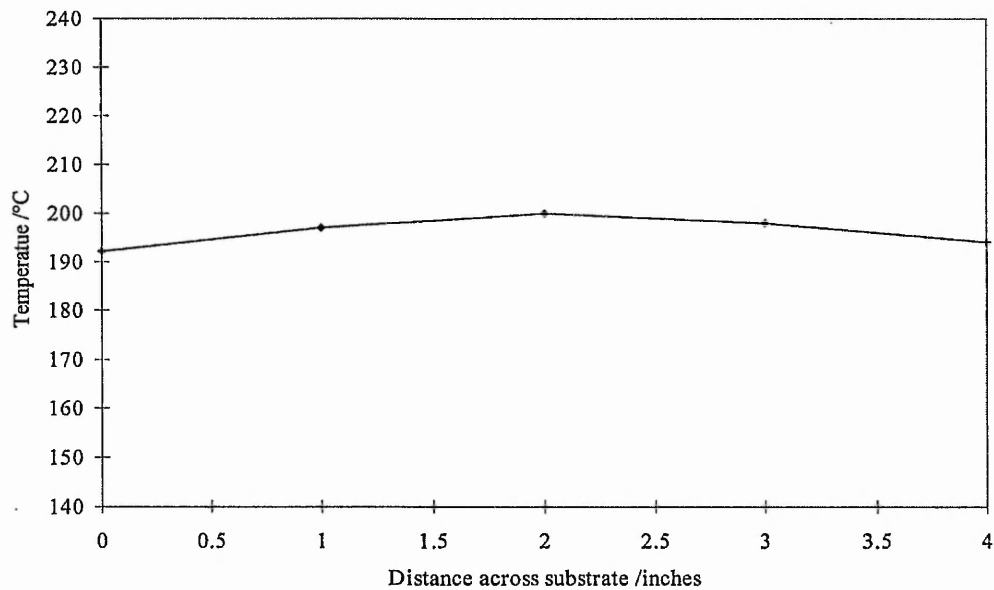
Figure 2.13 Temperature profile across a 4" substrate using the heater in figure 2.14
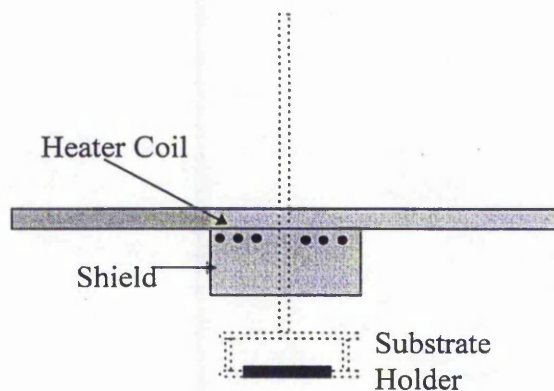
Figure 2.14 Final configuration of heater fitted to the secondary chamber. During deposition the Aluminium plate is lowered to encase the substrate holder. This prevents deposition on the back face of the substrate.
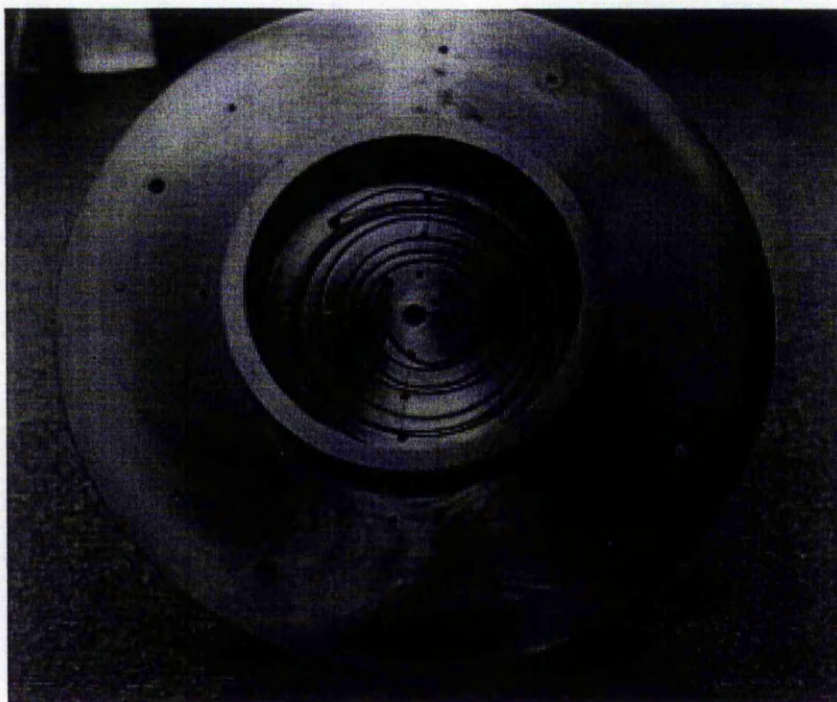
Figure 2.15 Photograph of the heater shown schematically in figure 2.14. The heating coil is suspended inside the shield.

2.3.2 - Multi Electrode Configuration

To improve the overall capability of the dual chamber system it was decided to install three electrodes in the secondary chamber. This new configuration would allow the deposition of $BaTiO_3$ (dielectric), Al (electrode) and SiO_2 (passivation) thin films without breaking the vacuum. Hence, with transfer between this chamber and the LETFEL deposition chamber, the full deposition sequence of LETFEL thin films, detailed in section 1.6, could be accommodated without the removal of the substrates from the vacuum. The three electrodes were installed in the chamber at the same angle, 45° relative to the substrate, as those in the LETFEL deposition chamber, thus maintaining continuity throughout the fabrication route. A rotating shutter system was also designed and installed to protect the electrodes when not in use. To aid the monitoring of the depositing thin film a laser interferometer was also added. Further details on the operation of the interferometer are given in section 2.5.1. The final chamber configuration is shown in figure 2.16.
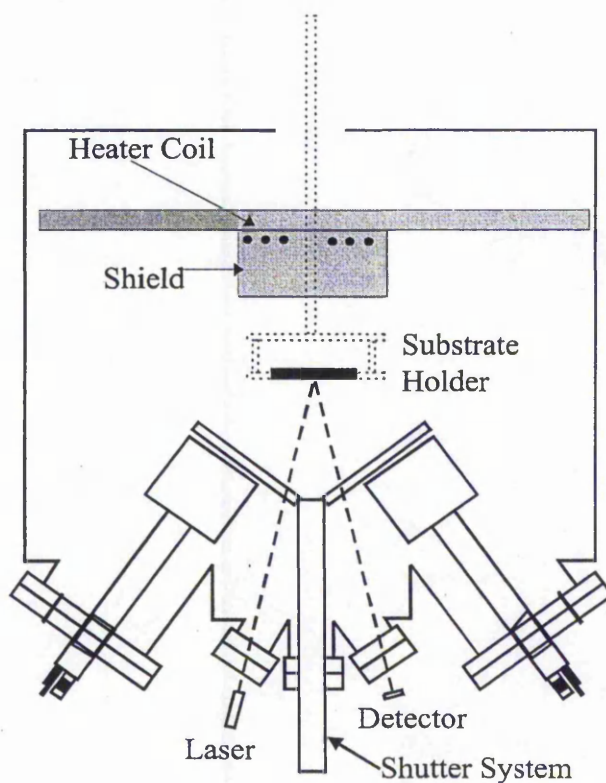
Figure 2.16 Final configuration of BaTiO₃ deposition system.

2.4 - Experimental Technique

BaTiO$_3$ thin films were deposited by RF magnetron sputtering in the system described above. The films of BaTiO$_3$ were deposited on 100 mm diameter n-type silicon wafers using as source material 99.9 % pure BaTiO$_3$ manufactured by Cerac Inc. During deposition the substrates were rotated at a controlled temperature to ensure uniformity. The gas composition and pressure were adjusted via an MKS 250 controller linked to two MKS mass flow controllers. The chamber was evacuated to a base pressure of 2.0×10^{-8} Bar via a rotary

backed diffusion pump with a long life liquid N_2 cold trap to prevent back streaming of oil and to enhance the pump rate.

Deposition occurred at 200 °C, which is the deposition temperature used for the LETFEL device [23], or with no direct substrate heating corresponding to approximately 60 °C. For both temperatures a series of films were deposited varying: (i) the partial pressure of Oxygen in the Argon sputtering gas, (ii) the overall gas pressure, (iii) the RF power supplied, and (iv) the post-deposition annealing temperature. Film thickness was monitored during deposition using an in-situ interferometric technique [24] as described below. A one hour post-deposition annealing process was performed in vacuum in the LETFEL deposition chamber, with substrates rotated to ensure uniformity. This has been shown to be the optimum annealing condition for LETFEL devices[2].

2.5 - Characterisation Procedure

2.5.1 - Thickness Measurement

(A) Interferometry

This method of monitoring the film thickness during deposition has been used successfully for LETFEL thin film deposition for the last 5 years. [24].

The reflected intensity of a visible laser beam from the thin film and substrate can be monitored via a photodiode. The reflected intensity varies due to the phase

shift produced between rays reflected from the substrate and those reflected from the thin film surface. If the reflected intensity is recorded, a series of intensity maxima and minima are produced, as shown in figure 2.17. From this data, using equation Eq. 2.2. a value for the film thickness for each cycle, or the refractive index of the sample can be determined.

$$\lambda = 2nmd \hspace{3cm} Eq. \ 2.2$$

Where λ = wavelength of the laser, d = the known thickness of the film, n = the refractive index of the material and m is an integer.

Therefore the thickness of one measured intensity cycle of $BaTiO_3$ is given by

$$d = \lambda/2n \hspace{3cm} Eq. \ 2.2a$$

Hence, if the thickness is known the refractive index can also be determined.

Initially a dry etch was used (details below) to determine the thickness of the material deposited for one complete cycle. This gave the initial deposition rate and refractive index. This method is reliant upon knowledge of the refractive index of the material. The refractive index of $BaTiO_3$ is known to vary from 1.9 to 2.1 with an increase in deposition temperature from 27 to 227 °C[5]. Therefore, the values from this method were only used as a guide during deposition and the thickness of all films deposited was subsequently confirmed by the dry etching method.
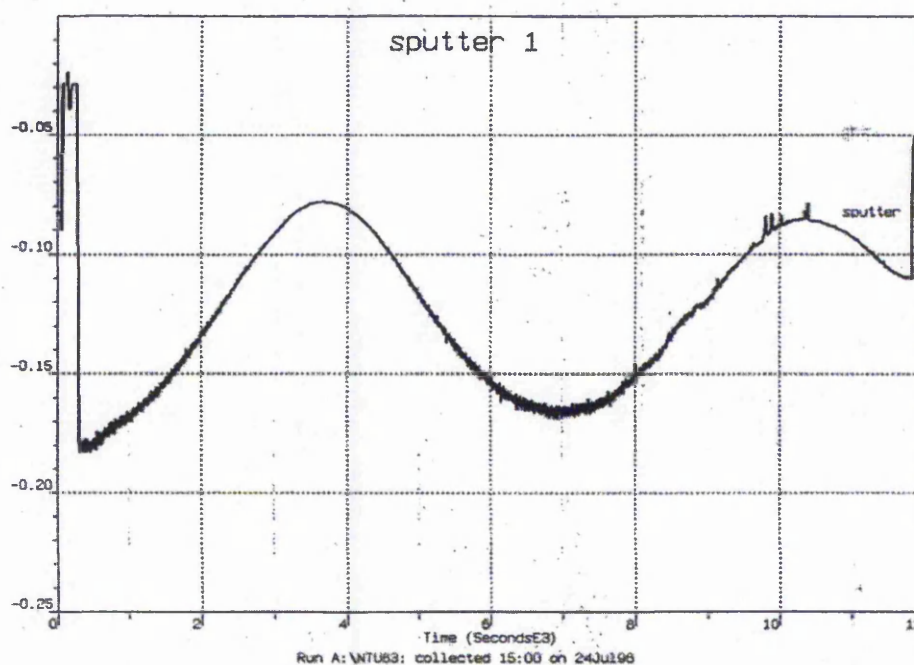
Figure 2.17 Example of interferometer reflected intensity recorded during the deposition of 300 nm BaTiO₃.

(B) Dry Etching

For thickness calibration purposes a dry etch process was used to define a step in the BaTiO₃ thin film down to the Si substrate. A photolithographic process was used to define a layer of photoresist on the BaTiO₃ thin films, as detailed in table 2.4. The role of the photoresist is to physically protect a section of the film during etching. After the etch and the removal of the photoresist a step remains in the film; this is where the thickness measurements are taken. The etch was performed in a system dedicated to the reactive ion etching (RIE) of thin films. The principle of this process is similar to sputter deposition and is known as RIE or reactive sputter etching. The difference is that in RIE the substrate replaces the

target in the deposition system and the gas utilised produces a reactive discharge. Therefore the ions remove the unmasked material from the substrate and the material is etched. Table 2.2 summarises the etching conditions. The etch was monitored in-situ using the interferometry technique, described above. Observing the trace and the film, the etch is finished at a maximum on the intensity cycle. The maximum is when there is no remaining thin film present. When no film is present there is no phase shift in the reflected intensity, therefore the maximum intensity of the laser is reflected directly to the photodiode. By direct comparison with the deposition maximum and minimum trace the exact number of cycles deposited is known, therefore a prediction of when the etch is going to finish can be made. After the removal of the photoresist, the step height of the film thickness, d, was then determined using a Sloan Dektak IIA Profilometer. Using equation 2.2, and the measured value of d, a corresponding value for the refractive index of each film was determined. Hence, when combined with the data recorded during deposition, the growth rate of the thin films could also be calculated. As it has been previously reported that the refractive index of BaTiO$_3$ can alter depending on the sputter conditions, [4,5] the determination of the thickness and refractive index was repeated for all the samples. The refractive index of the films was also confirmed by the nulling method of ellipsometery at South Bank University using a PLASMOS SD2100 ellipsometer at $\lambda = 632.8$ nm.

Step	Process	Details
1	Dehydration bake of the substrate	100 °C 2 min
2	Adhesion Promoter (HMDS type APX-1K)	APX - 1K 4 Drops 2500 rpm 10 sec.
3	HMDS bake	170 °C 20 sec.
4	Photoresist (PR) spin coat	Photoresist:-OFPR800 23 cps 1 drop 5000 rpm 1 min
5	Prebake temp. / time.	95 °C 2 min
6	Exposure to Ultra Violet (UV) Light.	Mask Aligner:-PLA500 20 sec at 350 integral
7	PR Development.	Developer:-AZ527MIF 40 seconds
8	De-ionised water rinse.	1 min
9	Hardbake Temp/Time	130 °C 60 min
10	PR descum.	O_2 Plasma 100 mT 40 W 30 sec
11	Reactive Ion Etching	See table 2.2
12	PR Strip	Remover:-AZ100 10 min
13	De-ionised water rinse.	1 min
14	Dehydration bake	100 °C 5 min

Table 2.1 Photolithographic processing steps for patterning of thin films

Material to be Etched	Partial Pressure of Argon /mT	Partial Pressure of Freon 14 (CF_4) /mT	Applied Power /Watts	Etch Rate /nm min^{-1}
$BaTiO_3$	1	4	50	3

Table 2.2 Reactive ion etch conditions for $BaTiO_3$

2.5.2 - Dielectric Constant and Breakdown Strength

Dielectric characterisation of $BaTiO_3$ thin films was achieved via the fabrication of metal insulator semiconductor (MIS) diodes, 3 mm in diameter. Electrical contacts were made by the thermal evaporation of 300 nm of Al followed by a photolithographic masking process and a chemical etch. The Al was etched in ISOFORM Aluminium Etchant, from Micro-Image technology Ltd. to form the diodes. An experiment prior to this determined that the ISOFORM Al etchant did not etch the $BaTiO_3$ thin films. An ohmic back contact to the Si substrate was made by the thermal evaporation of 500 nm of Al followed by a rapid thermal annealing process which has been shown to produce ohmic contacts to silicon[25]. Electrical characterisation was performed in a darkened probe station. Capacitance-voltage analysis was performed at 1 MHz using a computer controlled HP4192 LF impedance analyser and the electrical breakdown was measured using a Telequipment CT71 Curve Tracer.

2.6 - Results

2.6.1 - Film Deposition

The deposition rate of $BaTiO_3$ on Si was highly dependant, as expected, on the deposition variables. For new $BaTiO_3$ targets, a pre-sputter period of up to 2 hours at 0.9 Watts cm^{-2} was required before deposition commenced. This is a standard procedure to clean the target after insertion into the chamber and to equilibrate the target surface[12]. This is required since during initial deposition the different components of a target will sputter at different rates. An equilibrium at the target surface must be established for consistency in the resultant thin film composition. Following this period the deposition rate varied between 35 $nmhr^{-1}$ to 97 $nmhr^{-1}$: increasing linearly from 53 $nmhr^{-1}$ to 97 $nmhr^{-1}$ with an increase in RF power from 1.75 Wcm^{-2} to 2.62 Wcm^{-2}, decreasing from 87 $nmhr^{-1}$ to 55 $nmhr^{-1}$ with an increase in oxygen concentration from 0 % to 40 % and exhibiting a peak of 66 $nmhr^{-1}$ at 7 mT of total pressure. See figures 2.18 to 2.20.
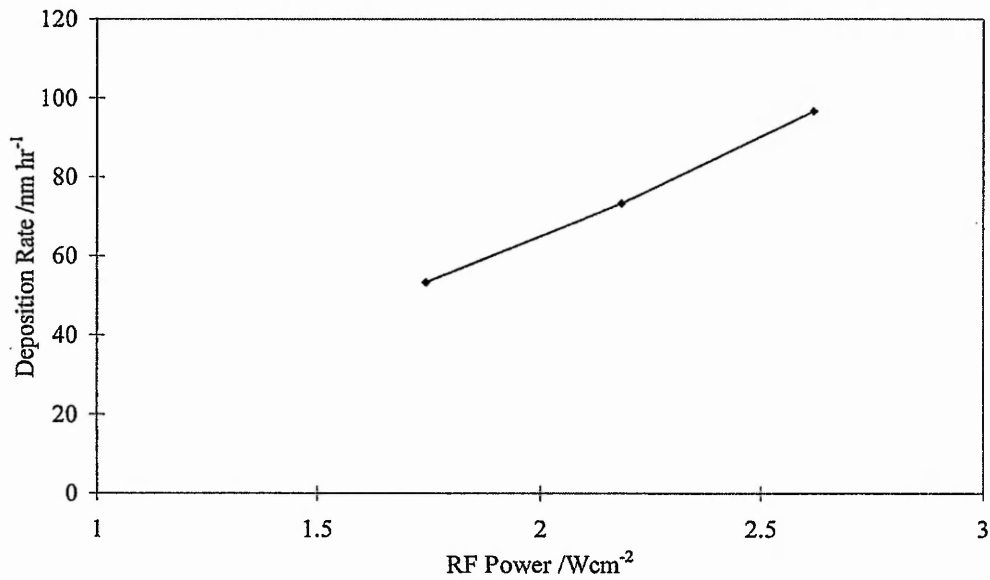
Figure 2.18 Variation in deposition rate with increase in RF power. Films deposited at 60 °C, 5 mT total pressure with a 90/10 ratio of Ar to O_2
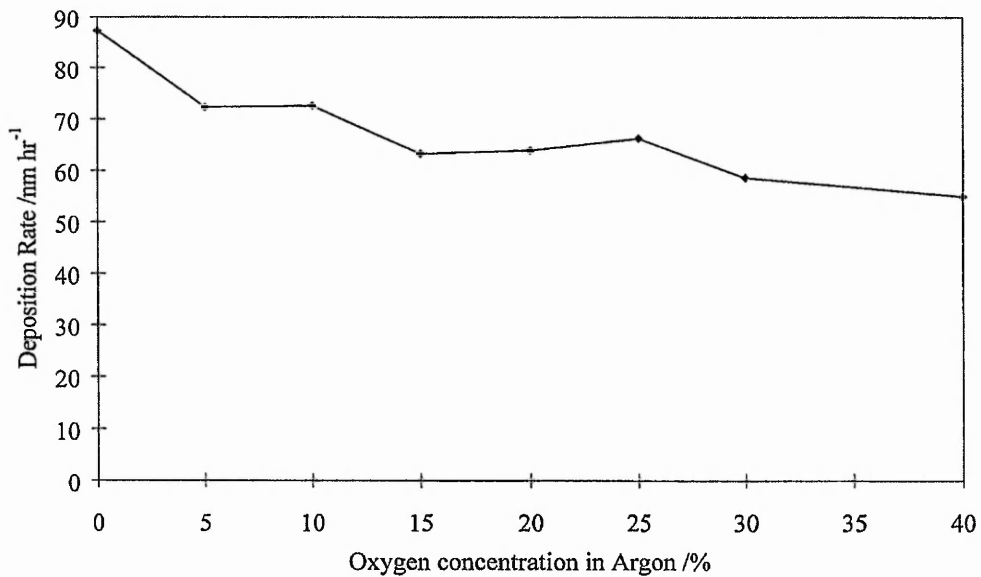
Figure 2.19 Variation in deposition rate with increase in oxygen concentration in the sputter atmosphere. Films deposited at 60 °C at 2.18 Wcm^{-2} in a total pressure of 5 mT
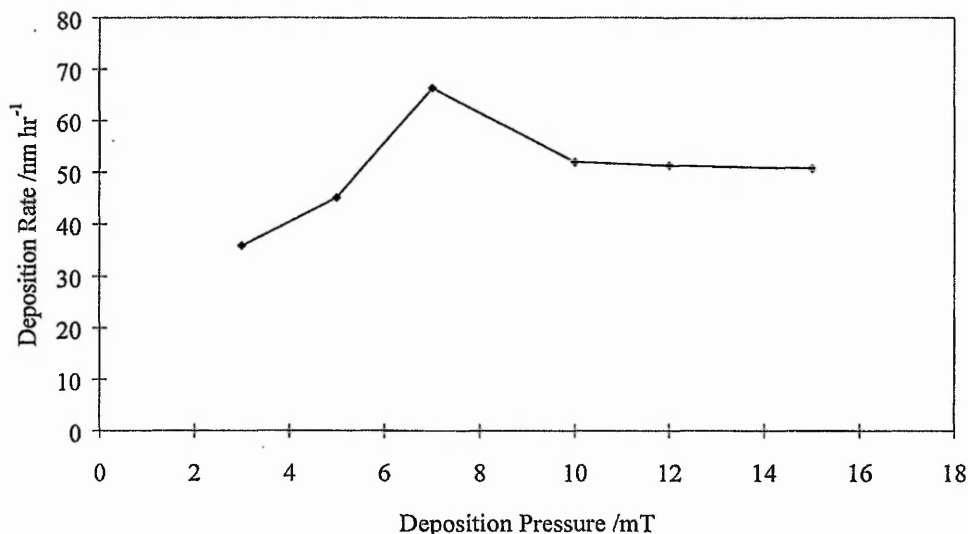
Figure 2.20 Variation in deposition rate with increase in total sputter pressure. Films deposited at 60 °C, 2.18 Wcm^{-2} with a 90/10 ratio of Ar to O$_2$.

2.6.2 - Uniformity and Adhesion

Initially problems were encountered regarding the uniformity of the deposition of the BaTiO$_3$ thin films. The non-uniformity could be visually observed with out the requirement of etching. This was seen as a series of concentric rings on the substrate as in figure 2.21. Each of the different colours represents a different thickness or refractive index. Table 2.3 is a colour chart versus thickness adapted from that for thin films of SiO$_2$[26]. The colour of the films is dependant on the refractive index and for this table only the refractive index was assumed to be constant at n = 1.9. The rings of colour made it simple to observe any improvement in the uniformity of the thin films. The uniformity problem was

solved by adjusting the substrate to target distance. Initially this distance was set at 15 cm, the distance in the LETFEL deposition chamber. On adjustment, the optimum distance for uniformity in the secondary chamber was determined to be 12 cm. Figure 2.22 is a photograph of a 1700Å thick film of $BaTiO_3$ deposited at this distance. The uniformity of the colour across the substrate gives a good indication of the uniformity of the film. Quantitative confirmation of the uniformity was determined utilising the dry etch method detailed in section 2.6.1[B]. The result from a typical set of uniformity measurements is shown in figure 2.23. The thickness uniformity was determined to be $\pm$ 6 % across the substrate. This value is acceptable and was reproducible from substrate to substrate.

A very crude but successful technique was utilised to test the adhesion of the thin films to the substrate. This technique simply involves placing a length of sellotape on the film, applying pressure and removing the tape in one swift action. The adhesion of the thin film is deemed to be satisfactory if none of the film is removed with the sellotape. Without exception all of the $BaTiO_3$ thin films deposited following the optimisation of the heater and electrode configuration exhibited suitable adhesion.
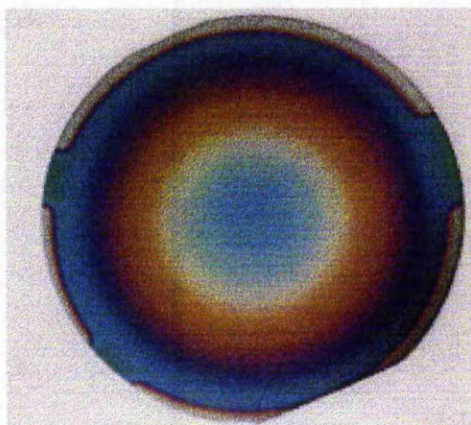
Figure 2.21 Photograph showing concentric colour rings giving a visual indication of the non-uniformity of film thickness.

Colour	SiO_2 Thickness /Å n=1.5	$BaTiO_3$ Thickness /Å n=1.9
Silicon	270	213
Brown	270-530	213-418
Golden Brown	530-730	418-576
Red	730-970	576-765
Deep Blue	970-1000	765-789
1st Order Blue	1000-1200	789-947
Pale Blue	1200-1300	947-1026
Very Pale Blue	1300-1500	1026-1184
Silicon	1500-1600	1184-1262
Light Yellow	1600-1700	1262-1341
Yellow	1700-2000	1341-1578
Orange - Red	2000-2400	1578-1894
1st Order Red	2400-2500	1894-1973
Dark Red	2500-2800	1973-2209
2nd Order Blue	2800-3100	2209-2446
Blue - Green	3100-3300	2446-2603
Light Green	3300-3700	2603-2919
Orange - Yellow	3700-4000	2919-3156
2nd Order Red	4000-4400	3156-3472

Table 2.3 A comparison of the thickness of $BaTiO_3$ and SiO_2 thin films with respect to the observed film colour. Assuming a refractive index of n = 1.9, the multiplication factor was 0.789, determined by $n(SiO_2)/n(BaTiO_3)$.
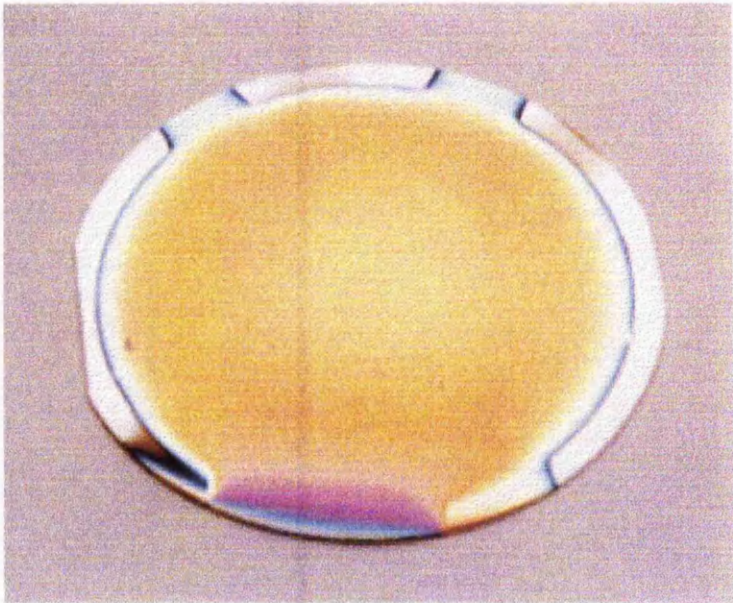
Figure 2.22 A 1700 Å Thick BaTiO$_3$ thin film on Si. The uniformity of the colour across the substrate gives a good indication of the uniformity of the thickness across the substrate.

Position	Thickness /Å
1	1410
2	1465
3	1500
4	1535
5	1590
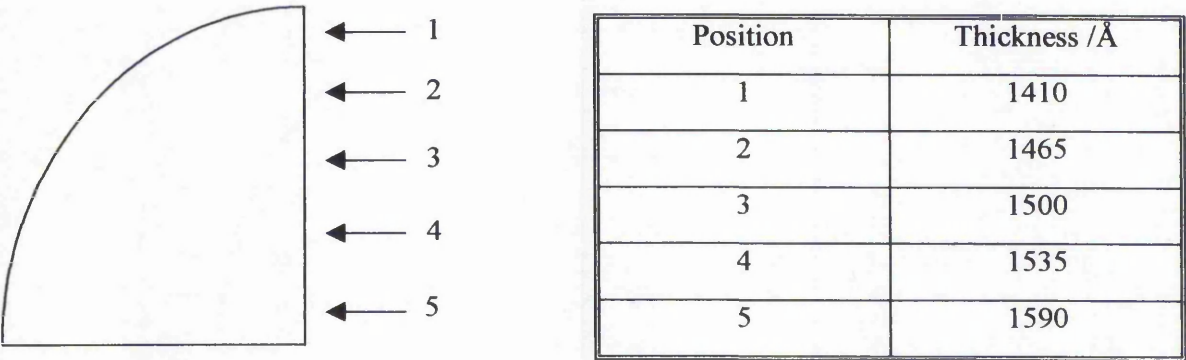
Figure 2.23 Demonstration of the distribution of the uniformity thickness measurements taken across the substrate. Also, a typical set of thickness uniformity results measured from the etched step height, showing a uniformity of ± 6 % across the substrate.

2.6.3 - Dielectric Properties

As shown in figure 2.24, the $Al/BaTiO_3/Si$ structures exhibit the capacitance - voltage (CV) characteristics of an ideal MIS device [26,27]. Regions of majority carrier accumulation, depletion and inversion are observed, allowing the relative dielectric constant to be determined from the accumulation capacitance. The set of ten 3 mm diameter diodes was then analysed for breakdown strength. A Telequipment curve tracer was utilised to determine the value of applied voltage at which electrical breakdown occurred. The electrical breakdown is defined as the applied voltage at which breakdown occurs. The breakdown measurements were carried out on both virgin and post CV characterised diodes. No marked difference in breakdown strength was seen between the two sets of diodes.

Figures 2.25 to 2.27 show the variation in measured ε_r and n due to: the oxygen concentration (figure 2.25), the overall sputter pressure (figure 2.26) and the annealing temperature (figure 2.27) for both the 60 °C and the 200 °C deposition temperatures. Each point on the graph represents the mean value from a set of ten measurements. Tables 2.5 to 2.7 show the mean and standard deviations of all the characteristics exhibited for the devices tested.
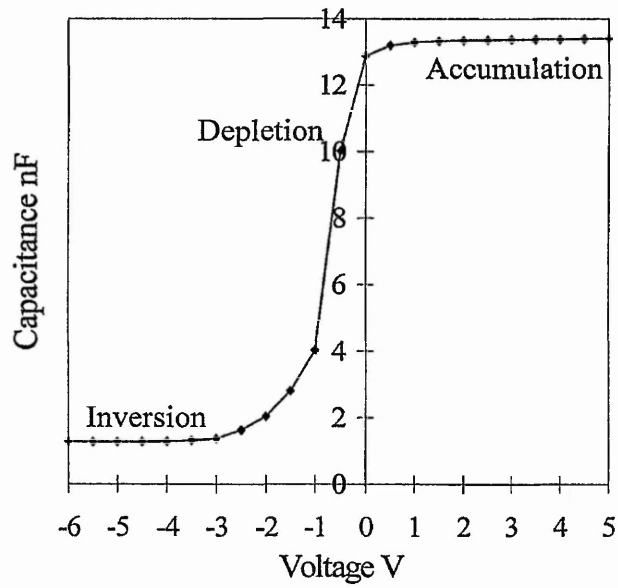
Figure 2.24 A typical capacitance - voltage (C-V) characteristic for a 3 mm diameter Al/BaTiO$_3$/n-Si MIS device with a 125 nm thick BaTiO$_3$ thin film, measured at 1 MHz.

Deposition Parameters T_s = Deposition Temp /°C M_{o2} = O_2 % in Ar Pressure = 5 mT Power = 2.18 Wcm^{-2}	Dielectric Constant ε_r		Refractive Index n		Breakdown Field $E_{b/d}$ $MVcm^{-1}$		Charge Storage Capacity μCcm^{-2}
No Annealing	Mean	σ	Mean	σ	Mean	σ	
T_s = 60 M_{o2} = 0	7.13	0.2	1.89	.02	8.29	0.7	5.23
T_s = 60 M_{o2} = 5	14.14	0.5	1.91	.01	3.36	0.3	4.2
T_s = 60 M_{o2} = 10	14.63	0.6	1.85	.01	4.74	0.4	6.14
T_s = 60 M_{o2} = 15	14.25	0.6	1.93	.03	3.09	0.2	4.03
T_s = 60 M_{o2} = 20	11.33	0.3	1.88	.01	3.62	0.3	3.64
T_s = 60 M_{o2} = 25	11.35	0.4	1.88	.02	3.45	0.4	3.46
T_s = 60 M_{o2} = 30	11.42	0.5	1.88	.02	2.89	0.2	2.92
T_s = 200 M_{o2} = 0	19.47	0.6	1.93	.01	2.5	0.3	4.4
T_s = 200 M_{o2} = 5	18.8	0.7	2.07	.03	3.6	0.2	5.9
T_s = 200 M_{o2} = 10	19.18	0.5	2.07	.03	3.9	0.4	6.7
T_s = 200 M_{o2} = 15	18.9	0.4	2.06	.01	3.6	0.2	6.1
T_s = 200 M_{o2} = 20	22.5	0.8	2.03	.02	4.2	0.4	8.5
T_s = 200 M_{o2} = 25	22.9	0.6	2.05	.02	4.6	0.4	9.3
T_s = 200 M_{o2} = 30	23.51	0.4	2.06	.01	3.7	0.3	7.2
T_s = 200 M_{o2} = 40	16.6	0.2	2.05	.03	3.0	0.2	4.5

Table 2.5 Variation in measured dielectric characteristics of $BaTiO_3$ thin films with a variation in the oxygen concentration in the sputter atmosphere.

Deposition Parameters T_s = Deposition Temp /°C P = Pressure /mT Power = 2.18 Wcm^{-2} Mo_2 = O_2 % in Ar No Annealing		Dielectric Constant ε_r		Refractive Index n		Breakdown Field $E_{b/d}$ $MV\ cm^{-1}$		Charge Storage Capacity CSC $\mu C\ cm^{-2}$
		Mean	σ	Mean	σ	Mean	σ	
T_s = 60 Mo_2 = 10 P = 3		13.96	0.5	1.77	.02	2.95	0.3	3.65
T_s = 60 Mo_2 = 10 P = 5		12.47	0.3	1.98	.05	3.81	0.4	4.21
T_s = 60 Mo_2 = 10 P = 7		15.19	0.6	1.91	.01	5.5	0.1	7.4
T_s = 60 Mo_2 = 10 P = 10		15.31	0.7	1.91	.06	3.45	0.3	4.68
T_s = 60 Mo_2 = 10 P = 12		13.73	0.3	1.89	.03	5.42	0.2	6.58
T_s = 60 Mo_2 = 10 P = 15		14.25	0.2	1.85	.02	4.74	0.4	5.98
T_s = 200 Mo_2 = 30 P = 3		14.5	0.3	2.06	.04	6	0.6	7.7
T_s = 200 Mo_2 = 30 P = 5		16.2	0.6	2.06	.03	6.6	0.5	9.44
T_s = 200 Mo_2 = 30 P = 7		22.9	0.7	2.05	.05	4.6	0.3	9.3
T_s = 200 Mo_2 = 30 P = 10		14.2	0.4	2	.05	5	0.6	6.33
T_s = 200 Mo_2 = 30 P = 12		14.7	0.6	2	.03	5.6	0.5	7.4
T_s = 200 Mo_2 = 30 P = 15		15.5	0.5	2	.01	4.2	0.5	5.7

Table 2.6 Variation in measured dielectric characteristics of $BaTiO_3$ thin films with a variation in total sputter pressure.

Deposition Parameters T_s = Deposition Temp /°C T_a = Annealing Temperature P = 7 mT $Mo2$ = O_2 % in Ar Power = 2.62 Wcm^{-2}		Dielectric Constant ε_r		Refractive Index n		Breakdown Field $E_{b/d}$ $MV\ cm^{-1}$		Charge Storage Capacity CSC $\mu C\ cm^{-2}$
		Mean	σ	Mean	σ	Mean	σ	
T_s = 60 Mo_2 = 10 T_a = 0		13.12	0.2	2.09	.01	4.41	0.5	4.51
T_s = 60 Mo_2 = 10 T_a = 400		15.7	0.4	2.05	.04	4.5	0.3	6.58
T_s = 60 Mo_2 = 10 T_a = 500		17.7	0.3	2.1	.05	3.9	0.2	5.98
T_s = 60 Mo_2 = 10 T_a = 600		15.7	0.5	2.26	.03	5.1	0.6	7.98
T_s = 60 Mo_2 = 10 T_a = 700		23.6	0.6	2.28	.02	3.1	0.1	6.44
T_s = 200 Mo_2 = 30 T_a = 0		22.9	0.3	2.05	.02	4.6	0.2	9.3
T_s = 200 Mo_2 = 30 T_a = 400		23	0.4	2.07	.01	3.7	0.3	7.5
T_s = 200 Mo_2 = 30 T_a = 500		21.1	0.3	2.075	.04	3.3	0.2	6.1
T_s = 200 Mo_2 = 30 T_a = 600		21.9	0.2	2.09	.02	4.1	0.5	8
T_s = 200 Mo_2 = 30 T_a = 700		25.9	0.3	2.1	.03	2.4	0.2	5.5
T_s = 200 Mo_2 = 30 T_a = 800		39	0.8	2.45	.05	1.1	0.6	3.9

Table 2.7 Variation in measured dielectric characteristics of $BaTiO_3$ thin films with a variation in post deposition annealing conditions.

These results are plotted in figures 2.25 to 2.27, both the oxygen concentration and the overall sputter pressure had a measurable effect on the dielectric constant. The optimum conditions with respect to the maximum dielectric constant were 10 % oxygen and 30 % oxygen in argon for the substrate temperatures of 60 °C and 200 °C respectively at a total gas pressure of 7 mT. The deposition power affected only the deposition rate as shown in figure 2.18.

Post deposition annealing caused a pronounced change of dielectric constant. These results are shown in figure 2.27. For both deposition temperatures there is a critical point on the dielectric curve at an annealing temperature of 700 °C. Above this point the dielectric constant increases, with a corresponding increase of the refractive index. However the breakdown strength decreases and hence the charge storage capacity decreases. Analysis utilising a Scanning Electron Microscope (SEM) of the films indicated an increase in surface roughness as the annealing conditions were increased from no annealing to 500 °C and finally to 700 °C, see figures 2.28 to 2.30. This is consistent with previously published results showing that high temperature annealing results in an increase in crystallite size [28]. Similar results were reported for Y_2O_3 thin films [29] deposited by E-beam evaporation, where an increase in annealing temperature from 400 - 700 °C caused a transition from amorphous to a crystalline structure. This resulted in an increase in dielectric constant and a decreased breakdown strength.

2.6.4 - Refractive Index

For lateral transmission of light in LETFEL devices the refractive index of the insulator film needs to be less than that of the phosphor thin film, i.e. n < 2.35 for ZnS:Mn phosphor. Shown in figures 2.25 to 2.27 are the variations of the refractive indices versus O_2 partial concentration, total pressure and annealing temperature. The refractive index is seen to be approximately 10 % higher for the films deposited at 200 °C compared with those grown at the lower temperature, regardless of the deposition parameters. The refractive index of the films deposited at 60 °C increases towards an unacceptable value (i.e. > 2.35) for annealing temperatures above 500 °C. For the films deposited at 200 °C the refractive index stays below 2.35 up to annealing temperatures of 700 °C. Therefore, the optimum annealing temperature for $BaTiO_3$ thin films is identified as 700 °C for a maximum value of dielectric constant and a refractive index at n = 2.1 sufficient to provide internal reflection at the ZnS:Mn/$BaTiO_3$ interface.
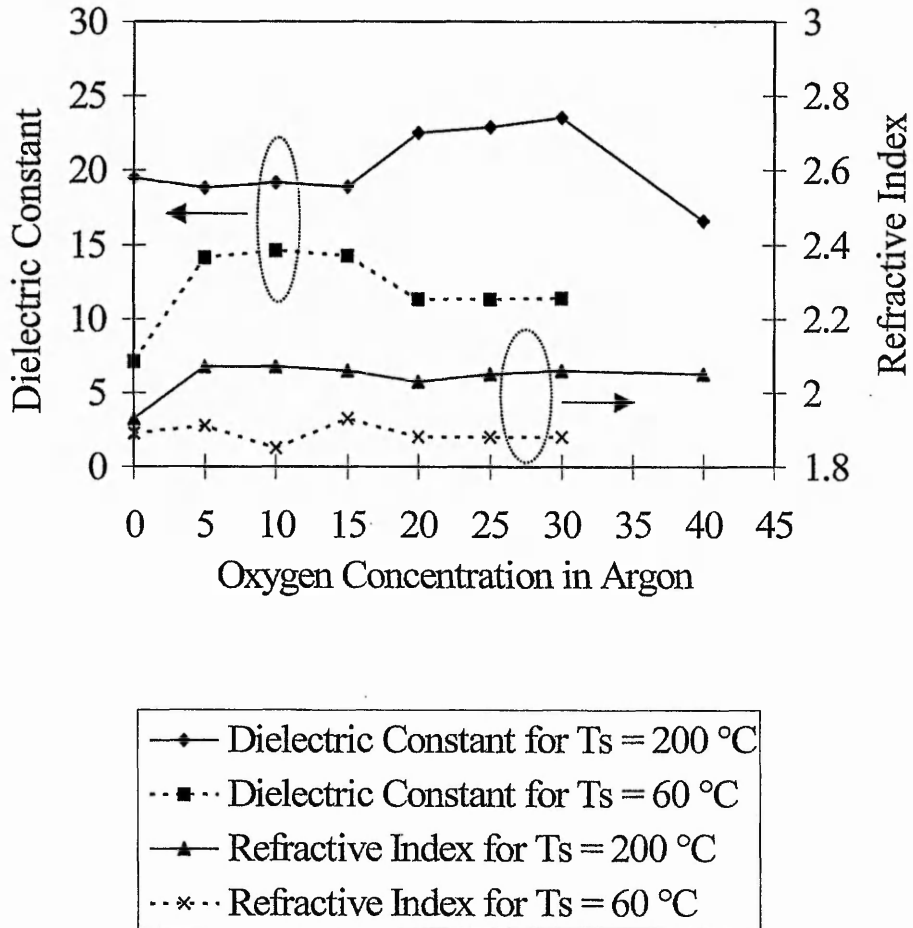
Figure 2.25 Effect of oxygen concentration on the characteristics of BaTiO$_3$ thin films. Deposition occurred at the two temperatures indicated at a power density of 2.18 Wcm^{-2} in a total pressure of 5 mT
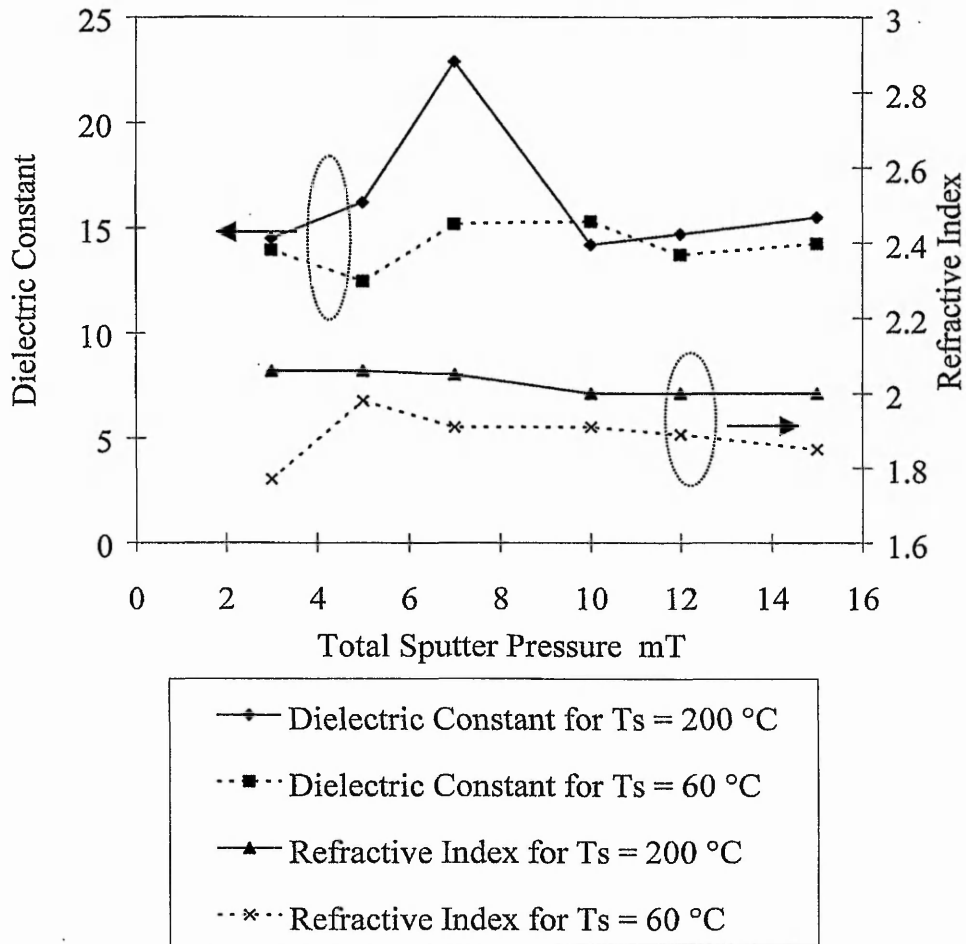
Figure 2.26 Effect of the sputter pressure on the characteristics of $BaTiO_3$ thin films. Deposition occurred at the two temperatures indicated at a power density of 2.18 Wcm^{-2} in 10 % and 30 % oxygen for Ts = 60 and 200°C respectively.
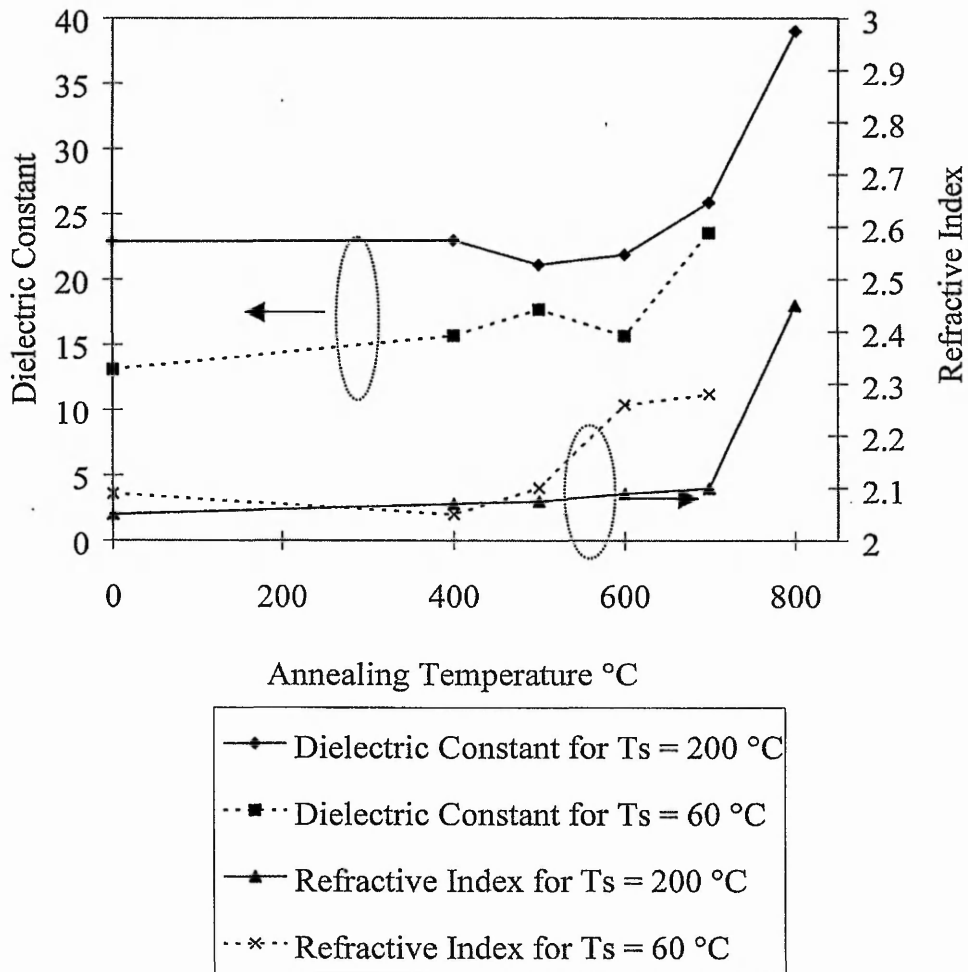
Figure 2.27 Effect of annealing temperature on the characteristics of BaTiO$_3$ thin films. Deposition occurred at the two temperatures indicated at a power density of 2.62 Wcm^{-2} in 10 % and 30 % oxygen for Ts = 60 and 200°C respectively at a total pressure of 7 mT.

2.6.5 - Breakdown Strength and Charge Storage Capacity

The breakdown strength of the thin films was determined to be greater than the required minimum of 3 $MVcm^{-1}$ for all of the deposition and post-deposition conditions up to the 700 °C annealing temperature. At 700 °C, the breakdown strength dropped to 3 $MV\ cm^{-1}$ and 2.4 $MV\ cm^{-1}$ for deposition at 60 °C and 200 °C respectively. At 800 °C the breakdown strength decreased to 1.1 $MVcm^{-1}$ for deposition at 200 °C. Such decrease corresponds to an increase in surface roughness, shown in figures 2.28 to 2.31. Stated previously is the necessity for the value of the charge storage capacitance of the films to exceed 3 $\mu C\ cm^{-2}$ for LETFEL device use. For all of the deposition and post-deposition conditions this value was only once less than 3 $\mu C\ cm^{-2}$. This film was deposited at 60 °C in a 30 % O_2 in Ar atmosphere. Disregarding this film, all of the films deposited are suitable for use in LETFEL devices although it is preferable to utilise films with high breakdown strength for greater device protection.
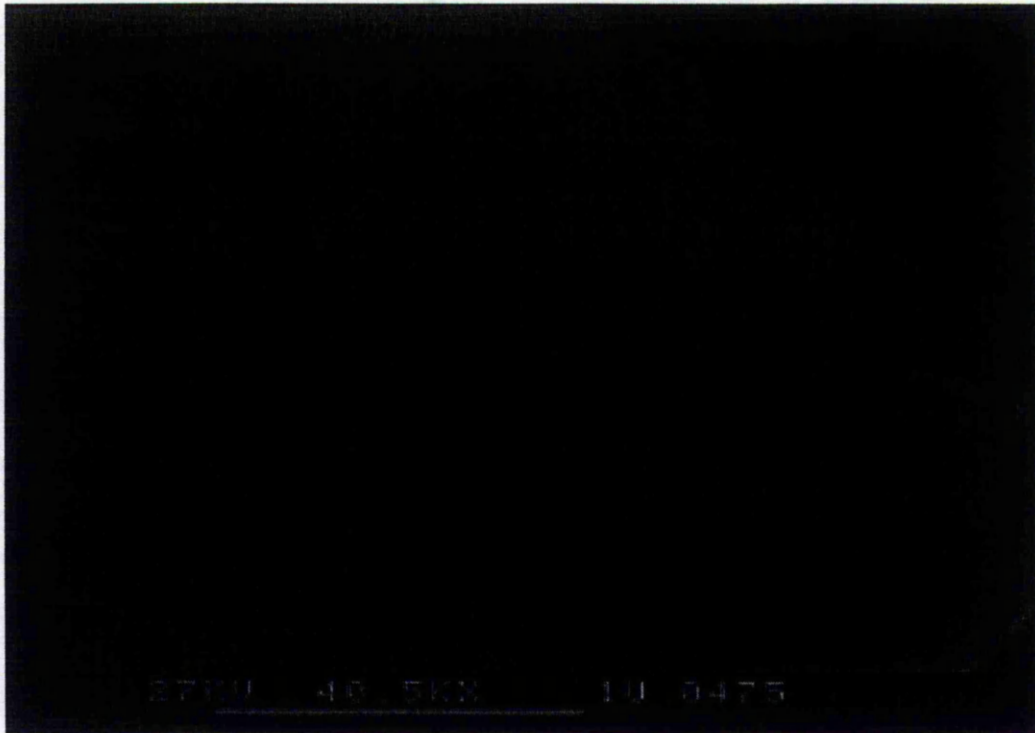
Figure 2.28 An SEM photograph of a BaTiO$_3$ thin film deposited at 200 °C with no post deposition annealing

Figure 2.29 An SEM photograph of a BaTiO$_3$ thin film deposited at 200 °C and annealed for 1 hour at 500 °C.
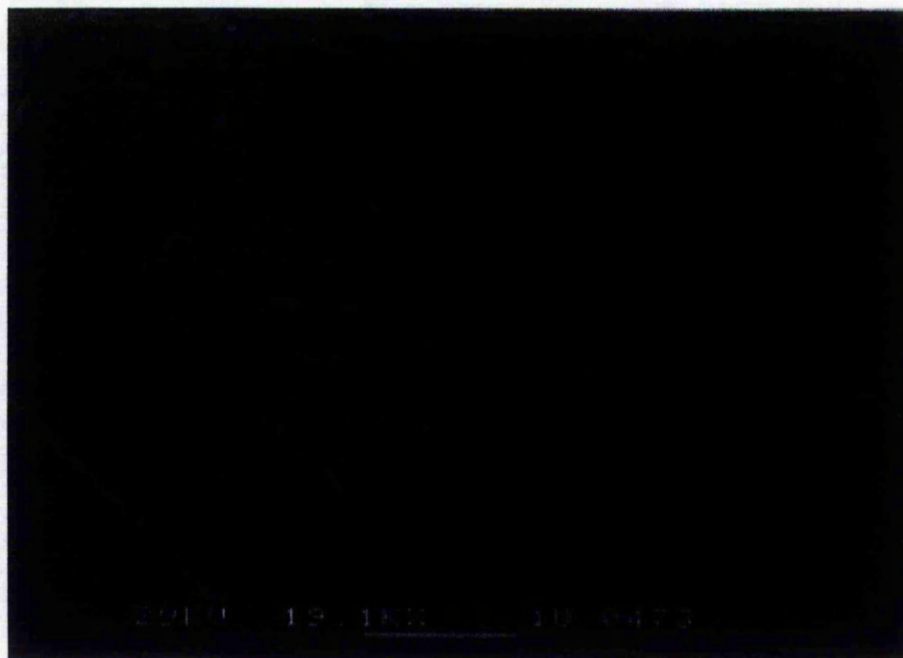
Figure 2.30 An SEM photograph of a BaTiO$_3$ thin film deposited at 200 °C and annealed for 1 hour at 700 °C.

2.7 - Conclusions

Demonstrated here for the first time is the optimisation of the dielectric constant and refractive index for BaTiO$_3$ thin films deposited by RF magnetron sputtering, specifically for use in LETFEL devices. Variation of the deposition and post-deposition annealing conditions have yielded the optimum conditions. Demonstrated has been that under these optimum conditions, the resultant thin films of BaTiO$_3$ are viable for use as the insulator layer in a LETFEL device specifically designed for lateral transmission of light. Furthermore, BaTiO$_3$ thin films deposited via the optimised process provide improved characteristics as compared with those of the Y$_2$O$_3$ thin films, which are utilised in current LETFEL

devices. Specifically, the increased dielectric constant of $BaTiO_3$ over Y_2O_3 enables the use of a thicker insulator in the LETFEL device structure working at the same drive voltage. Therefore, $BaTiO_3$ thin films have the potential for providing improved lateral emission. The study has shown that the optimum growth conditions for $BaTiO_3$ thin films deposited by RF magnetron sputtering are a substrate temperature of 200 °C in an atmosphere of 30 % oxygen in argon at 7 mT at 2.62 Wcm^{-2} with a post-deposition anneal at 700 °C for 1 hour. These deposition conditions produce a film with a dielectric constant of 26, a refractive index of 2.1, a breakdown strength of 2.5 MV cm^{-1} and a charge storage capacity of 5.5 $\mu C\ cm^{-2}$.

This has demonstrated that under the above conditions $BaTiO_3$ thin films are suitable, in principle, for use as insulators in LETFEL devices. The next stage is to integrate these deposition conditions into the full device fabrication procedure.

2.8 References

1   D. M. Alt, D. B. Dove and W. E. Howard, *J. Appl. Phys.*, 53 1982 p5186.

2   W.M. Cranton PhD. Thesis University of Bradford (1995).

3   N.M. Abuhadba and C.R. Aita; *Jnl. Appl. Phys.* **71** (1992) p3045.

4   A. Mansingh and C.V.R. Vasanta Kumar; *Jnl. Mat. Sci. Lett.*, **7** (1988)
        p1104.

5   M. Wöhlecke, V. Marrello and A.Onton; *Jnl. Appl. Phys.* **48** (4) (1977)
        p1748.

6   H. Venghaus, D. Theis, H. Oppolzer and S. Schild; *Jnl. Appl. Phys.* **53** (6)
        (1982) p4146.

7   K. Screenivas, A. Mansingh and M. Sayer; *Jnl. Appl. Phys.* **62** (11) (1987)
        p4475.

8   I.H. Pratt and S. Firestone; *Jnl. Vac. Sci. & Tech.* **8** (1) (1971) p256.

9   C.A.T. Salama and E. Siciunas; *Jnl. Vac. Sci. & Tech.* **9** (1) (1971)p91.

10   A. Yamanashi, K. Tanaka, T. Nagatomo and O. Omoto; *Jap. Jnl. Appl.
        Phys.* Part 1 **9B** (1993) p4179.

11   T.L. Rose, E.M. Kellier, A.N. Scoville and S.E. Stone; *Jnl. Appl. Phys.* **55**
        (10) (1984)   p3706.

12   J. L. Vossen and W. Kern; (1978) *Thin Film Processes* (London:
        Academic Press)

13   L. A. Wills, B.W. Wessels, D. S. Richeson and T. J. Marks; *Appl. Phys.
        Letts.* 59 (1996) p3547

14   M. N. Kamalasanan, N. Deepak Kumar and Subhas Chandra; *Jnl. Appl. Phys.* **74** (9) (1993) p5679

15   Z. Q. Shi, Q. X. Jia and W. A. Anderson; *J. Vac. Sci. Technol.*, A 10 4 (1992) p733.

16   H. Venghaus, D. Theis, H. Oppolzer and S. Schild; *Jnl. Appl. Phys.* **53** (6) (1982) p4146.

17   H. Nanto, T. Minami, S. Murakami and S. Takata; *Thin Solid Films,* 164 (1988) p363

18   J. B. Sykes;, *The Concise Oxford Dictionary,* Seventh Edition (1984) p1029

19   R. Waits; *J. Vac. Sci. and Tech.,* **15** 2 (1978) p179-187

20   Private Communication P. Stonestreet. UHV Design.

21   J. L. Vossen; *Jnl. Vac. Sci. and Tech.* **8** (5) (1971) pS12.

22   C.B. Thomas, R. Stevens, W. M. Cranton, I. P. McClean, M. R. Craven and A. H. Abdullah; *SID* (1995) p887

23   W. M. Cranton, D. M. Spink, R. Stevens and C. B. Thomas; *Thin Solid Films*, 226 (1993) p156.

24   D. Sands; *Ph.D. Thesis*, University of Bradford, (1987).

25   S. M. Sze; *Physics of Semiconductor Devices*, (Wiley, New York, 2nd edn.) (1981), p393.

26   E. H. Nicollian and J. R. Brews; *MOS Physics and Technology*, (Wiley, New York) (1982).

27   N-Y. Lee, T. Sekine, Y. Ito and K. Uchino; *Jpn. J. Appl. Phys.*, 33 (1994) p1484.

28   A. C. Rastogi and R. N. Sharma; *J. Appl. Phys.*, 71 10 (1992) p5041.

Chapter 3 Fabrication and Characterisation Of BaTiO₃ Based LETFEL Test Structures For Improved Efficiency

3.1 Introduction

Following the characterisation of BaTiO₃ thin films, as detailed in chapter 2, it was determined that when deposition and annealing occurred utilising the optimum conditions, these films exhibited suitable characteristics for use as insulators in LETFEL devices. The optimum conditions, as summarised in table 3.1, produce films with:- a high dielectric constant, $\varepsilon_r = 26$, a high breakdown field, $E_{bd} = 2.4$ MV/cm, a refractive index of n = 2.1 and a charge storage capacity, C.S.C = 5.5 μC/cm². Films deposited using the conditions in table 3.1 have been utilised for the fabrication of LETFEL device structures as shown in figure 3.1. This chapter deals with the fabrication and characterisation of these BaTiO₃ based LETFEL devices.

Material	Ts - Substrate Temp °C	Power Density Wcm⁻²	Sputter Pressure mT	% Oxygen in Argon	Deposition Rate nm/hr	Ta - Annealing Temp °C
BaTiO₃	200	2.62	7	30	97	700

Table 3.1. Summary of optimum deposition and annealing conditions for BaTiO₃ thin films.

Top Al Electrode

Insulator 2 — C_{Ins1}

Phosphor — C_{Phos1}

Insulator 1 — C_{Ins2}

Silicon
Substrate

Bottom Al
Electrode
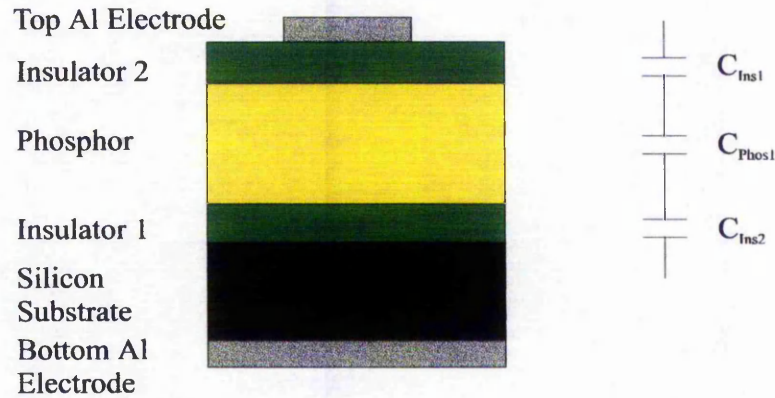
Figure 3.1 Basic LETFEL test device structure with its equivalent circuit. This equivalent circuit is only valid for an applied voltage less than the threshold voltage of the device.

Changing the insulator material in a LETFEL device is not a trivial operation. Ideally an increase in performance will be obtained without detrimentally affecting any of the other properties of the device. An increase in performance of the device can be defined as either an improvement in luminance or a decrease in either the drive or switching voltages. Predicted in section 1.5 is that an increase in insulator thickness in the LETFEL device will lead to an increase in the optical confinement of light in the structure. Hence, an improvement in luminance from laterally emitted light would be expected. There are of course many other factors that could potentially affect the performance of a LETFEL device by the replacement of the insulator material. A summary of these other effects is given in section 3.2.

Many or all of the effects detailed in section 3.2 may contribute to a change in the luminance and performance of a LETFEL device. Therefore, a full investigation

into the replacement of Y_2O_3 thin film insulators by $BaTiO_3$ thin film insulators in the LETFEL device stack is required.

In summary there are four questions to be addressed by this chapter.

1) Are $BaTiO_3$ thin films suitable for use as the insulator material in LETFEL devices ?

2) Which is the optimum combination of insulator thin films ?

That is, which is optimum, $BaTiO_3$ thin films as both insulator one and two, or Y_2O_3 as one insulator and $BaTiO_3$ the other.

3) What is the effect of varying the insulator thickness on the device performance ?

4) Is there any relationship between the theory of a step index waveguide and the LETFEL device structure?

Finally, a first order geometric approximation for the propagation of light through the LETFEL device structure has been developed from the theory of a step index waveguide. The attenuation coefficient and luminance for all the devices have been measured. These results have been compared to the predicted increase in light confinement theoretically achieved by increasing the insulator thickness.

Therefore, detailed in this chapter is the full fabrication and characterisation of a series of LETFEL devices to satisfy the above unknowns.

3.2. Possible Effects on Changing the Insulator in a LETFEL Device

3.2.1 Effect on Threshold and Drive Voltage

At an applied voltage below the threshold voltage the thin film stack in a LETFEL device acts as three capacitors in series. Figure 3.1 shows the thin film stack and a simple equivalent circuit for the device at a voltage below threshold voltage. The total capacitance of the device structure is given by: -

$$\frac{1}{C_T} = \frac{1}{C_{Ins1}} + \frac{1}{C_{Phos}} + \frac{1}{C_{Ins2}} \qquad \text{Eq. 3.1}$$

Where

$$C = \frac{\varepsilon_o \times \varepsilon_r \times A}{d} \qquad \text{Eq. 3.2}$$

and ε_o is the permittivity of free space (8.854×10^{-12} Fm^{-1}), ε_r is the relative dielectric constant of the material, A is the area of the device and d is the thickness of the material.

It is proposed to replace the current Y_2O_3 insulator thin films with those of $BaTiO_3$. Regarding the total capacitance of the device, Y_2O_3 has a dielectric constant of 16[1] compared to that of 26 for $BaTiO_3$. Hence, by replacing the Y_2O_3 thin films directly with the same thickness of $BaTiO_3$ thin films, an increase in the total capacitance of the device will be seen. This increase in capacitance will lead to a reduction in both the threshold and drive voltages of the device. The reduction of these voltages is beneficial with respect to the overall display system.

It means that lower voltage drive electronics are required and hence a reduction in the overall cost of the display module will be achieved. However, of greater interest is the potential for enhanced luminescence via thickening of the insulator layers. Hence, the second part of this chapter deals with the increase in insulator layer thickness. An increase in the thickness of the insulator will lead to an increase in the threshold voltage, but since $\varepsilon_{BaTiO_3} > \varepsilon_{Y_2O_3}$, the devices can be engineered to operate at the same drive voltage. A limit for the threshold voltage, Vth, of the new devices of 200 Volts ground to peak has been used to match the current $Y_2O_3/ZnS:Mn/Y_2O_3$ device[2]. Therefore a trade off is required between the threshold voltage of the device and it's maximum luminance.

It is possible, using Eq. 3.3[3], to determine the field dropped across each layer in the device structure at the threshold voltage

$$E_z = \frac{\varepsilon_I}{d_I \varepsilon_z} Vth \left(1 + \frac{d_z \varepsilon_I}{d_I \varepsilon_z} \right)^{-1} \qquad \text{Eq. 3.3a}$$

$$E_I = \frac{\varepsilon_z}{d_z \varepsilon_I} Vth \left(1 + \frac{d_I \varepsilon_z}{d_z \varepsilon_I} \right)^{-1} \qquad \text{Eq. 3.3b}$$

$$Vth = E_z \left(1 + \frac{d_z \varepsilon_I}{d_I \varepsilon_z} \right) \left(\left(\frac{\varepsilon_I}{d_I \varepsilon_z} \right)^{-1} \right) \qquad \text{Eq. 3.3c}$$

Where E_z, E_I are the field across the phosphor and the insulator respectively, d_z and d_I are the thickness of the phosphor and insulator films respectively, ε_z and ε_I are the relative dielectric constants of the phosphor and the insulator respectively and Vth is the threshold voltage of the device.

In the standard Y_2O_3 (300 nm)/ZnS:Mn (800 nm)/Y_2O_3 (300 nm) device the threshold voltage, Vth, is 200 V. Therefore using equation 3.3a the field dropped across the ZnS:Mn layer is 2.11 MVcm⁻¹.

$$Ez = \left(\frac{16}{300^{-9} \times 8} \right) \times 200 \times \left(1 + \frac{800^{-9} \times 16}{300^{-9} \times 8} \right)^{-1}$$

$$= 2.11 \text{ MVcm}^{-1}$$

This is the field required across the ZnS:Mn for the onset of emission. Therefore with this knowledge and the knowledge of both the thickness and the relative dielectric constant of the insulator film it is possible to estimate the threshold voltage of a LETFEL device utilising equation 3.3c.

3.2.2 Effect On Attenuation

As light propagates through the material a decay in the intensity of the light can be measured. The losses suffered, causing the decay of luminance, in the material may be due to absorption or scattering. If a single attenuation coefficient for the material is assumed, the relative luminance at any point can be calculated using equation 3.4[4].

$$L = L_0 \exp^{-\alpha x} \qquad \text{Eq. 3.4}$$

Where L_0 is the initial intensity, x is the distance travelled and α is the attenuation coefficient (m⁻¹).

In the case of a LETFEL device, assuming that the structure behaves as a step index waveguide, it can be shown that a certain amount of energy will propagate in the insulator due to evanescent outcoupling from the guiding layer, figure 3.2 for example. Therefore a change in the material of the cladding may have a pronounced effect on the attenuation coefficient of the device structure.
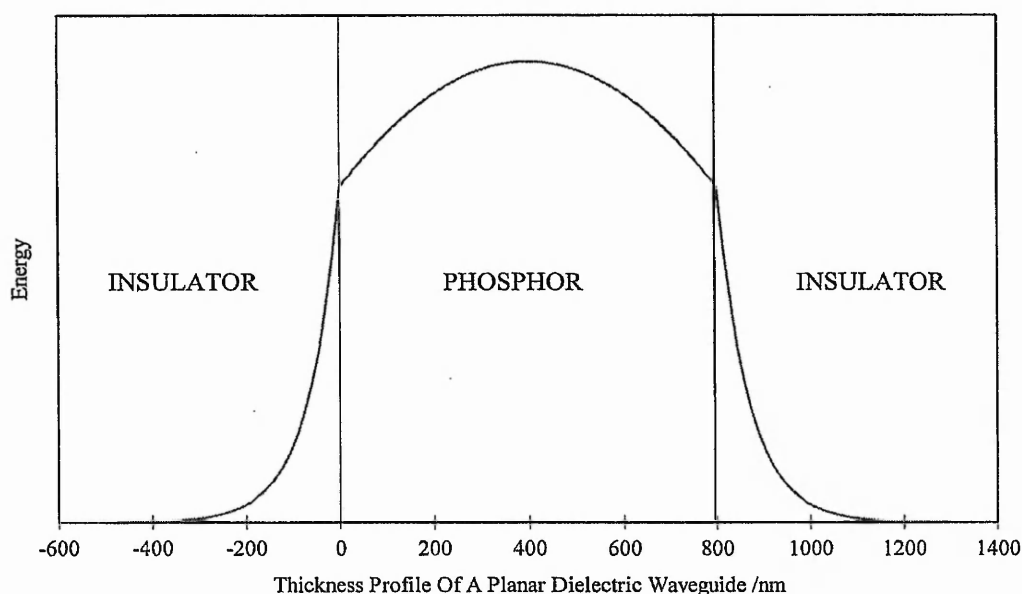
Figure 3.2 Propagation of a single mode of light through a planar dielectric waveguide.

3.2.3 Effect of Changing the Interface

The interface between the phosphor and the insulator in a LETFEL device is crucial to the performance of the device. Firstly, it is from this interface that the electrons originate. These electrons are accelerated under the applied high field and impact excite the Mn^{2+} ions[5]. It is the radiative decay of a proportion of these excited ions which produces the luminescence. Therefore, if there are more

electrons at the interface, with the correct energy, there is a higher probability of the Mn^{2+} ions being excited and hence a greater chance of luminescence. Secondly, the physical roughness of the interface will effect the amount of light lost due to scattering at this interface. By replacing the insulator material a change in this interface may be produced. If the replacement insulator has a higher density of interface states there could be an increase in the number of electrons and hence an increased probability of the electrons being injected into the phosphor layer. Hence, the probability of the Mn^{2+} ions being excited may increase. This in turn would be expected to lead to an increase in the observed luminance. Finally, if the roughness of the interface is changed a change in the scattering will be observed.

3.2.4 Effect Of the Change in Refractive Index Profile

It has been reported by Marcuse[6] that as the difference in refractive indices between the core and cladding in a thin film waveguide decreases, the loss of light due to scattering at the interface decreases. The refractive indices of ZnS:Mn, Y$_2$O$_3$ and BaTiO$_3$ are n = 2.35, 1.9 and 2.1 respectively[3,7]. By the replacement of Y$_2$O$_3$ with BaTiO$_3$ the difference in refractive indices between the core and the cladding does decrease, therefore a decrease in scattering would be expected. This in turn could lead to an increase in luminance.

3.2.5 Effect of a Change in The Crystallinity of the Insulator

Finally, the crystallinity of the ZnS:Mn thin film is known to affect the luminance of the TFEL device[8]. An increase in crystallinity of the ZnS:Mn has been shown to increase the luminance from the device[9]. It has also been shown that the crystallinity of the ZnS:Mn is dependent on the crystallinity of insulator 1[10]. Therefore any difference in crystallinity of insulator 1 in figure 3.1 could affect the luminance of the device.

3.3 Development of a First Order Geometric Approximation for the Propagation of Light in a LETFEL Device

W. M. Cranton[3], amongst others[11], has proposed that the LETFEL device structure is that of a leaky step index waveguide. To date no expansion of the theory of a step index waveguide or comparison of that theory to experimental measurements has been reported. In reality, since the insulator thickness is typically ~ 300 nm, the (insulator) cladding thickness is smaller than the wavelength of the emitted light (λ_0 = 585 nm for ZnS:Mn) and energy may be lost via evanescent coupling out of the waveguide. Therefore any increase in cladding thickness should yield an increase in the optical confinement of the light in the waveguide structure. This increase should in turn lead to a decrease in the attenuation coefficient for laterally transmitted light and hence an increase in luminance would be observed.

As a means to examine this effect, a simple one dimensional model has been developed to compare with experimental data. The theory of a step index waveguide is well known. The reader is directed towards Optoelectronics :- An Introduction by Wilson and Hawkes [12] for a full explanation. In summary, there are five main stages of the development of this model:-

1) Determination of the critical angles for total internal reflection. This needs to be calculated for both the Y_2O_3/ZnS:Mn and the $BaTiO_3$/ZnS:Mn interfaces.

2) Determination of the number of potential modes and the relative mode angles supported by each of the device structures with the two different cladding materials.

3) Determination of the decay of the evanescent wave into the two cladding materials.

4) Determination of the profile of the energy propagating through the device for all of the device configurations.

5) Determination of the amount of energy propagating outside the device structure for different thickness cladding layers.

3.3.1 Determination of the Critical Angles at each Interface

At a boundary of two dielectric materials, shown in figure 3.3, when $n_1 > n_2$, it is possible to have total internal reflection when $\theta_i > \theta_c$,[13]

where

$$\theta c = \sin^{-1}\left(\frac{n_2}{n_1}\right)$$ Eq. 3.5

Where θ_c is the critical angle and n_1 and n_2 are the refractive indices of the two materials.
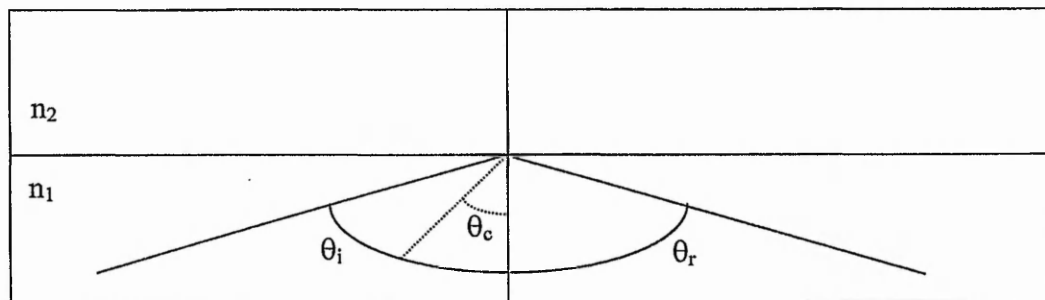
Figure 3.3 Behaviour of incident light ray at the boundary of two dielectric interfaces with refractive indices n_1 and n_2. θ_c = critical angle, θ_i, and θ_r are the angles of incidence and reflection respectively.

Table 3.2 gives the critical angles for the two interfaces under investigation here.

Interface	n_1	n_2	θ_c
Y$_2$O$_3$/ZnS:Mn	2.35	1.91	54.37
BaTiO$_3$/ZnS:Mn	2.35	2.10	63.33

Table 3.2 Summary of critical angles for the two different cladding materials used in a LETFEL device

3.3.2 Determination of the number of modes supported and their associated interface angles.

In figure 3.3 the light is shown as a single ray. In reality, the light propagates along the waveguide as a wave front. This wave front is the result of many single rays propagating at the same angle but slightly offset from one another. With regard to this wave front all of the single rays at a cross section must be in phase. For the wave front to propagate the phase shifts experienced at each reflection must be taken into account. Hence, for a mode of light to propagate in a step index dielectric waveguide it must satisfy the following condition[12]:-

$$\pi \times m = \frac{2 \times \pi \times d \times n_1 \times \cos(\theta)}{\lambda} - \phi \qquad \text{Eq. 3.6}$$

Where d is the thickness of the core, n_1 is the refractive index of the core, m is an integer, θ is the angle of incidence, λ is the wavelength of the light (585 nm) and ϕ is the phase shift.

The simplest method of solving equation 3.6 is graphically by plotting equations 3.7 and 3.8 for $\theta = \theta_c$ to 90°[12].

$$f(y) = \frac{2 \times d \times n_1 \times \cos(\theta)}{\lambda} \qquad \text{Eq. 3.7}$$

and

$$f(y) = \pi \times m + \phi \qquad \text{Eq. 3.8}$$

where

$$\phi(\theta) = 2 \times \psi \qquad \text{Eq. 3.9}$$

and

$$\tan(\psi) = \frac{\left[\sin(\theta^2) - \left(\frac{n_2}{n_1}\right)^2\right]^{\frac{1}{2}}}{\cos(\theta)}$$

Eq. 3.10

Where d is the thickness of the core, n_1 and n_2 are the refractive indices of the core and cladding respectively, λ is the wavelength of the light (585 nm for ZnS:Mn) and m is the mode number

From equations 3.9 and 3.10, equation 3.8 becomes equation 3.11. Therefore the two equations plotted are equation 3.7 and 3.11.

$$f(\theta) = \left[\frac{\tan^{-1}\left[\frac{\left[\sin(\theta)^2 - \left(\frac{n_2}{n_1}\right)^2\right]^{\frac{1}{2}}}{\cos(\theta)}\right]}{2}\right] + \pi \times m$$

Eq. 3.11

Where the plots of equations 3.7 and 3.11 intersect both the mode number and it's associated angle can be determined. Figures 3.4 and 3.5 show the solutions for these equations for the Y$_2$O$_3$ and BaTiO$_3$ clad devices respectively. Table 3.3 gives the number of theoretical modes and their respective angles for the modes potentially supported in each waveguide with a ZnS:Mn core thickness of 800 nm.

Mode Number	Mode Angles (BaTiO$_3$)	Mode Angles (Y$_2$O$_3$)
0	87.85	87.85
1	79.4	79.3
2	70.75	70.4
3		61.05

Table 3.3 The number and angles of the modes potentially supported by a LETFEL device with a 800 nm core and the different cladding materials

From table 3.3 it can be seen that a Y$_2$O$_3$ clad device with a 800 nm ZnS:Mn core will potentially support 4 modes of energy. The equivalent BaTiO$_3$ device structure will only potentially support the first three modes due to the higher value of θ_c at for the BaTiO$_3$/ZnS:Mn interface.
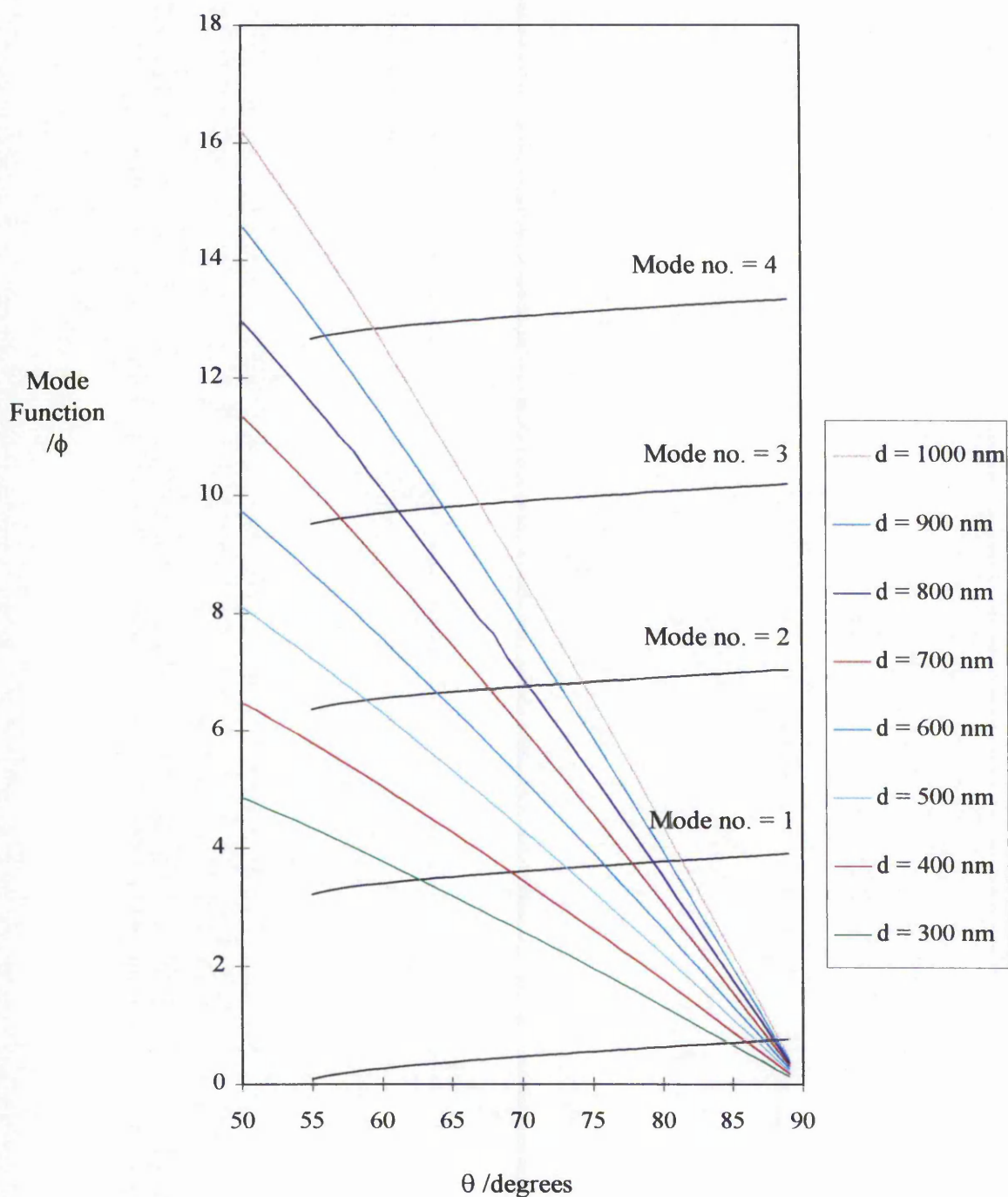
Figure 3.4 Determination of the number of modes potentially supported in a Y$_2$O$_3$ clad device where d is the thickness of the ZnS:Mn core /nm.
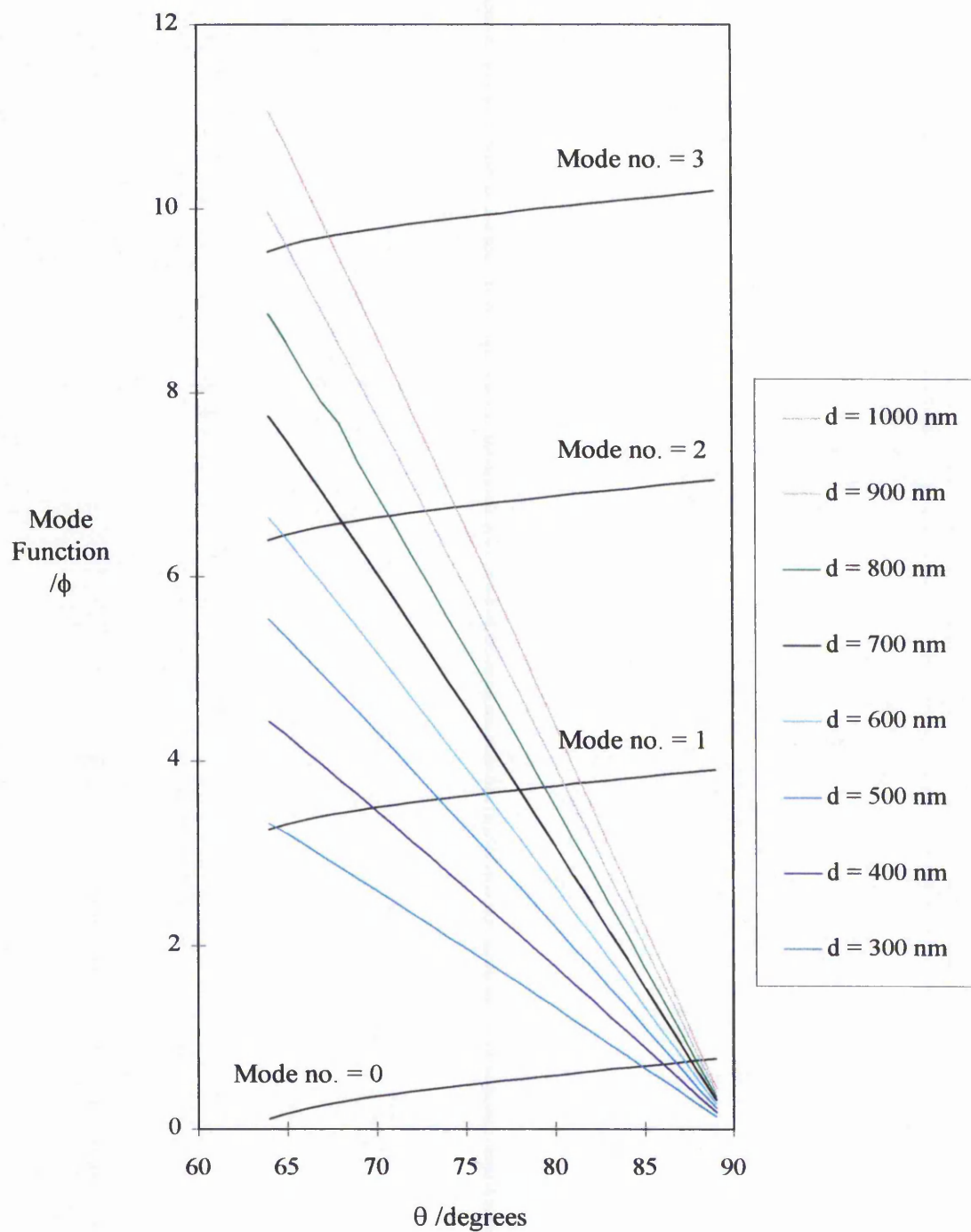
Figure 3.5 Determination of the number of modes potentially supported in a BaTiO$_3$ clad device where d is the thickness of the ZnS:Mn core /nm.

3.3.3 Decay of the evanescent wave into the cladding of the device for each mode.

When $\theta_i > \theta_c$ all of the incident energy in the wave front is reflected due to total internal reflection. Even so a disturbance is still experienced in the second medium. The energy propagating in the cladding is known as the evanescent wave. Although the amplitude of the evanescent wave decays rapidly in the cladding region, in an ideal waveguide the cladding region extends infinitely from the boundary so no energy is lost. In the case of the LETFEL device the cladding thickness, typically 300 nm, is less than the wavelength of the emitted light, 585 nm for ZnS:Mn. Therefore, light will be lost as the evanescent wave will extend outside of the cladding layers, known as evanescent out coupling. The next stage is to determine the decay of the evanescent wave into the cladding for each mode using equation 3.12[12]. This will enable an insight to the increase in light confinement attained with an increase in cladding thickness.

$$f(y) = \exp\left[\left(\frac{-2 \times \pi \times n_2}{\lambda}\right) \times \left[\left(\frac{n_1}{n_2}\right)^2 \times \sin(\theta)^2 - 1\right]^{\frac{1}{2}} \times y\right] \qquad \text{Eq. 3.12}$$

Where λ = the wavelength of the light (585 nm for ZnS:Mn), n_1 and n_2 are the refractive indices of the core and cladding respectively, θ is the mode angle and y is the distance into the cladding region.

Figures 3.6 and 3.7 show the decay of the evanescent wave as determined by plotting $f(y)$, equation 3.12, into the cladding region for each of the modes supported in both the Y₂O₃ and BaTiO₃ clad devices respectively. Also indicated is the amount of energy travelling outside the waveguide for a standard 300 nm

clad device. This energy may be absorbed by either the Si substrate or the Al top electrode. It can be seen that as the cladding thickness is increased the amount of energy propagating in the waveguide is increased.
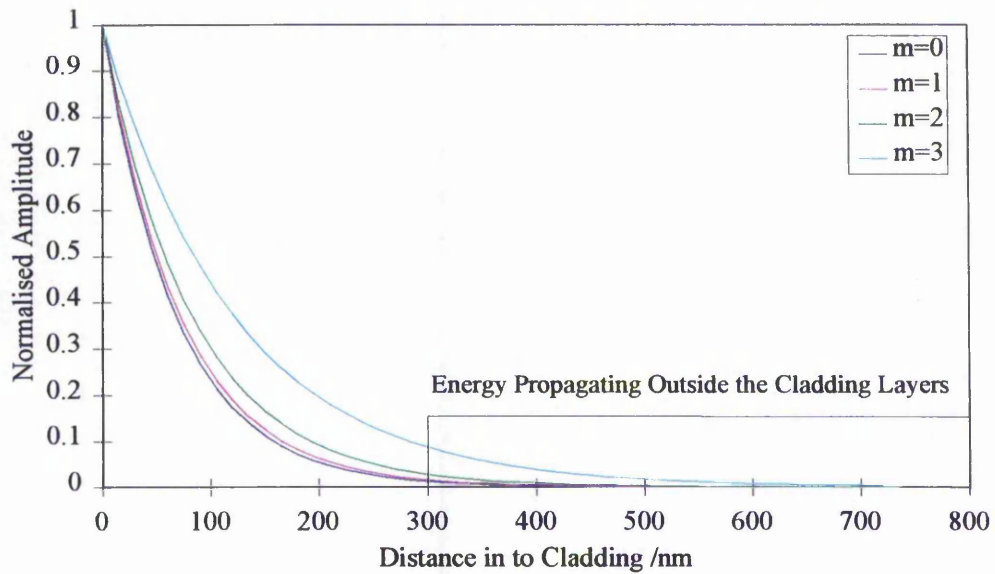
Figure 3.6 Decay of the evanescent wave into the Y_2O_3 cladding for each supported mode. Where m is the mode number.
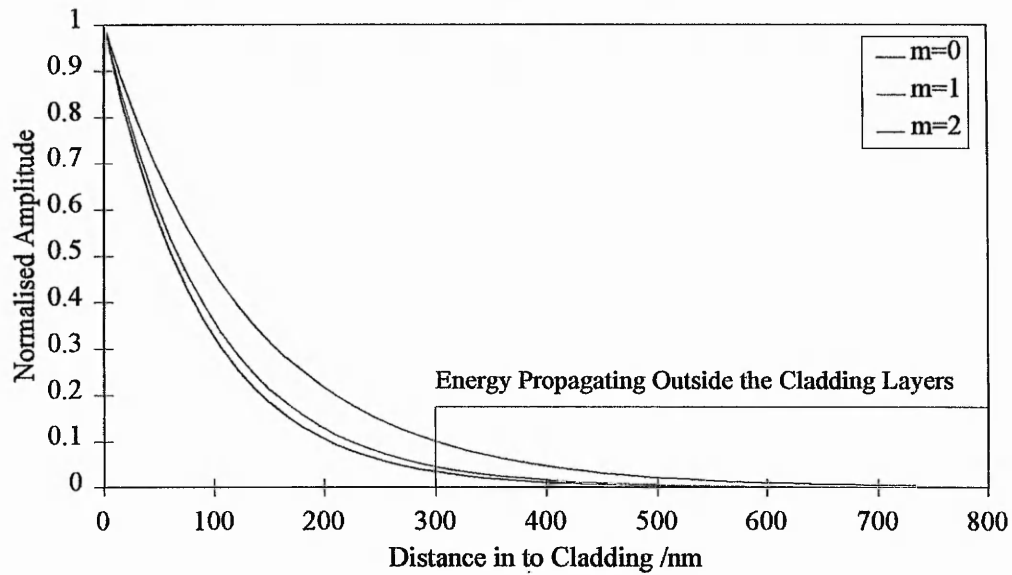
Figure 3.7 Decay of the evanescent wave into the BaTiO$_3$ cladding for each supported mode. Where m is the mode number.

3.3.4 Determination of the amount of energy propagating in each mode

In section 3.3.2. it was shown that the light in a step index waveguide propagates as a series of wave fronts. To gain an insight into the theoretical improvement by increasing the light confinement it is necessary to determine the energy propagating in each mode in each layer of the waveguide. Using equation 3.13[12] it is possible to determine the relative energy amplitude, and hence the relative energy profiles, of each mode propagating through the device structure. It has been assumed that the initial energy has a value of 1.

$$E = 2 \times E_0 \times \cos\left[\left(\frac{\pi \times m}{2}\right) - \frac{y}{d} \times \left(\pi \times m + \varphi\right)\right] \qquad \text{Eq. 3.13}$$

Where m is the mode number, y is the distance into the cladding, d is the thickness of the core, Eo is the initial energy intensity and ϕ is the phase shift.

Figures 3.8 and 3.9 show the energy profile in each device structure. These figures have been determined using equation 3.13 for the profile of the energy in the core region. For the profile in the cladding region, the energy at the interface has been taken and then multiplied by the evanescent decay functions for each mode shown in figures 3.6 and 3.7 for both the Y_2O_3 and $BaTiO_3$ clad devices respectively. The total amount of energy in each of the layers in the device structure can be calculated by the integration of the energy amplitude. Table 3.4 details this energy breakdown. Table 3.5 shows the increase in light confinement obtained when the thickness of the $BaTiO_3$ cladding is increased.
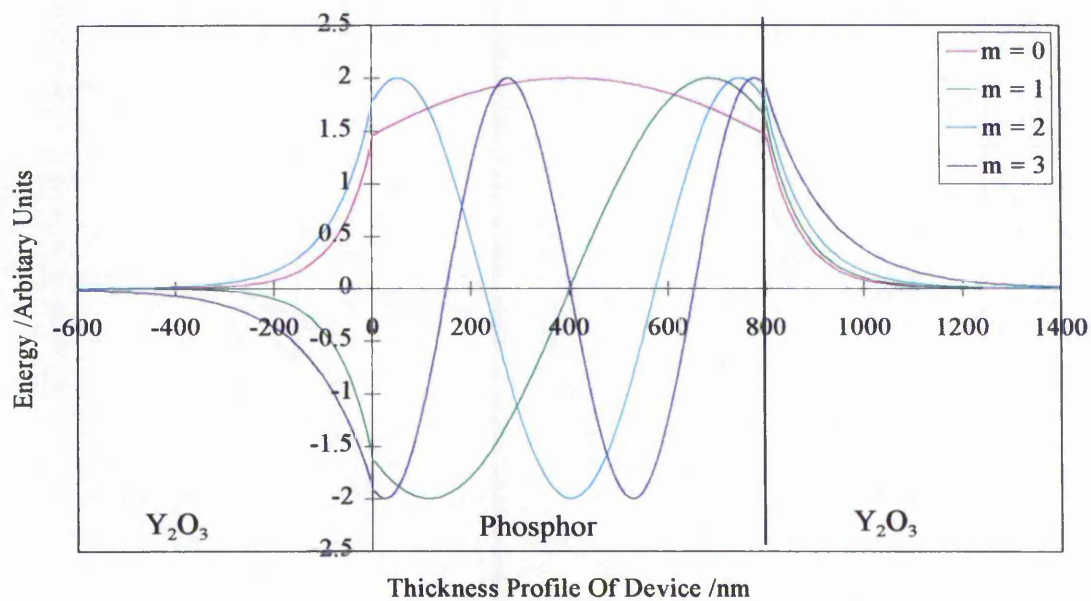
Figure 3.8 The profile of energy propagation through a Y$_2$O$_3$ clad device.
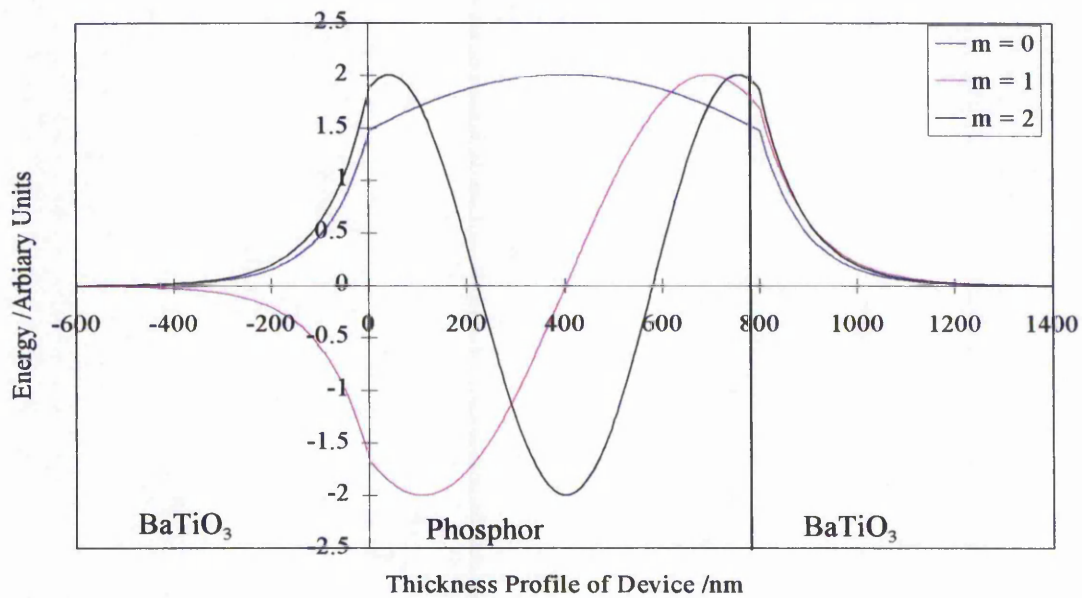
Figure 3.9 The profile of energy propagation through a BaTiO$_3$ clad device.

Layer	Y$_2$O$_3$ 300 nm Clad Device		BaTiO$_3$ 300 nm Clad Device	
	Relative Energy	Percent of Total Energy in each layer	Relative Energy	Percent of Total Energy in each layer
Phosphor	4848.242	81.6	3733.914	81.16
Insulator	1038.250	17.4	835.861	18.17
Outside Waveguide	54.531	1	30.699	0.67
Total	5941.023	100	4600.475	100

Table 3.4 Distribution of energy in the device structures.

	BaTiO$_3$ Cladding Thickness			
Layer	300 nm	370 nm	440 nm	490 nm
Phosphor	81.16	81.16	81.16	81.16
Insulator	18.17	18.53	18.69	18.78
Outside Waveguide	0.67	0.31	0.15	0.06
Total	100	100	100	100

Table 3.5 Percentage distribution of energy in the BaTiO$_3$ clad device.

Figure 3.10 shows the predicted decrease in the light propagating outside the device structure with increasing insulator thickness relative to a 300 nm clad device. It is this evanescently propagating energy outside of the structure that could be lost. Hence, a reduction in this energy will enhance the total attenuation for the laterally transmitted light.

The remainder of this chapter deals with the experimental investigation to test this theory, hence potentially demonstrating a reduction in the attenuation predicted in figure 3.10 with an increase in cladding thickness.
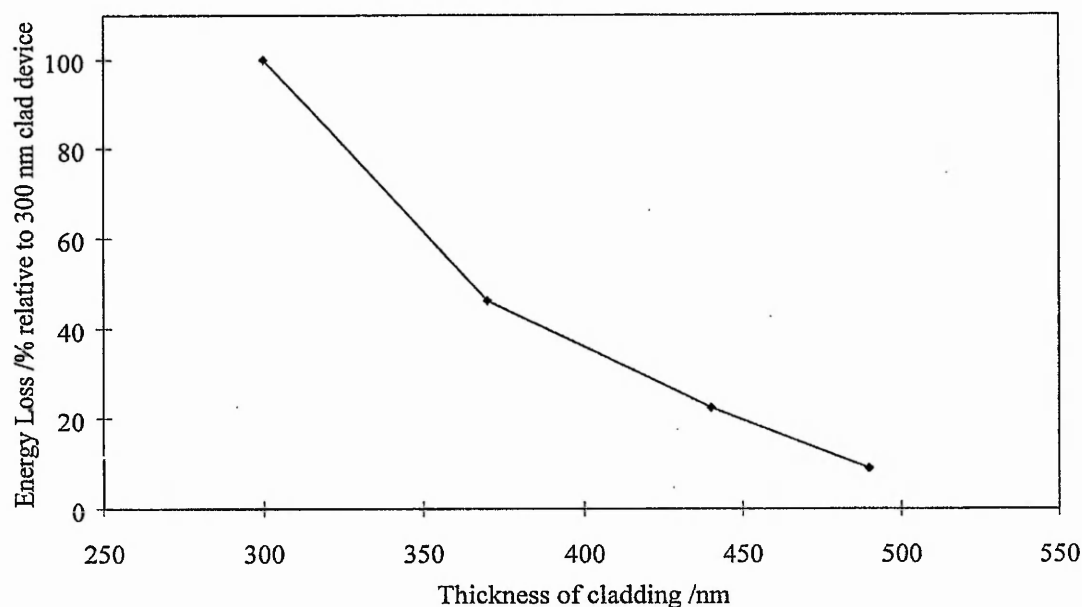
Figure 3.10 Predicted decrease in energy travelling outside (loss) the device structure with an increase in cladding thickness as compared to the loss from a 300nm clad device.

3.4 Device Fabrication Procedure

The devices utilised in this chapter, of the structure shown in figure 3.1, were deposited by RF magnetron sputtering in the dual cluster system shown in figure 3.11. Thin films of BaTiO$_3$ were deposited in the secondary chamber as described in chapter 2. The optimised deposition conditions were utilised, as summarised in table 3.7 and the thickness of these films was monitored in-situ utilising the interferometric technique detailed in section 2.5.1. Thin films of ZnS:Mn and Y$_2$O$_3$ were deposited in the LETFEL deposition chamber of the system utilising previously optimised conditions[3], summarised in table 3.7. All of the devices

were post deposition annealed at 700 °C for 1 hour, to give the optimum characteristics for the BaTiO₃ thin films and to activate the phosphor.
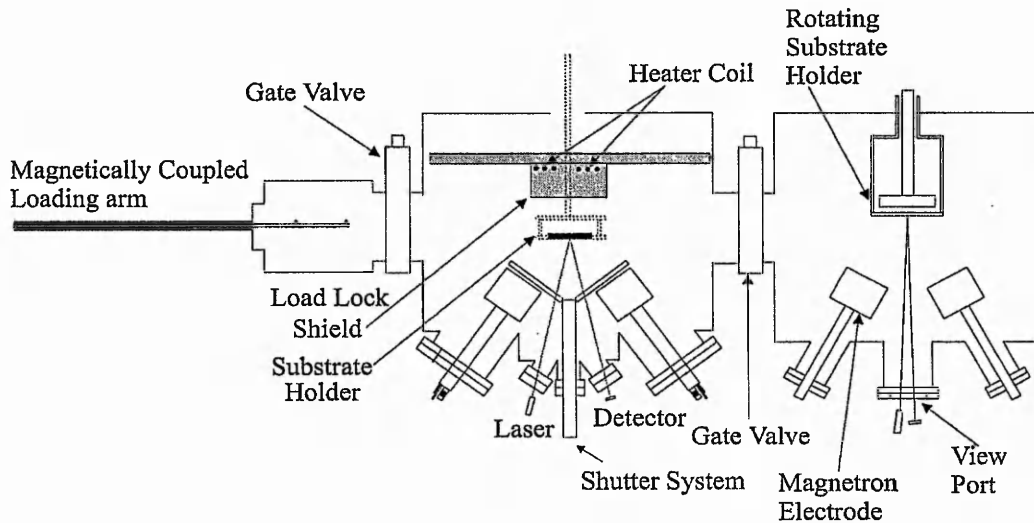
Figure 3.11 The final configuration of the dual chamber cluster magnetron sputter deposition system

Material	Ts - Substrate Temp °C	Power Density W cm⁻²	Sputter Pressure mT	% Oxygen in Argon	Ta - Annealing Temp °C
BaTiO₃	200	2.62	7	30	700
Y₂O₃	200	2.62	3	0	700
ZnS:Mn	200	1.95	3	0	700

Table 3.7 Summary of RF magnetron sputter deposition conditions for the thin films required in a LETFEL device.

To fabricate a large area, 0.54 mm by 3 mm, LETFEL test device the top electrode was formed by the thermal evaporation of 400 nm of Al through a shadow mask. An ohmic back contact to the Si substrate was made by the thermal evaporation of 500 nm of Al followed by a rapid thermal annealing process which has been shown to produce ohmic contacts [14]. The substrate was cleaved

producing LETFEL devices on which the direct measurement of the LV characteristic was performed.

3.5 Characterisation Procedure

Two major characteristics of the devices were measured: the luminance – voltage characteristic and the lateral attenuation of light.

3.5.1 Luminance Voltage Characterisation

The main characterisation of these devices was the determination of the Luminance - Voltage, L-V, response. From these measurements the variance in both the threshold voltage and maximum luminance across a substrate can be obtained. Also a measure of both the steepness of response, the switching voltage, of the L-V characteristic and the yield of the devices can be determined.

All of the characterisations were undertaken on a specially designed test rig for large area LETFEL devices at NTU. This is shown both pictorially and schematically in figure 3.12a and 3.12b respectively. In summary, a computer is utilised to control the output from a Tektronix AFG5501 function generator. This signal is amplified and applied across the device. The luminance is directly measured by the use of a Minolta LS110 luminance meter, which can be used to focus on a 1.1 mm diameter of the emitting area of the device. The computer also records the 0 to 1V analogue output from the MINOLTA LS110. The applied voltage is increased in a series of steps from a voltage below Vth up to a voltage of 30 volts above the knee of the LV characteristic. At each step both the applied

voltage and the measured luminance are recorded. The computer programme was written in such a way to produce a data output file containing the voltage and luminance readings at each step of the characterisation. This file was then imported into Microsoft Excel 5.0 to allow the L-V responses to be plotted. The computer programme also allows variation in both the drive waveform and frequency. All of the characteristics detailed here were carried out utilising a 5 KHz sine wave.
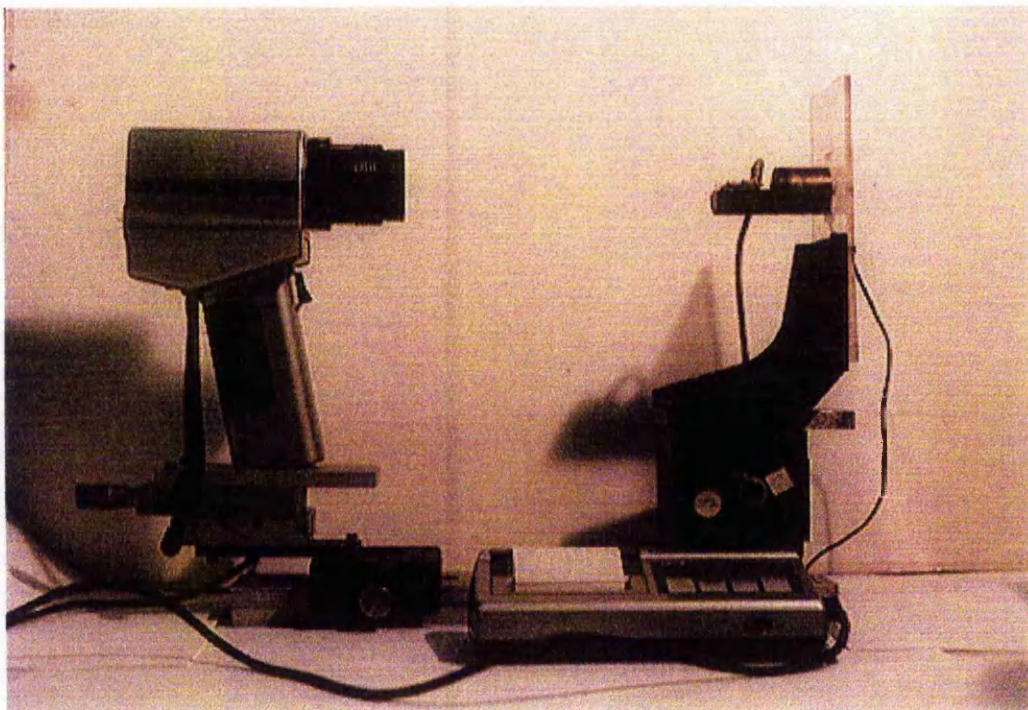
(a)
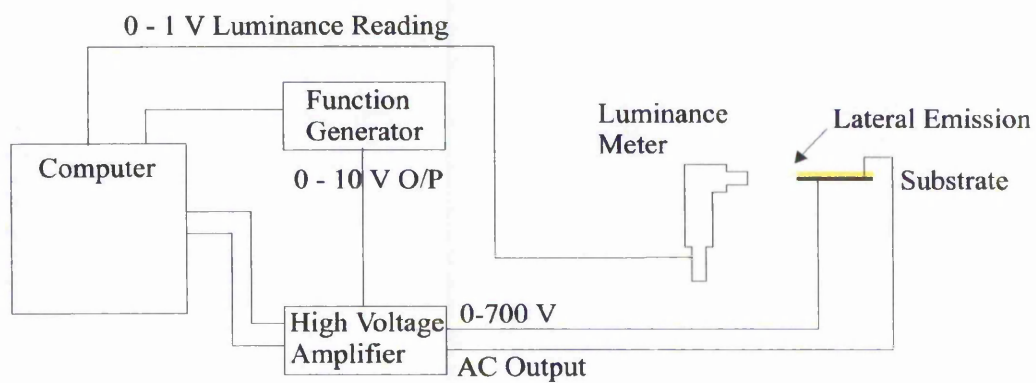
(b)

Figure 3.12 Configuration for the testing of the large area test LETFEL devices shown in figure 3.1.

3.5.2 Attenuation Measurements

Previous attenuation measurements on LETFEL devices have been carried out utilising devices on the same substrate with increasing lengths of active material leading into a micro mirror[15]. A plot of luminance Vs active material length yields a $(1 - (\exp^{-\alpha x}))$ rise up to a certain value of active material length. At device lengths greater than this value no further increase in luminance is measured, an example is shown in figure 3.14. Hence, this saturation length is defined as the attenuation length of the device. Utilising a curvefitting routine (Tablecurve version 1.0 from Jandel Scientific) and equation 3.14 a figure for the attenuation coefficient can thus be determined.

$$f(y) = I_0 \times (1 - \exp^{(-\alpha x)}) \qquad \text{Eq. 3.14}$$

Where I_0 is the maximum intensity, α is the attenuation coefficient and x is the length of the active material

To produce the devices to utilise this method the full fabrication route for micro-mirror based LETFEL devices has to be followed. This fabrication route has been detailed by R. Stevens[16]. This route involves up to five photolithographic masking and reactive ion etching stages following the standard thin film deposition. These stages are costly, time consuming and increase the risk of device failure due to misalignment and the shipping of the substrates between NTU and Qudos Ltd, Oxford. To simplify and reduce the fabrication time it was

decided to develop a new method to measure the attenuation coefficient of a LETFEL device.

The advantage of the large area test devices detailed in section 3.4 is that not only can the L-V response be measured from the cleaved edge, but the lateral decay in luminance away from the electrode can also be observed from above the device. A measure of this spatial decrease in light intensity from the edge will consequently yield a value for the lateral attenuation coefficient. In detail, a CCD image of the device is taken via a CCD camera mounted on a microscope linked to a computer with a frame grabber card. A computer programme commissioned by the author can then be used to measure the intensity at a series of points away from the electrode edge, as shown in figures 3.13a and b. This information is again fed into the curvefitting routine and an attenuation coefficient is calculated using equation 3.15.

$$f(y) = I_0 \times \exp^{(-\alpha x)} \qquad \text{Eq. 3.15}$$

Where I_0 is the maximum intensity, α is the attenuation coefficient and x is the length of the active material

CCD Camera

Microscope

Substrate

Device

Area Image

(a)

1.5 mm Electrode   Exposed Device Surface

Decay in
Luminance
From Edge

Pixel
Luminance

Distance from edge of device
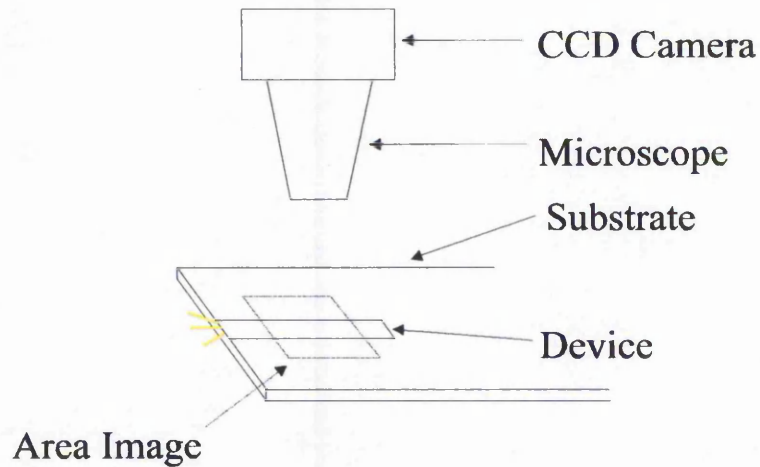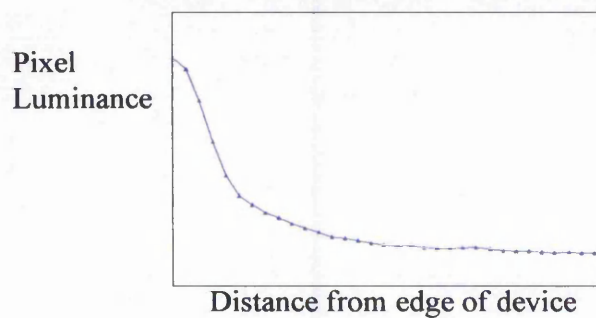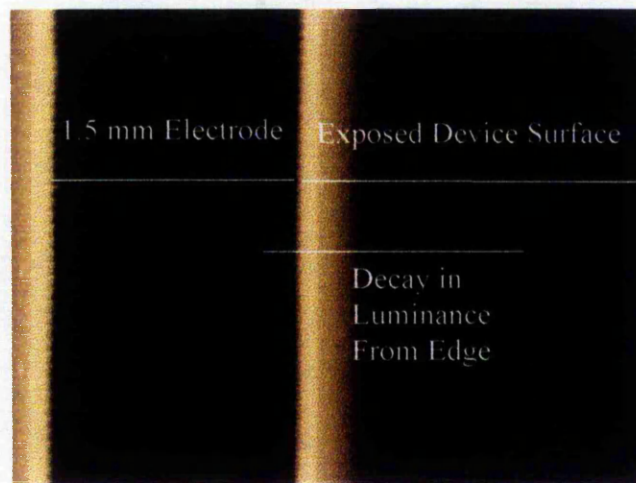
(b)

Figure 3.13 a and b Schematic of configuration for the CCD image capture of a LETFEL device. This shows the decay in luminance away from the electrode edge. A series of point measurements of luminance and distance from the edge are taken to determine the attenuation coefficient of the device.
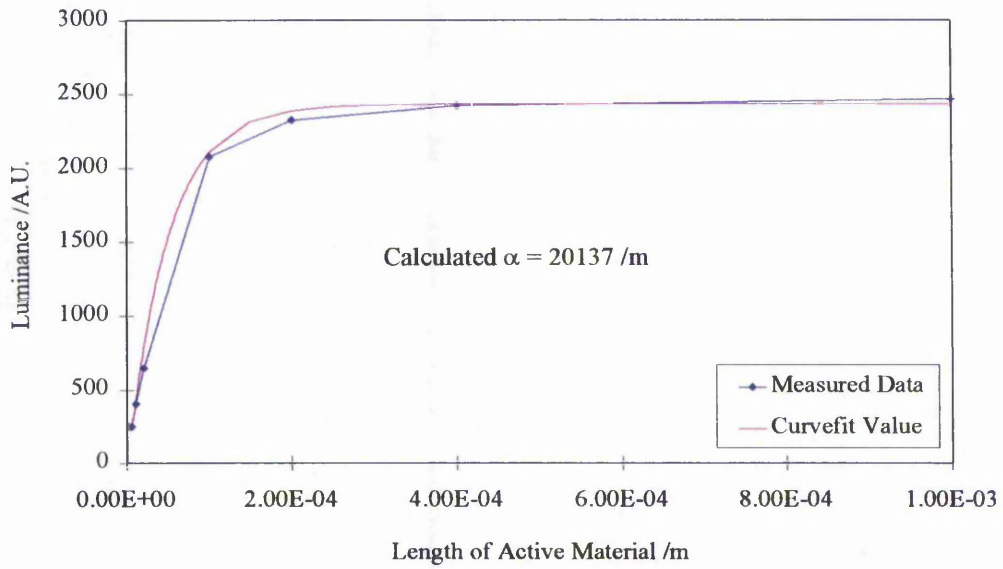
Figure 3.14 Comparison of measured luminance and calculated attenuation. Using the increase in active material method.
The device structure tested was Y_2O_3(300 nm)/ZnS:Mn(800 nm)/Y_2O_3(300 nm,
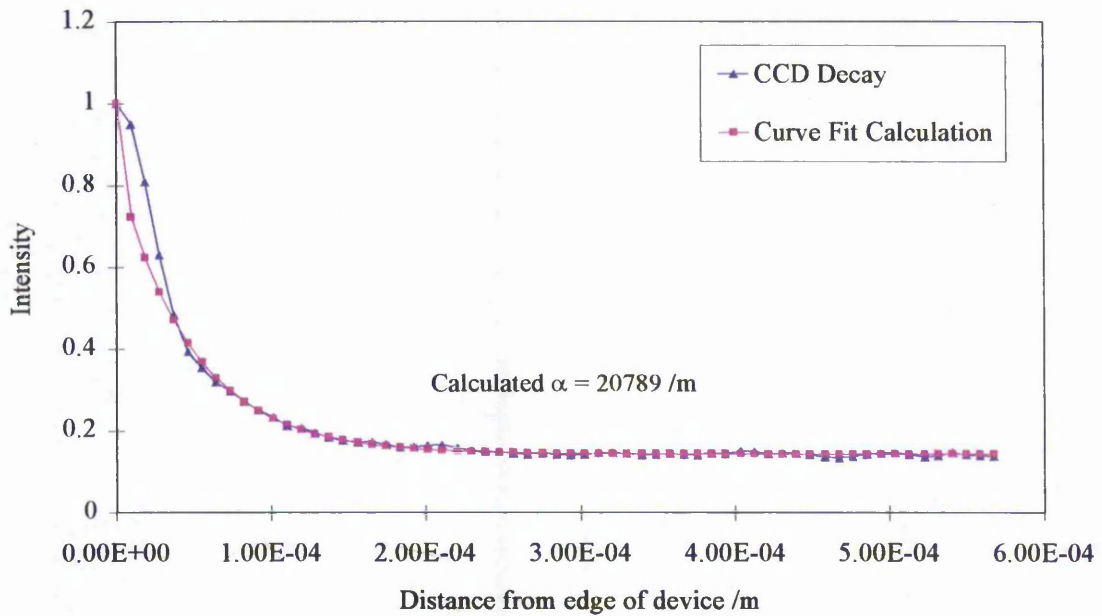
driven by a 5 KHz sine wave at Vth + 50 Volts (250V).

Figure 3.15 Measured data and curvefit calculation for the attenuation coefficient of the device structure Y_2O_3(300 nm)/ZnS:Mn(800 nm)/Y_2O_3(300 nm, driven by a 5 KHz sine wave at Vth + 50 Volts (250V).

An initial test was performed using a standard $Y_2O_3/ZnS:Mn/Y_2O_3$ structure. The attenuation coefficient for this device structure was determined utilising both the standard method of increasing the active material length and the novel CCD imaging techniques. Figures 3.14 and 3.15 give both the measured results and the calculated attenuation coefficients utilising both methods. The attenuation coefficient from the increase in active material length was 20137 m^{-1}, the corresponding value utilising the imaging technique was 20789 m^{-1}. These results confirmed that using the CCD image capture method with the simple test structures the calculated attenuation coefficient was within ± 5 % of the value calculated utilising the standard increase in active material length method. The values determined here are also compatible with those published previously by the research group at NTU[15]. Hence, for all of the attenuation measurements given here the CCD imaging technique with simple test structures was utilised.

3.6 Results

For simplicity, the questions to be addressed by the work presented in chapter, as detailed in section 3.1, have been divided into three separate investigations. Stage one incorporates the first two areas of interest, namely:-

a) Are $BaTiO_3$ thin films suitable for use as insulators in the LETFEL device structure?

and

b) What is the best combination of the two insulator materials?

Stage 2 was to fabricate a series of devices to investigate the effect of increasing the thickness of the insulator layers.

The final stage was the determination of the attenuation coefficients for comparison to the geometric model.

3.6.1 The Effect of the Position and Material of the Insulator on the Performance of a LETFEL Device

Four LETFEL device structures of the form in figure 3.1, with electrode configuration shown in figure 3.16, were fabricated varying the insulator material and position as detailed in table 3.8. All of the devices had 800 nm ZnS:Mn phosphor thin films and were annealed at 700 °C for 1 hour.

Using Eq. 3.2 and 3.3, the variation in capacitance of the different device configurations was determined. A prediction of the expected threshold voltage of each device structure was also made utilising Eq. 3.4c. The details of the variation in capacitance and the threshold voltage are given in table 3.9.
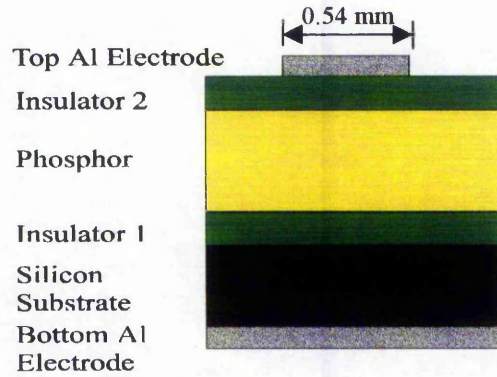
Figure 3.16 Large area LETFEL test device configuration.

The resultant L-V characteristics are shown in figure 3.17. Each characteristic on the graph is the mean characteristic from a set of ten devices from each substrate. Table 3.10 details the mean and variance of the threshold voltage, Vth, and the luminance at Vth + 50 V of all the devices tested. From these characteristics it can be seen that all of the devices exhibited typical L-V responses. That is a region of non-linearity. An important feature of the L-V response is the switching voltage. This is the applied voltage required to switch the device from the off to the on state, defined as the difference between Vth and a voltage at 20 V above the knee of the LV response. The mean and variance of the switching voltages are also detailed in table 3.10.

Substrate	Insulator 1		Insulator 2		Reasoning
Number	Material	Thickness /nm	Material	Thickness /nm	
124	Y_2O_3	300	Y_2O_3	300	Control
120	$BaTiO_3$	300	Y_2O_3	300	$BaTiO_3$ Bottom
126	Y_2O_3	300	$BaTiO_3$	300	$BaTiO_3$ Top
125	$BaTiO_3$	300	$BaTiO_3$	300	$BaTiO_3$ Both

Table 3.8 Structural details of four initial device structures fabricated. Showing the variation of insulator material and position.

Substrate Number	Ins 1 Capacitance /nF	Ins 2 Capacitance /nF	Phosphor Capacitance /nF	Total Capacitance /nF	Predicted Threshold Voltage /V
124	0.76	0.76	0.38	0.19	200
120	1.24	0.76	0.38	0.21	194
126	0.76	1.24	0.38	0.21	194
125	1.24	1.24	0.38	0.24	188

Table 3.9 Summary of capacitance and predicted threshold voltages for the four different device structures fabricated in section 3.5.1.
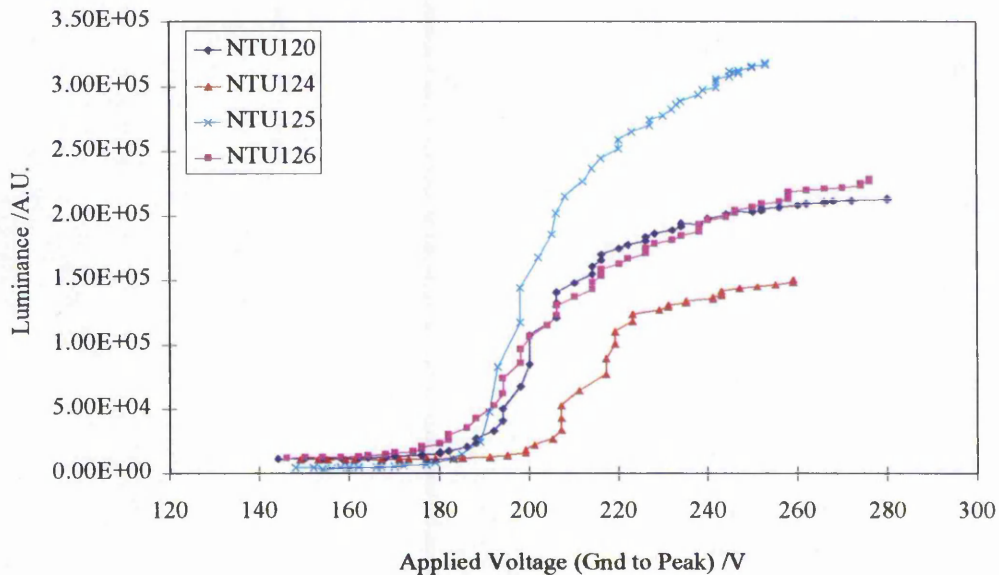
Figure 3.17 Luminance - voltage characteristics for the variation in cladding materials.

Substrate Number	Threshold Voltage /V		Luminance at Vth + 50 V /fL		Switching Voltage /V
	mean	σ	mean	σ	mean
124	202	2.3	144905	1210	39
120	194	1.7	201461	1362	40
126	194	1.2	198844	1375	50
125	189	1.6	297326	1450	43

Table 3.10 Summary of the luminescent properties of the four device structures fabricated in section 3.6.1.

On comparison of the L-V characteristics between the different device structures many interesting observations can be made. Firstly, regarding the threshold voltage of the devices. As predicted in table 3.9 the threshold voltage of the devices is dependant on the insulator material used on each side of the phosphor. The predicted values in table 3.9 and the measured values in table 3.10 have a close correlation. This confirms that the dielectric constant of the BaTiO₃ thin films is unaffected by its use as an insulator in the LETFEL device, also the internal electric field strength required for luminance, E_z, is independent of the insulator used.

With regards to the luminance, in section 1.3 it was predicted that an increase in cladding thickness would yield an improvement in the waveguiding properties of the LETFEL device. This would in turn lead to an increase in measured luminance. All of the devices fabricated here have the same cladding thickness so there was no change in the light confinement of the LETFEL structure and hence no change in the measured luminance was expected due to this effect. However, on comparison of the measured luminance of the different device structures fabricated here it can be seen that the luminance at Vth + 50 V does indeed vary. The device exhibiting the highest overall luminance was the device with BaTiO₃

as both insulators 1 and 2. The two asymmetrical devices exhibited similar luminances with the device having Y_2O_3 as both insulators 1 and 2 exhibiting the lowest luminance.

As discussed above, the increase in measured luminance of the devices utilising at least one $BaTiO_3$ thin film could not be due to an increase in the light confinement as the cladding thickness for all the devices was kept constant. The increase in luminance could be due to one or more of the other four effects discussed in section 3.2. The first effect could be due to a change in the interface states at the $Y_2O_3/ZnS:Mn$ interface and the $BaTiO_3/ZnS:Mn$ interface. If for example there is a higher density of interface states at the $BaTiO_3/ZnS:Mn$ interface there may be an increased supply of electrons, hence the probability of injection of one of these electrons into the phosphor to produce luminescence would be higher.

Secondly, each of the films exhibits an attenuation coefficient, which in turn contributes to the overall attenuation coefficient of the device structure. If the attenuation of the light propagating in the $BaTiO_3$ thin films is less than that of the light propagating in the Y_2O_3 thin films an increase in measured luminance would be expected. Measurements of the attenuation coefficient of these devices have been taken and are dealt with in detail in section 3.5.3.

Thirdly, if the $BaTiO_3$ thin films exhibit a higher degree of crystallinity over the Y_2O_3 thin films, the ZnS:Mn could also show a higher degree of crystallinity with insulator 1 being $BaTiO_3$. As reported by Minami, an increase in crystallinity of

ZnS:Mn would yield a higher measured luminance[9]. In this case, as the luminance of the two asymmetrical devices is similar, it is assumed that the crystallinity of the ZnS:Mn is similar. Therefore, the crystallinity of the Y_2O_3 and $BaTiO_3$ must also be similar and would not contribute to enhanced phosphor performance.

Finally, waveguide theory states that as the difference in refractive indices of the guiding and the cladding region of a waveguide is reduced less light is lost due to scattering [7]. The difference in refractive index between $BaTiO_3$ and ZnS:Mn is 0.25 with the equivalent difference utilising Y_2O_3 is 0.35, thus leading to a higher scattering factor with the Y_2O_3.

To gain an insight into which of these effects may be contributing to the increase in measured luminance the transient luminance from an asymmetrical device was examined by coupling the emitted light into a photo multiplier tube, (PMT), via an optical fibre. Both the outputs from the PMT and the voltage amplifier were observed on an oscilloscope. This configuration, shown in figure 3.18, allows the observation of the transient intensity of the light emitted on every pulse, i.e. from each interface. Figure 3.19 shows a typical trace from the oscilloscope. It is seen that the luminance from the +ve going pulse is greater than the luminance from the -ve going pulse (applied to the top electrode). On inspection of the device structure in figure 3.1 it is seen that the device tested has $BaTiO_3$ as insulator 1 and Y_2O_3 as insulator 2. Therefore, the greater luminance is coming from the $BaTiO_3$/ZnS:Mn interface. This increase could be due to either an increase in

density of interface states or an increase in efficiency of the electrons coming from the BaTiO$_3$/ZnS:Mn interface or in fact it could be due to a reduction in scattering caused by either the reduction of the difference in refractive indices or a change in surface roughness at the interface. The same test was performed utilising the second asymmetric device. This also showed a greater luminance from the BaTiO$_3$/ZnS:Mn interface over the Y$_2$O$_3$/ZnS:Mn interface.
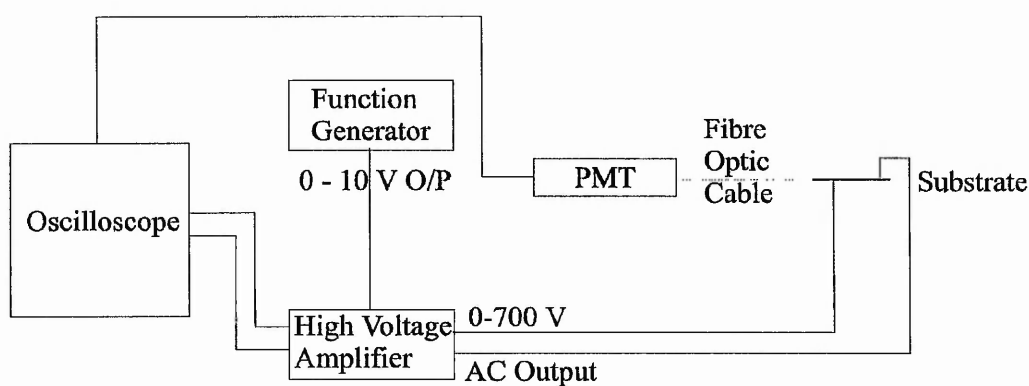
Figure 3.18 Measurement system used to investigate the transient luminescent properties of LETFEL devices.
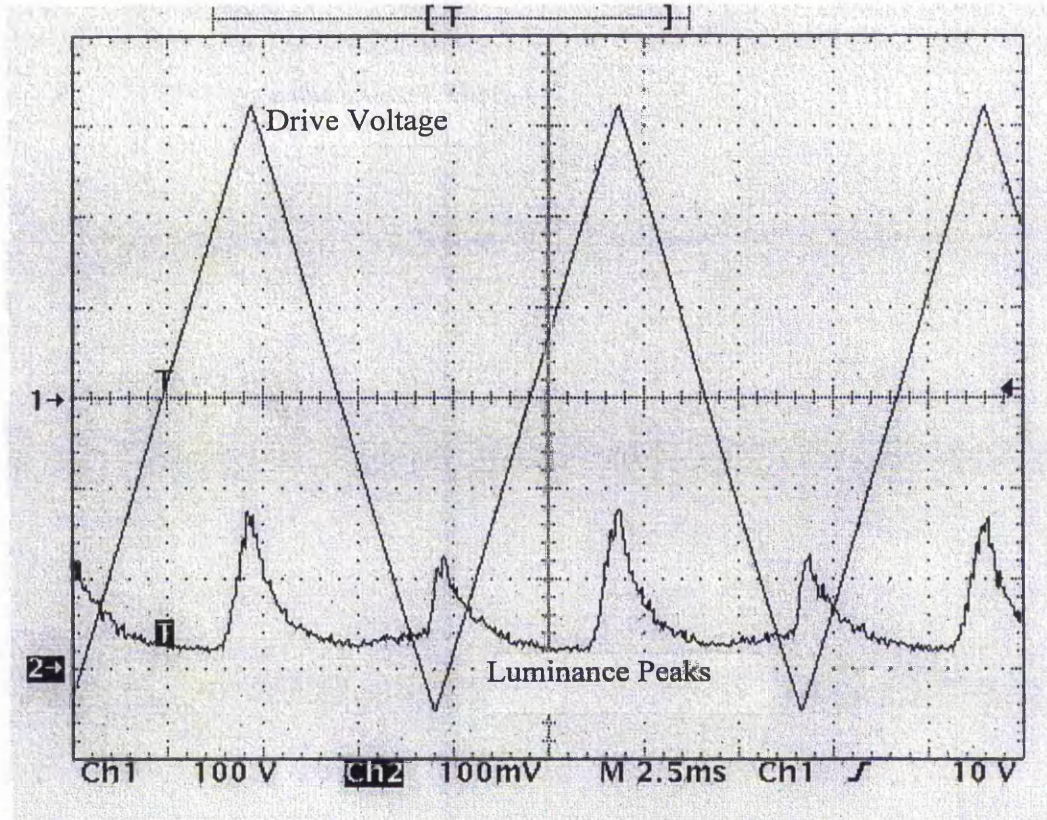
Figure 3.19 A typical interface - luminance trace from an asymmetric device. The device structure being that of substrate 120 in table 3.8. It shows that there is a higher luminance from the BaTiO$_3$/ZnS:Mn interface than the Y$_2$O$_3$/ZnS:Mn interface.

3.6.2 Delamination

During further investigation of the devices, the devices with BaTiO$_3$ as both insulators 1 and 2, consistently exhibited delamination - peeling away from the substrate, see figure 3.20. This unfortunately indicates that these devices are unsatisfactory for LETFEL use. Either residual stress from the deposition of the BaTiO$_3$ thin films or the absorption of water from the atmosphere into the BaTiO$_3$ thin films could cause the delamination. Absorption of water from the atmosphere has been previously reported[17] and delamination was reduced if the

devices were stored in vacuum. The asymmetrical device with $BaTiO_3$ as insulator 2 also suffered from this delamination. However, the devices with $BaTiO_3$ as insulator 1 and Y_2O_3 as insulator 2 did not suffer from this problem. This suggests that the problem could be due to water absorption.
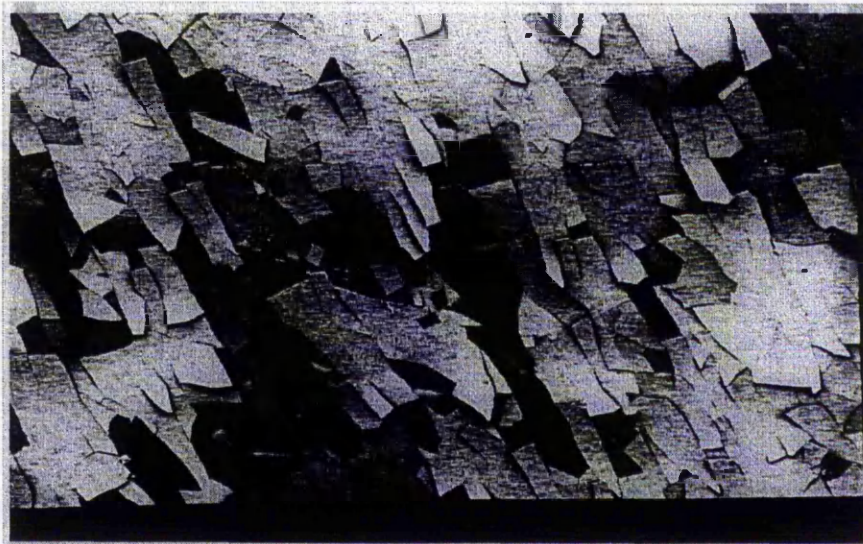
Figure 3.20 An example of delamination of the thin films from the substrate in a $Y_2O_3/ZnS:Mn/BaTiO_3$ device.

3.6.3 The Effect of Insulator Thickness on The Performance of the LETFEL Device

The next stage of this investigation was to determine the effect of increasing the cladding thickness on the device performance. Considering the delamination problem, it was decided that the device structure to be utilised should be that with $BaTiO_3$ as insulator 1 and Y_2O_3 as insulator 2. A set of four devices were

fabricated. With BaTiO$_3$ insulator thickness varied from 300 nm to 490 nm. For this study, the thickness of the BaTiO$_3$ insulator was limited to a maximum of 490 nm. This would give a threshold voltage of 200 V, which is comparable with the threshold voltage of a typical LETFEL device. Table 3.11 details the range of four devices fabricated including the device capacitance and the predicted threshold voltage for each thickness of BaTiO$_3$ insulator. Each device had the standard 800 nm ZnS:Mn phosphor layer and a 300 nm Y$_2$O$_3$ insulator 2 layer. The devices were post deposition annealed at 700 °C for 1 hour.

Substrate Number	BaTiO$_3$ Thickness /nm	BaTiO$_3$ Capacitance /nF	Total Capacitance /nF	Predicted Threshold Voltage /V
145	300	1.24	2.38	194
153	370	0.99	2.13	196
154	440	0.84	1.98	198
156	490	0.75	1.89	200

Table 3.11 Summary of capacitance and predicted threshold voltages for the four different device structures fabricated in section 3.5.2.

The resultant L-V characteristics are shown in figure 3.21. Each datum on the graph is the mean value from a set of ten devices from each substrate. Table 3.12 details the mean and variance of the threshold voltage, Vth, and luminance at Vth + 50 V of all the devices tested. Figure 3.22 shows the increase in luminance at Vth + 50V as the cladding thickness increases. From these characteristics it can be seen that all of the devices again exhibited typical L-V responses. That is a region of non-linearity. The mean and variance of the switching voltages are also detailed in table 3.12.
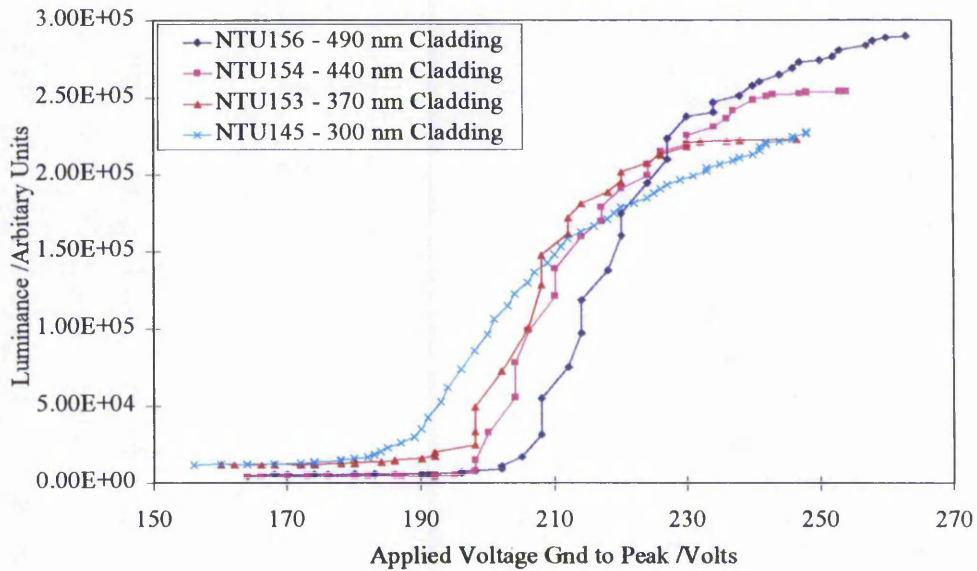
Figure 3.21 Summary of the L-V characteristics fabricated in section 3.6.2. This shows an increase in both the threshold voltage and maximum luminance as the insulator thickness increases.

Substrate Number	Threshold Voltage /V		Luminance at Vth + 50 V /KfL		Switching Voltage /V
	mean	σ	mean	σ	mean
145	189	2.3	209340	1249	47
153	195	1.7	221859	1356	43
154	198	1.9	248570	1106	42
156	202	2.1	272898	1436	45

Table 3.12 Summary of the luminescent properties of the four device structures fabricated in section 3.5.2.
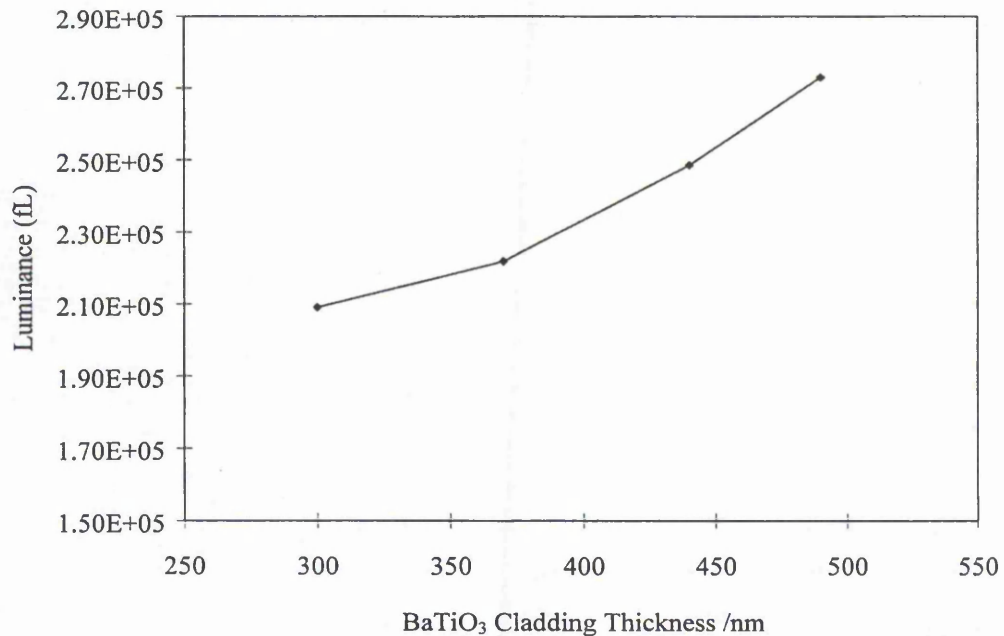
Figure 3.22 Variation in measured luminance at Vth + 50V with an increase in the BaTiO$_3$ cladding thickness.

Two effects are observed from these characteristics. Firstly, the threshold voltage of the devices increases with an increase in cladding thickness. This is as expected since an increase in cladding thickness decreases the overall capacitance of the device structure.

Secondly, the observed luminance, at Vth + 50 V, increases with insulator thickness.

Both the interfaces and the refractive index differences are the same for all four of these devices. The increase in luminance can thus be attributed to the increase in cladding thickness. This is consistent with the hypothesis of section 1.5 that an

increase in cladding thickness would yield an improvement in the light guiding properties of the device.

3.6.4 Attenuation Measurements

The attenuation coefficients for all four of the devices with different BaTiO$_3$ insulator thickness' have been calculated utilising the CCD imaging method described in section 3.5.2. Figure 3.23 shows the variation in attenuation coefficient with the increase of the BaTiO$_3$ cladding thickness. Each datum is the mean attenuation coefficient from ten devices.
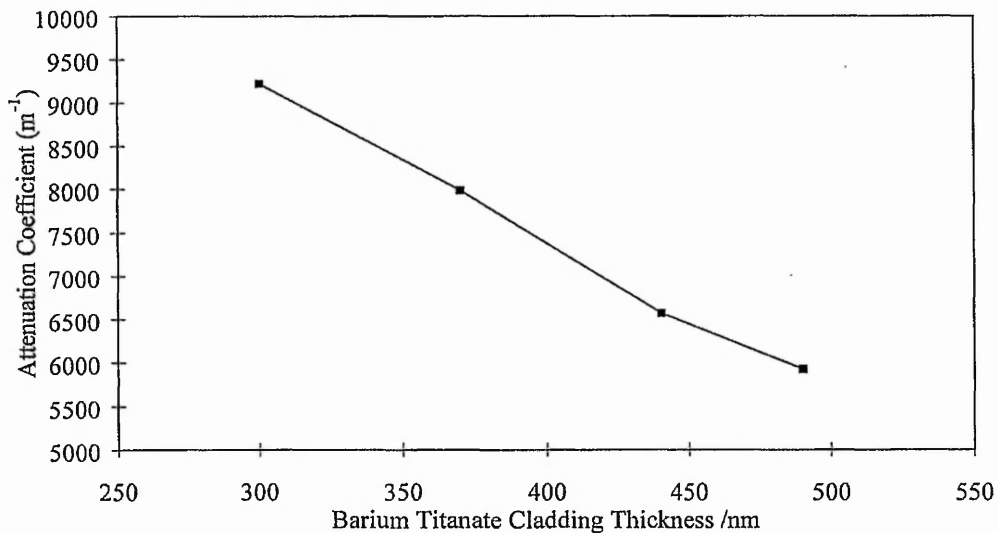
Figure 3.23 Decrease in attenuation coefficient with an increase in BaTiO$_3$ cladding thickness.

As expected, the attenuation coefficient of the device decreases with an increase in cladding thickness, due to the concomitant improvement in optical confinement

of the devices. None of the other effects discussed in section 3.2 would be expected to influence this result, since it is only the cladding thickness which has been altered in this set of devices. A comparison between the measured and predicted increase in light confinement is given in section 3.7.

3.7 Comparison Between the Measured Results and the Geometric Model Proposed in Section 3.3

One of the main aims stated in section 3.1 was to determine the relationship, if any, between the theory of a dielectric waveguide and the LETFEL device structure.

Due to the problems discussed in section 3.6.1 it was decided to utilise asymmetric devices for the investigation into the effect of increasing the cladding thickness. The device structure used was $Si/BaTiO_3/ZnS:Mn/Y_2O_3/Al$. Therefore the model had to be adjusted to reflect this device structure. It has been assumed that there are only three modes potentially supported in the asymmetric device structure due to the higher critical angle of $BaTiO_3$. The calculations were redone and the resulting energy profile through the device structure is shown in figure 3.24 and summarised in table 3.6. Figure 3.25 shows the predicted percentage decrease in energy propagating outside of the device with an increase in the $BaTiO_3$ cladding thickness, as compared to the standard 300 nm clad device.
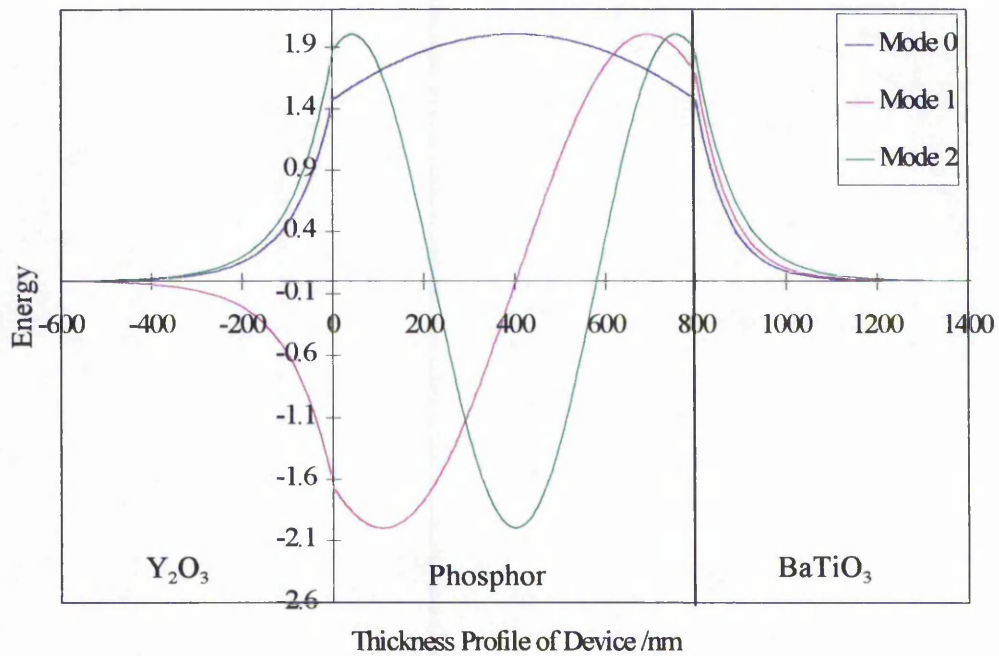
Figure 3.24 The profile of energy propagation through an asymmetric device.

	BaTiO₃ Cladding Thickness			
Layer	300 nm	370 nm	440 nm	490 nm
ZnS:Mn	82.43	82.43	82.43	82.43
BaTiO₃	9.63	9.80	9.89	9.95
Y₂O₃	7.45	7.45	7.45	7.45
Outside Waveguide	0.49	0.32	0.23	0.18
Total	100	100	100	100

Table 3.6 Percentage distribution of energy in the asymmetrical device with an increase in BaTiO₃ cladding thickness.
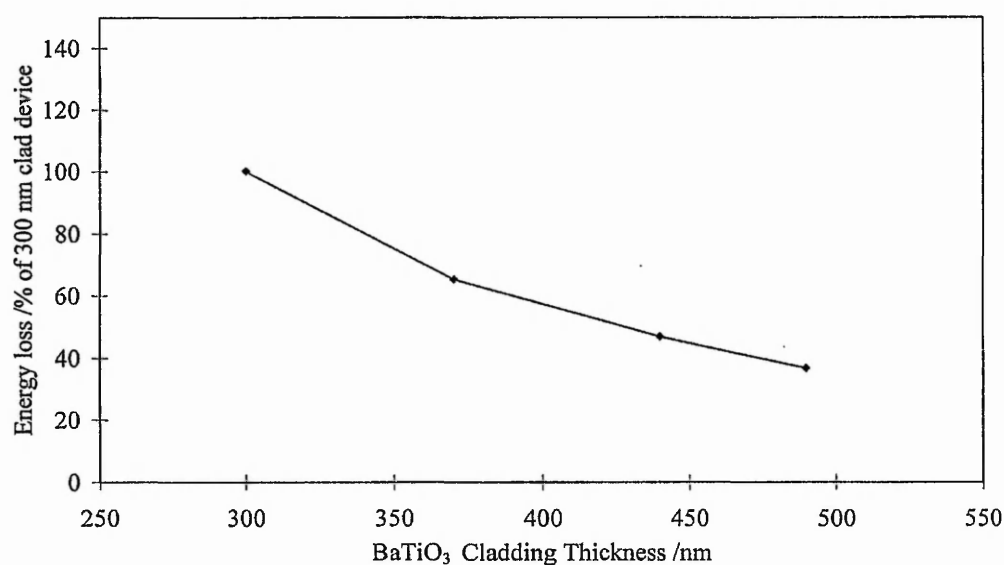
Figure 3.25 Predicted change in energy propagating outside the asymmetrical device structure with an increase in BaTiO₃ cladding thickness.

Presented in figure 3.26 is a summary of the predicted change in the light propagating outside of the waveguide with an increase in cladding thickness. Also shown is the decrease in attenuation coefficient from the measured results. The values plotted are all normalised with respect to the 300 nm clad device.
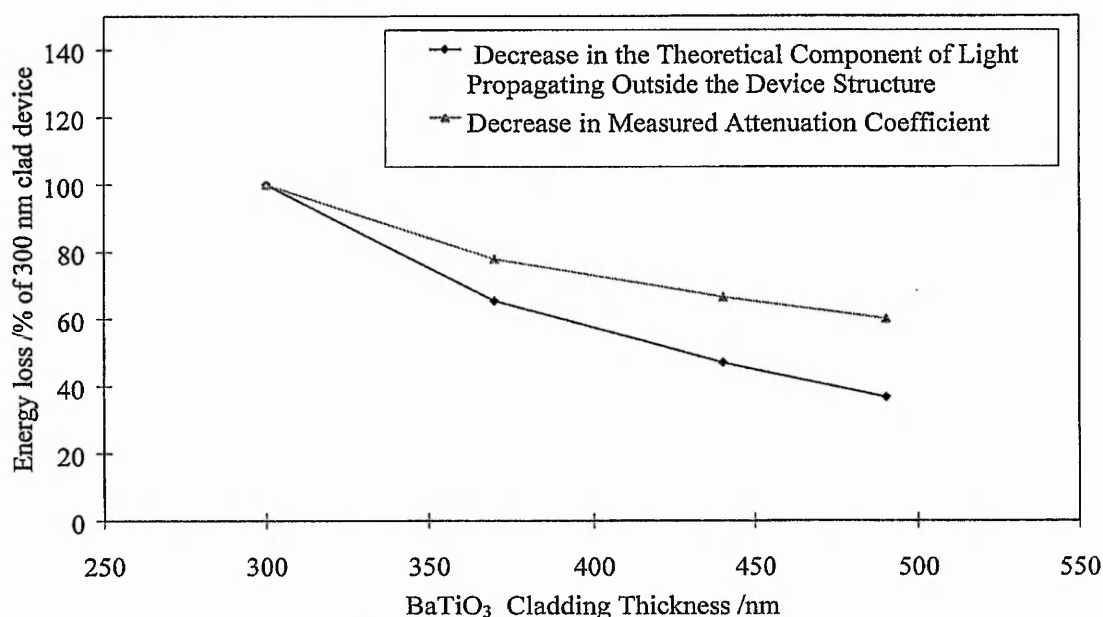
Figure 3.26 Relative change in energy loss and attenuation coefficient with an increase in cladding thickness. All calculated with respect to the 300 nm clad device

It can be clearly seen from figure 3.26 that the measured results do in fact follow the same trend as the predicted values. This infers that there is indeed a relationship between the decrease in attenuation coefficient and the decrease in light propagating outside the device structure as determined via the model of section 3.3. These results represent the first demonstration of a direct relationship between the LETFEL device structure and that of the step index waveguide. Consequently, it is now possible to predict a value for the attenuation coefficient for any device of the structure detailed in section 3.4.2. The optimum thickness of the cladding would be at least twice the wavelength of the emitted light (585 nm for ZnS:Mn), i.e. at least 1.17 μm. This is usual for a step index fibre optic cable

and ensures very low losses due to evanescent outcoupling from the guide region[12].

3.8 Conclusions

Demonstrated here for the first time are LETFEL devices utilising high dielectric constant BaTiO$_3$ thin film insulators. Devices with BaTiO$_3$ thin films as both insulators 1 and 2 have exhibited the highest reported luminance from a LETFEL device structure, or indeed from any reported electroluminescent device. This structure was unfortunately prone to delamination effects. The optimum device structure has been thus determined to be BaTiO$_3$/ZnS:Mn/Y$_2$O$_3$. It has been shown that the luminance from the BaTiO$_3$/ZnS:Mn interface is greater than the corresponding Y$_2$O$_3$/ZnS:Mn interface. This effect may be due to a higher density of interface states or the decrease in scattering due to the reduction of the difference in refractive indices. Of major significance is that demonstrated for the first time is that the LETFEL device structure behaves in accordance with the predicted model of a step index waveguide. It has been shown that as the thickness of the insulator is increased the corresponding measured luminance also increases. This is due to enhanced confinement of the light in the device structure and has been shown to be linear with respect to the increase in insulator thickness. It has also been shown that there is an agreement between the trends of the decrease in measured attenuation coefficient and the theoretical decrease in the light propagating outside the device. This shows that the device behaves according to the model of a step index waveguide. Finally, from these results, it may be concluded that the ideal LETFEL device structure would include a more

stable insulator with an even higher dielectric constant. This would enable a very thick insulator layer to be utilised, hence increasing the light confinement further. A discussion of further alternative insulator materials is given in section 5.7.1.

3.9 References

1   W. M. Cranton, D. M. Spink, R. Stevens and C. B. Thomas; *Thin Solid Films,* 226 (1993) p 156-160.

2   C. B. Thomas, R. Stevens, W. M. Cranton, I. P. McClean, M. R. Craven and A. H. Abdullah; *Society for Information Display International Symposiam,* SID 95 Digest (1995) p887-890.

3   W. M. Cranton Ph.D. Thesis. University of Bradford (1995)

4   J. Wilson and J.F.B. Hawkes; *Optoelectronics :- An Introduction,* (Prentice Hall, London, 2nd Edition) (1988) P 305.

5   S. Tanaka, H. Kobayashi, H. Sasakura and Y .Hamakaura; *Jnl of Appl. Phys.* 47 (12) (1976) p 5391-5393

6   D. Marcuse; *Theory of Dielectric Optical Waveguides,* (Academic Press Inc. San Diego) (1974) Chapter 1.

7   M.R. Craven, W.M. Cranton, S. Toal and H.S. Reehal; *Semiconductor Science and Technology,* 13 (1998) p404-409.

8   Z.K. Kun, D. Leksell, P.R. Malmberg, J. Murphy and L.J. Sienkiewicz, *J. Electronic Materials,* 10(1) 1981 p287.

9   T. Minami, Y. Kuroi and S. Takata, *J. Vac. Sci. Technol. A,* 14(3) 1996 p1736.

10   Y. Nakanishi, S. Mori, T. Nakamura, H. Tatsuoka, H. Kuwabara and Y. Hatanaka, *Materials Chemistry and Physics,* 43 (1996) p 292-295.

11   J.H Ryu, S. Lim and J.F. Wager; *Thin Solid Films.* 248 (1994) p 63-68.

12   J. Wilson and J.F.B. Hawkes; *Optoelectronics :- An Introduction,*

(Prentice Hall, London, 2nd Edition) (1988) Chapter 8.

13   J. Wilson and J.F.B. Hawkes; *Optoelectronics :- An Introduction,*

        (Prentice Hall, London, 2nd Edition) (1988) P 307.

14   D. Sands; Ph.D. Thesis, University of Bradford (1987).

15   A. H. Abdullah PhD Thesis The Nottingham Trent University (To be

        Published)

16   R. Stevens Ph.D. Thesis University of Bradford (1994)

17   B. Chornik, V. A. Fuenzalida, C. R. Grahmann and R. Labbe; *Vacuum,* 48

        (2) (1997) p161-164.

Chapter 4 Fabrication Of High Resolution LETFEL Devices

4.1 Introduction

In the preceding chapters the deposition and optimisation of the insulating thin film has been discussed. A method of test device fabrication has been reported. Devices utilising this method have been successfully characterised. Full details of the fabrication procedure of these devices can be found in section 3.4. In summary, to fabricate a large area, 0.54 mm by 3 mm, LETFEL test device from the structure in figure 4.1a, the top electrode was formed by the thermal evaporation of 400 nm of Al through a shadow mask. An ohmic back contact to the Si substrate was made by the thermal evaporation of 500 nm of Al followed by a rapid thermal annealing process which has been shown to produce ohmic contacts [1]. The final device structure is shown in figure 4.1b. This method is ideal for these types of structure as it is quick and requires no lithography or etching steps. The substrate simply requires cleaving prior to testing. However, when fabricating high resolution displays a more complex procedure is required. In a high resolution LETFEL device, as shown in figure 4.2, micro-mirrors are utilised to reflect the laterally emitted light vertically [2]. The electrode is defined to allow the reflected light to escape from the region above the micro-mirror, which is the light emitting aperture of the device. The micro-mirrors are 1.5 μm high and 3 μm wide at the base. Therefore, the apertures above the micro-mirrors are typically 3 μm wide. It is impossible to achieve the resolution required for LETFEL displays using a shadow mask. To provide the required resolution of a

device feature, a series of photolithographic masking and etching procedures must be followed.
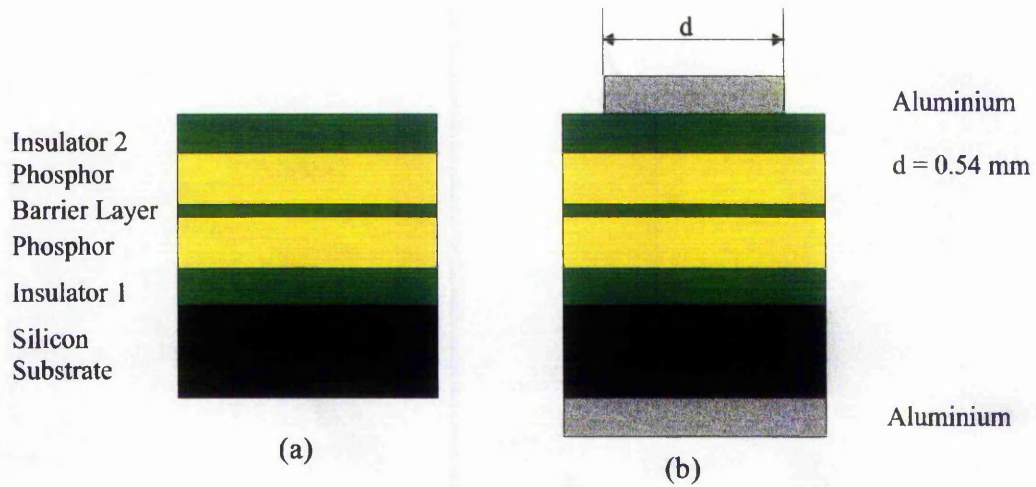
Figure 4.1 (a) Basic LETFEL test structure with no micro-mirrors and (b) showing Al top electrode after evaporation through a shadow mask.
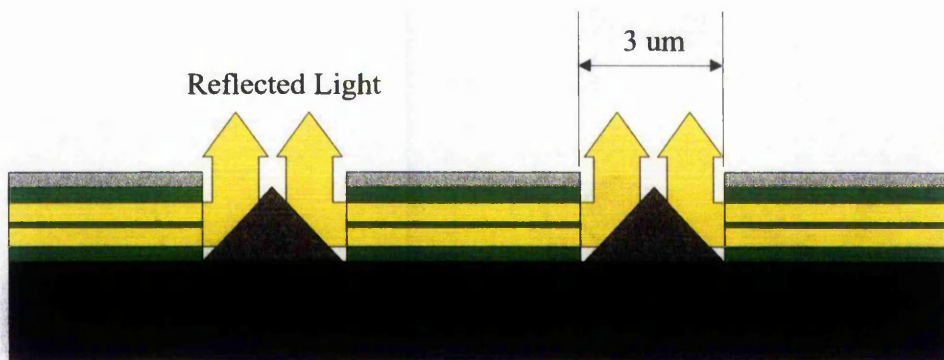
Figure 4.2 The LETFEL device structure utilising lateral emission reflected via micro-mirrors. The critical dimensions are of the order of ± 0.5 μm.

Typically, it is surface emitted light that is utilised from an AC TFEL device[3], requiring either a transparent top electrode or a transparent lower electrode and substrate must be utilised, as shown in figure 4.3. One option is to use an Indian Tin Oxide (ITO) electrode[3] and a glass substrate[3]. Alternatively as in LETFEL devices the inherent design utilises lateral emission reflected vertically via micro-mirrors[2], shown in figure 4.2. This negates the necessity for either a transparent electrode or substrate as the lateral light is reflected via micro-mirrors through the aperture. Therefore, a Si substrate and an Al electrode can be utilised. Aluminium is advantageous over ITO due to it's lower resistivity, $\rho = 2.417 \times 10^{-8}$ Ωm[4] compared to 3.0×10^{-4} Ωm for ITO[5], and use in standard Si processing. The deposition and etching conditions are well known and wire bonding can be made to metal pads. ITO requires the deposition of Al or gold in the bond pad region to enable wire bonding[6].

The use of a Si substrate has many advantages over glass. Previous optimisation of the post deposition annealing process for barrier layer LETFEL devices has reported that annealing at 700 °C for 1 hour produces devices with the highest luminance and sharpest L-V characteristic[7]. A low cost transparent substrate cannot be annealed to this temperature whereas a Si substrate can. The Si substrate also enables the integration of any future drive electronics into the substrate thus reducing interconnects at the final stage of processing. The principle of this has been demonstrated to produce an Optoelectronic Integrated Circuit (OEIC)[8]. Over and above these points, the use of a silicon substrate and

an Al electrode allows the use of well proven standard silicon processing techniques. These include metalisation, photolithography and etching.

Surface
Emission

Transparent Top Electrode

Top Insulator

Phosphor

Bottom Insulator

Silicon Substrate

Bottom Electrode

Top Electrode

Top Insulator

Phosphor

Bottom Insulator
Transparent Electrode

Transparent Substrate
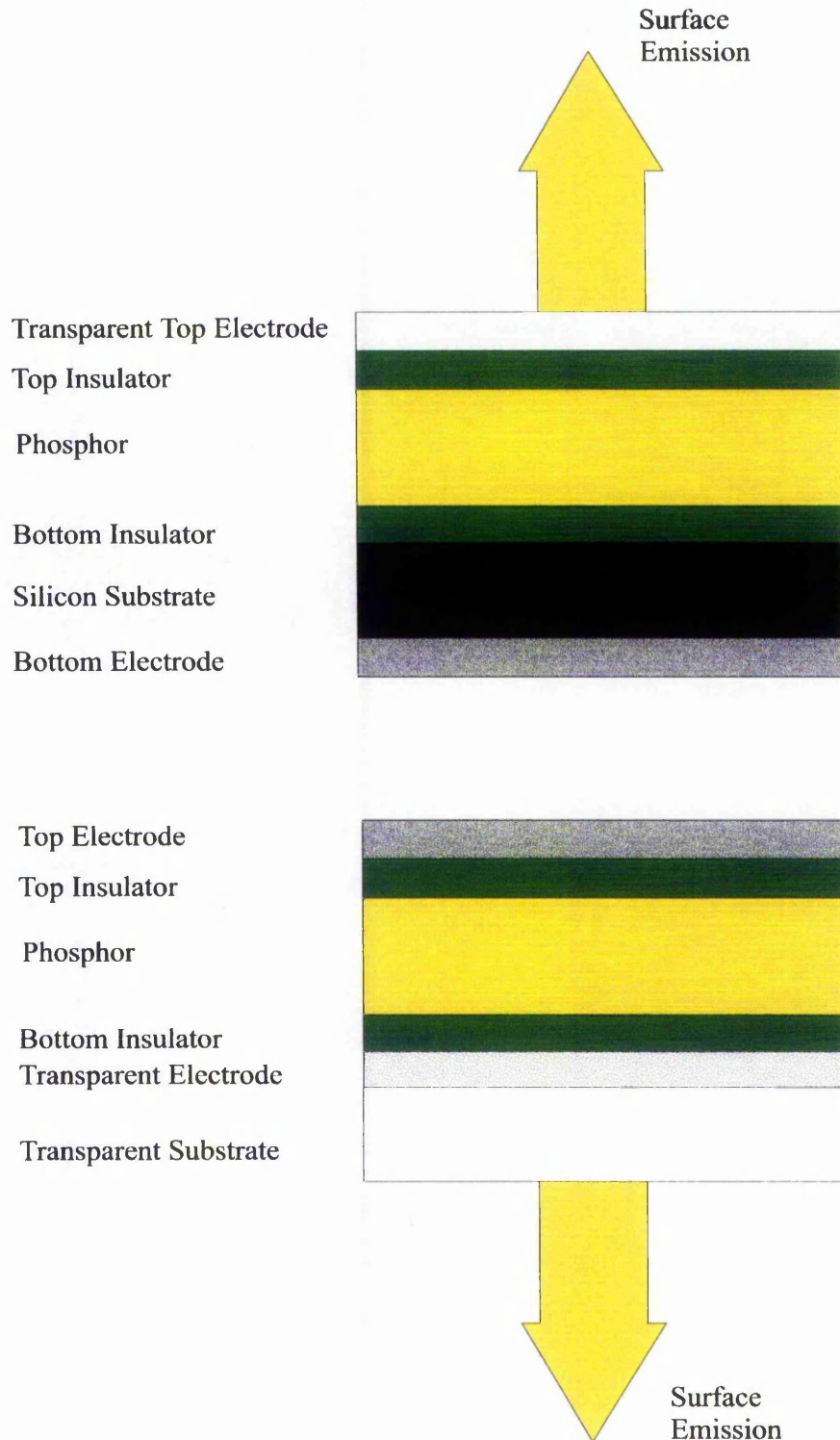
Surface
Emission

Figure 4.3 Typical AC TFEL device structures utilising surface emission

To form the LETFEL structure shown schematically in figure 4.2, an etching process is required to remove the electroluminescent layers within the aperture region. This etching procedure is critical to effective LETFEL operation and is the basis of a parallel Ph.D. investigation, where the efficiency of light outcoupling as a function of the etching process is being examined. The aim of that Ph.D. is to optimise the shape of the emitting aperture by the etching of some or all of the insulator and/or phosphor layers in the aperture region. Three processing techniques have been considered to etch the materials. They are 1) Reactive Ion Etching (RIE), Wet chemical etching and 3) Ion Milling. RIE has been disregarded, since an etch for the current insulator layer, Y_2O_3, has proved difficult to identify. Wet chemical etching has been previously shown to reduce the lifetime of a LETFEL device[9]. Ion Milling has been shown to be successful in the etching of LETFEL device materials[10]. Hence, ion milling has been chosen for the parallel investigation.

Detailed in this chapter therefore is the initial fabrication route and the final fabrication route developed by the author required to incorporate the changes which enable the ion milling of the aperture region in a LETFEL device. Full details of the ion milling investigation have been reported by S. Barros[11]. The reader is directed to this paper for full details of Ion Milling and the effect on the profile of the aperture.

4.2 Initial Fabrication Route

The fabrication route is defined as the series of stages required to produce a set of high resolution LETFEL displays on a standard 4" Si wafer. Figure 4.4 shows an overall summary of the five main stages required to fabricate a LETFEL device. The initial fabrication route has been developed over many years from a route defined by R. Stevens in 1994[12], which was used to produce the series of LETFEL devices reported previously[13]. This route utilised micro-mirror fabrication at AMPi, Taiwan. However, problems with these micro-mirror base layers were encountered due to a miss-match in mask aligners at AMPi and NTU. This caused minor alignment problems. Specifically, it was not possible to align more than 75% of the device structures on each substrate. The remaining devices showed misalignment of up to 3 μm. Due to these alignment problems, the yield of LETFEL devices from each substrate was reduced to a maximum of 75% before any processing was carried out. Concurrent to this, shipping of a substrate prior to final fabrication increases the possibility of contamination and hence increases the risk of device failure. Potential contamination of the substrate is a large problem since a 1μm particle of dust would cause device failure and hence a further drop in yield. Consequently, for this investigation, the route defined by R. Stevens[12] has been updated to eliminate the aligner miss-match and to reduce shipping time. Figure 4.6 shows in detail each stage in the initial fabrication route with a diagram of an aperture and bond pad at each point. Details of each of these processes are given below.

Micro-Mirror Fabrication
The basis of all high resolution LETFEL devices
are the 1.5 µm high micro-mirrors.
These are fabricated from SiO_2 and have a face
Angle of 45 − 55 degrees

LETFEL Device Material Deposition
All five of the thin films of the
insulator/phosphor stack are deposited by RF
Magnetron Sputtering.

Metalisation, Definition and Passivation
To electrically address each pixel in a display an
electrode has to be deposited and patterned. Also
at this stage a passivation layer is deposited to
provide environmental protection for the device
materials.

Contrast Enhancement
To increase the contrast and hence the definition
of the pixels a layer of black polyimide is
deposited and patterned.

Dicing and Wire Bonding
Each substrate is capable of accommodating well
over 100 individual displays. To enable final
use, each display is diced from the wafer. To
allow electrical addressing each pixel is then
wire bonded to its PCB or support substrate.

Figure 4.4 Overview block diagram of the five main processing stages in the
fabrication route of high resolution LETFEL devices.

4.2.1 Micro-mirror Fabrication

The fabrication of the micro-mirrors is the first and arguably one of the most important stages in the whole process. If the micro-mirrors are unsatisfactory, further processing is pointless.

The micro-mirrors are 1.5 μm high and 3 μm wide at the base. The face angle is 45 to 55° to the vertical. The first fabrication route involved the fabrication of the micro-mirrors at AMPi, Taiwan. Due to the aligner miss-match a new source of micro-mirrors was sought. The National Microelectronics Research Centre (NMRC), Cork has defined a route to produce high quality, reproducible mirrors, as shown in figure 4.5. The mask aligner utilised at NMRC is compatible with the one in use at NTU, hence the fabrication of the micro-mirrors were contracted to NMRC. Stages 1 to 4 in figure 4.6 summarise the process to form the micro-mirrors.

Figure 4.5 SEM Photograph of 1.5 μm high by 3 μm wide micro-mirrors supplied by NMRC.

4.2.2. LETFEL Device Material Deposition

The barrier layer LETFEL device is composed of a series of five thin films of alternating insulator and phosphor, shown in figure 4.1. The phosphor films are ZnS:Mn with the insulators currently being Y_2O_3. Both of these thin film materials are deposited by RF magnetron sputtering at NTU. The thickness of all of the thin films is monitored by the interferometric technique described in section 2.5.1. The optimisation of the deposition of Y_2O_3 and ZnS:Mn thin films is detailed elsewhere[7]. A summary of all of the deposition parameters is given in table 4.1.

Material	Deposition Temp. /°C	Concentration of Ar /%	Total Pressure /mT	RF Power /Watts cm^{-2}	Deposition Rate /nmhr^{-1}
ZnS:Mn	200	100	3	2.18	320
Y_2O_3	200	100	3	2.62	86

Table 4.1 The RF magnetron deposition conditions for the LETFEL device materials.

Immediately prior to any thin film deposition, the substrate with the micro-mirrors is subjected to a dehydration bake at 700 °C for half an hour under vacuum in the LETFEL deposition chamber. After cooling for one hour to 200 °C, the series of five thin films of the LETFEL stack are deposited (stage 5 figure 4.6). Post deposition annealing at 700 °C for 1 hour in vacuum is carried out for optimum device performance[7]. After a 1 hour cool to room temperature the substrate is removed from the deposition chamber to a vacuum storage jar for transport to

Qudos Ltd at the Rutherford Appleton Laboratory, Oxford, for the final fabrication stages.

4.2.3 Metalisation, Electrode Definition and Passivation

As stated earlier, Al is currently utilised as the electrode in the LETFEL device structure. The metalisation is a two stage process with the deposition of a passivation layer in between. The need for the two levels of Al is due to the device performance and the ability to bond to the device. Bonding requires at least 800 nm of Al, however, if this thickness was used on the active area of the device the performance of the device is reduced[14]. Therefore, a thin layer, up to 300 nm, of Al is deposited on the active area and a thicker, 800 nm, Al film is deposited in the bond pad region to allow bonding. Tables 4.2, 4.3 and 4.4 detail all the parameters for the deposition, photolithographic patterning and RIE respectively of both the Al electrode and Si_3N_4 passivation layers.

Material	Deposition Method	Deposition Temp. /°C	Gases	Gas Flow /sccm	Total Pressure /mT	Power /Watts
Al	DC Sputtering	Room Temp.	Ar	10	5	5000
Si_3N_4	PECVD	300	SiH_4 NH_3	120 18	320	83

Table 4.2 Deposition parameters for Aluminium and Silicon Nitride at Qudos Ltd

Step	Process	Details
1	Dehydration bake of the substrate	120 °C 30 min
2	Adhesion Promoter (HMDS type APX-1K) and bake	APX - 1K 145°C for 45 min. (Automatic, standard process at Qudos)
3	Photoresist (PR) spin coat	Photoresist:-Dyed JSR Positive 2.5 ml 3000 rpm 1 min
4	Pre-bake temp. / time.	100 °C 1 min
5	Exposure to Ultra Violet (UV) Light.	Mask Aligner:-SET 10 sec 23 mW/cm
6	Post Expose Bake	100 °C 1 min
7	PR Development.	Developer:-TMA238WA 40 seconds
8	De-ionised water rinse.	1 min
9	Hardbake Temp/Time	120 °C 30 min
10	PR descum.	O_2 Plasma 100 mT 40 W 30 sec
11	RIE	Conditions dependant on the material requiring etching. See table 4.4 for example
12	PR Removal	O_2 Plasma 100 mT 40 W 15 min

Table 4.3 Photolithographic Process Parameters.

Material	Gases	Flow /sccm	Pressure /mT	Power /Watts
Al	$SiCl_4$	40	70	160
Si_3N_4	CHF_3	45	100	300
	O_2	10		

Table 4.4 Reactive Ion Etching (RIE) conditions for Aluminium and Silicon Nitride at Qudos Ltd.

The first level metalisation, 300 nm of Al, is deposited by DC magnetron sputtering. A photolithographic process is utilised to define a protective photoresist mask in the shape of the electrodes. RIE is then used to etch the unrequired Al. This is mainly on the aperture region and between separate displays. Al must be removed from the aperture region to enable the light to be reflected by the underlying micro-mirror.

Next, the 300 nm of Si_3N_4 passivation is deposited by Plasma Enhanced Chemical Vapour Deposition, PECVD[15]. The role of the passivation is to protect the device materials from any environmental conditions. A via hole is required in the Si_3N_4 to allow electrical contact between the first and second level metalisation levels. Therefore, a second photolithographic step is used followed by an RIE process to open via holes.

Finally, the second level of metalisation, 800 nm Al, is deposited, again by DC magnetron sputtering. The final photolithographical stage and RIE is utilised to remove the thicker Al except in the bond pad region.

The above processes form stages 6 to 14 in the fabrication route detailed in figure 4.6. All of these processes are carried out by the author utilising the mini-fab facility at Qudos Ltd.

4.2.4 Contrast Enhancement

Due to the nature of the Al electrodes, any ambient light is reflected hence reducing contrast. Also due to the waveguide nature of the LETFEL devices, light spreads from the edge of the electrodes. This decreases the overall contrast and aesthetic appearance of the display. A solution to these problems is to deposit a film of black polyimide over the displays and remove it over the aperture and bond pad regions by chemical etching. This etching allows the light to escape in

the aperture region and access the bond pad. Figures 4.7 and 4.8 show the same device before and after the polyimide process. It can be observed that the contrast and definition are enhanced with the addition of polyimide. The full deposition and processing techniques for the polyimide film are detailed in table 4.5 and this process makes up stage 15 in the fabrication route in figure 4.6.

Step	Process	Details
1	Clean Substrate	Rinse in De-Ionised Water for 1 min
2	Dehydration bake of the substrate	170 °C 2 min
3	Adhesion Promoter (HMDS type APX-1K) and bake	APX - 1K 2 Drops Spin 2500 rpm for 10 sec. Bake 170 °C for 20 sec.
4	Deposit Polyimide (DARC 300)	2.5 ml by dropper, spin 5000 rpm for 10 sec
5	Polyimide Bake	Soft Bake 90 °C for 1 min β Bake 167 °C for 1 min
6	Photoresist (PR) spin coat	Photoresist:-Dyed JSR Positive 2.5 ml 3000 rpm 1 min
7	PR Soft bake	100 °C 1 min
8	Exposure to Ultra Violet (UV) Light.	Mask Aligner:-Cannon PLA 500 Automatic Light Integral = 500
9	Post Expose Bake	100 °C 1 min
10	PR Development.	Developer:- AZ 326 1 min
11	De-ionised water rinse.	1 min
12	Strip PR	Brewer Safestrip 1 min
13	Hard Bake	230 °C 60 min.

Table 4.5 Stages in the deposition and processing of the polyimide contrast layer.

(a)

34 um
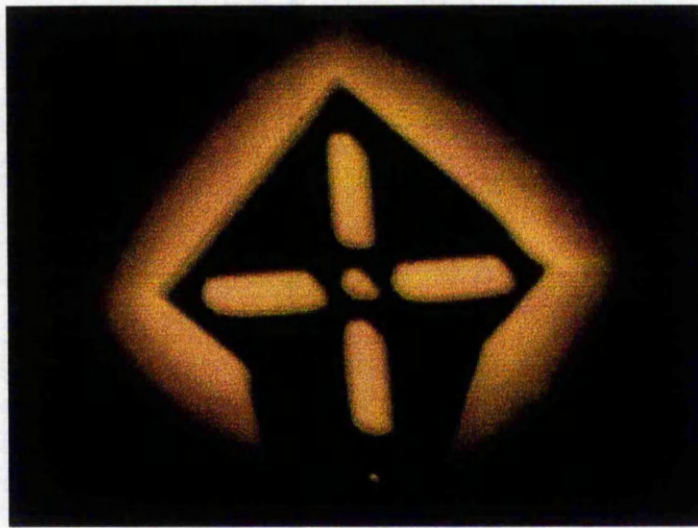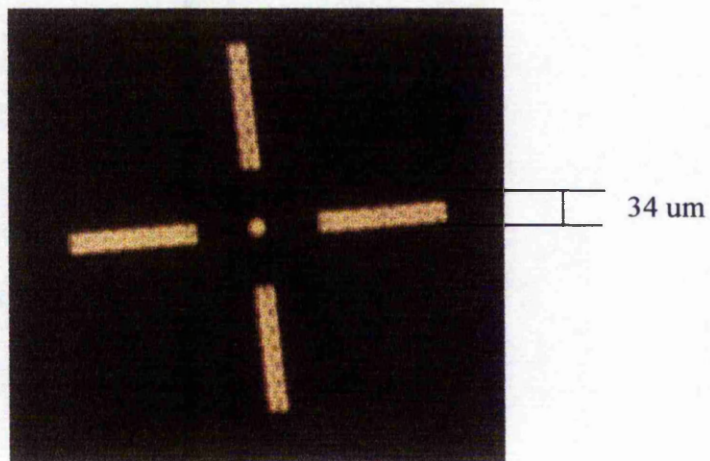
(b)

Figure 4.7a Cross of a device prior to polyimide deposition. (b) The same device after polyimide deposition, illustrating the improvement in contrast.

4.2.5 Dicing and Wire Bonding

The 4" substrate utilised for LETFEL devices can accommodate well in excess of 100 individual displays of dimension 4 mm by 4 mm. Figure 4.8 is such a substrate, it has 115 individual fixed legend displays and 400 test devices. Each display is designed to be mounted into dedicated optics. The substrate is consequently diced to produce individual display die. The displays are then mounted onto ceramics and each pixel is electrically connected to the external circuitry via wire bonding. Both the processes of dicing and wire bonding are standard Si techniques. A Sola Basic Tempress 602 is utilised for dicing and a Kulicke and Soffa 4123 wedge bonder is utilised for the wire bonding.

Prior to dicing the substrate is coated with a layer of photoresist to protect the devices from the small pieces of Si generated during the dicing process. After dicing the photoresist is removed chemically in photoresist remover (AZ100). The displays are then mounted on the ceramics and each connection is wire bonded. The completed displays are then mounted into the optical system required for the application they were designed for. Figure 4.9 is a photograph of a final display viewed through the optics of a Head Mounted Display System produced by Frazer Nash Research Ltd. This system is designed for use in leisure/sport activities such as scuba diving or hang gliding.
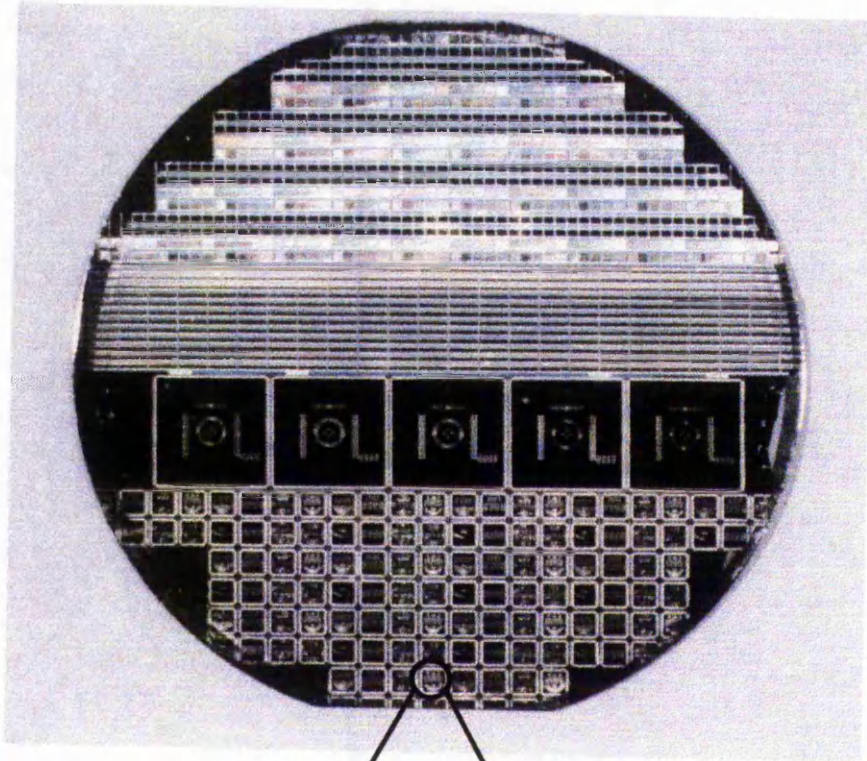
Figure 4.8   An example of a fully fabricated high resolution LETFEL device substrate
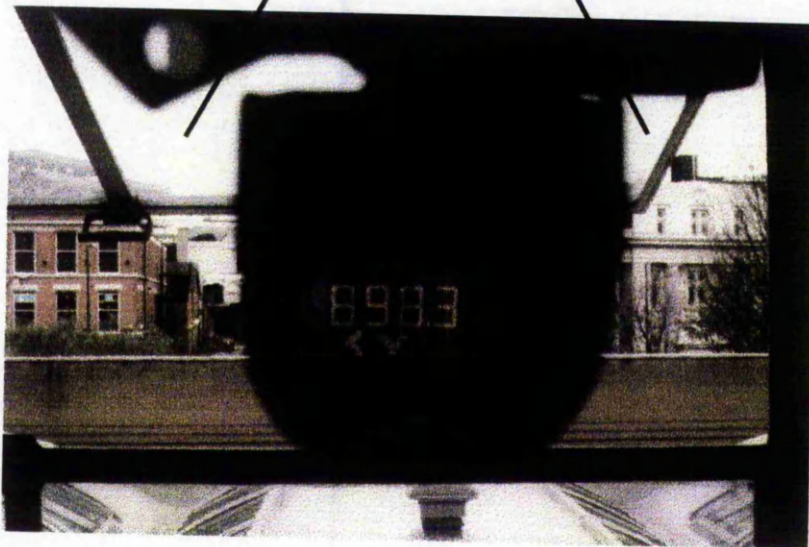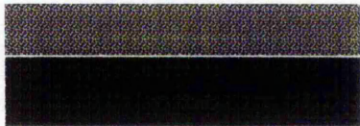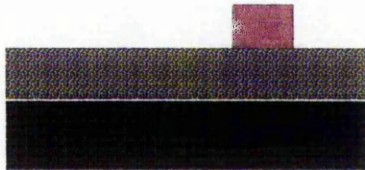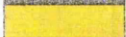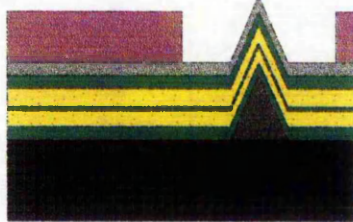
Figure 4.9 A LETFEL display device mounted in dedicated optics, viewed out of the laboratory window
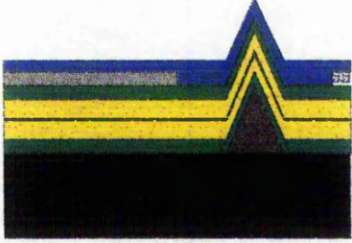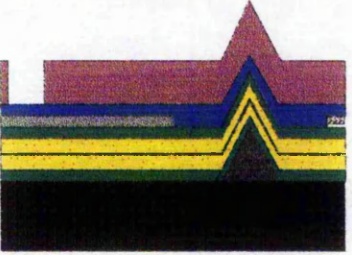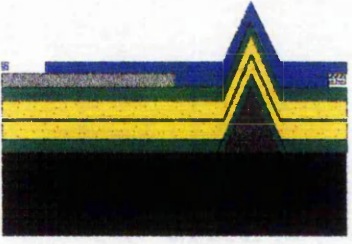
Figure 4.6 The initial fabrication route for the LETFEL device structure.
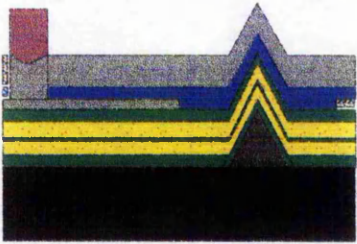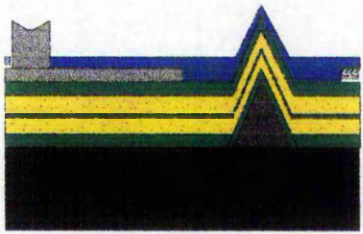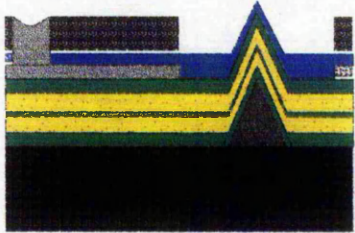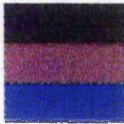
Process Number	Process Name / Location	Process Aim	Aperture Configuration
1	Plain Si Substrate (NMRC)	N -Type 2 - 6 Ohm/cm 100 ± 0.5 mm Diameter 525 ± 50 µm Thick	
2	Micro-mirror material deposition (NMRC)	Deposition of 1.5 µm SiO_2 utilising PECVD	
3	Micro-mirror definition (NMRC)	Photolithography to define the shape and location of the micro-mirrors	
4	RIE of Micro-mirrors and photoresist strip (NMRC)	RIE of SiO_2 to form mirrors with 45 - 55 ° side walls, then the photoresist mask is removed	

Aluminium
ZnS:Mn Phosphor
Insulator
SiO_2
Silicon

Polyimid
Photoresist
Si_3N_4

Process Number	Process Name / Location	Process Details	Aperture Configuration
5	LETFEL material deposition (NTU)	Deposition of 5 layers of insulator and phosphor thin films and post deposition annealing	
6	First level metalisation (Qudos)	Deposition of first layer of aluminium	
7	First layer metal definition (Qudos)	Photolithography mask to define the electrode and hence the aperture shape and size	
8	First layer metal etch (Qudos)	RIE of first layer metal and removal of photoresist	

Aluminium		Polyimid	
ZnS:Mn Phosphor		Photoresist	
Insulator		Si_3N_4	
SiO_2			
Silicon			

Process Number	Process Name / Location	Process Details	Aperture Configuration
9	Passivation (Qudos)	Deposition of Si_3N_4 to seal in the device layers and give environmental protection	
10	Passivation definition (Qudos)	Photolithography to define bond pad region on the device	
11	Passivation etch (Qudos)	RIE of Si_3N_4 in the bond pad region to give access to the electrode and removal of photoresist	
12	Second level metalisation deposition (Qudos)	Deposition of Aluminium to thicken bond pad region to enable wire bonding	

Aluminium
ZnS:Mn Phosphor
Insulator
SiO_2
Silicon

Polyimid
Photoresist
Si_3N_4

Process Number	Process Name / Location	Process Details	Aperture Configuration
13	Second level metal definition (Qudos)	Photolithography to define bond pad region on the device	
14	Second level metal etch (Qudos)	RIE of second level metal and removal of photoresist	
15	Contrast layer deposition and patterning (NTU)	Deposition and patterning of a black polyimide contrast layer	

Aluminium
ZnS:Mn Phosphor
Insulator
SiO$_2$
Silicon

Polyimid
Photoresist
Si$_3$N$_4$

4.3 Changes Required To Facilitate Ion Milling

Any shaping of the aperture by ion milling must occur between stages 8 and 9 in the fabrication route as detailed in figure 4.6. During this process a mask is required so that only the aperture is etched. Ideally, the photoresist used to define the electrodes would be used as the mask for the aperture etch. After an initial investigation it was determined that the photoresist polymerised during the process of ion milling which prevented the removal of the photoresist after the ion milling process. A solution to this problem was to utilise a sacrificial mask made of another material which could be removed following the ion milling. Ideally, the chosen material would be deposited and patterned using standard Si techniques. During the ion milling process it would be this material which would be sacrificially etched away, thus protecting the device structure underneath. Silicon Dioxide (SiO_2) and Silicon Oxynitride (SiO_xN_y) were chosen for investigation as suitable sacrificial mask materials. Both of these materials are used in standard Si processing techniques, hence no calibration of the deposition or RIE processes was required. Full details of the deposition and etching conditions of these materials is given in tables 4.6 and 4.7 respectively.

Material	Deposition Method	Deposition Temp. /°C	Gases	Gas Flow /sccm	Total Pressure /mT	Power /Watts
SiO_2	PECVD	300	SiH_4 N_2O	25 500	300	83
SiO_xN_y	PECVD	300	SiH_4 NH_3 N_2O	15 50 160	320	83

Table 4.6 Deposition parameters for SiO_2 and SiO_xN_y by PECVD at Qudos Ltd

Material	Gases	Flow /sccm	Pressure /mT	Power /Watts
SiO_xN_y	CHF_3	45	100	300
SiO_2	O_2	10		

Table 4.7 RIE parameters for SiO_2 and SiO_xN_y at Qudos Ltd

The initial stage of the investigation was to determine any effect on the device performance by the deposition of the sacrificial mask or in fact if there was any reaction between the aluminium and the mask material.

Initial test devices were fabricated as shown in figure 4.10. The sacrificial mask was deposited and etched using the conditions in tables 4.6 and 4.7. The devices were then Ion Milled for 5 min. The ion milling was carried out using the conditions in table 4.8, supplied by S. Barros[11], in a Veeco 10" Micro Etch. The excess sacrificial mask was then removed by RIE. A previous experiment showed that this RIE technique does not etch Y_2O_3.

Sacrificial Mask

Aluminium Electrode
Y₂O₃ Insulator
ZnS:Mn Phosphor
Y₂O₃ Insulator

Silicon Substrate

Aperture
Awaiting
Ion Milling
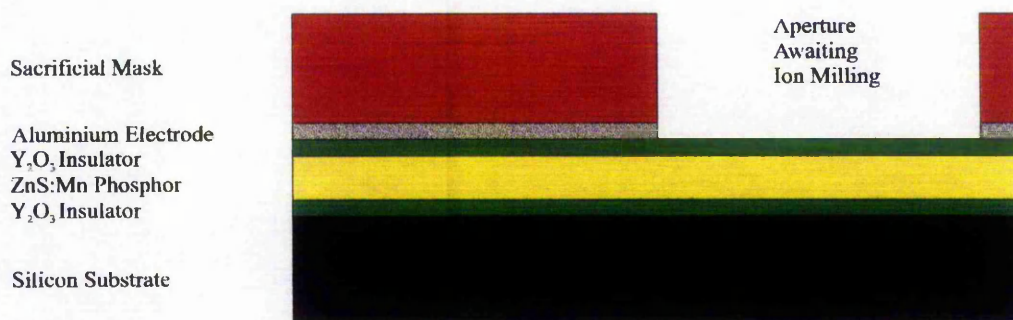
Figure 4.10 Device Structure With Sacrificial Mask Awaiting Ion Milling. After

Ion Milling the sacrificial mask was removed by RIE prior to characterisation.

Etch Gas	Pressure / mT	Beam Current /mA cm^{-2}
Ar	2.4	500

Table 4.8 Test Ion Milling conditions for the Veeco 10" Micro Etch.

On testing of these devices two problems occurred. Firstly, the devices electrically broke down at a voltage lower than the threshold voltage, i.e. no EL was observed. Secondly, wire bonding to the bond pad region was impossible. SEM analysis of a bond pad region revealed "spikes" of a material protruding up from the Al electrode, as seen in figure 4.11. Wire bonding requires a flat surface of pure metal for success. These spikes are consequently preventing bonding. As the spikes are observed to come up from the electrode, it could be assumed that they also protrude down into the top insulator, thus reducing the dielectric strength of the insulator layer and leading to the observed early breakdown effects.
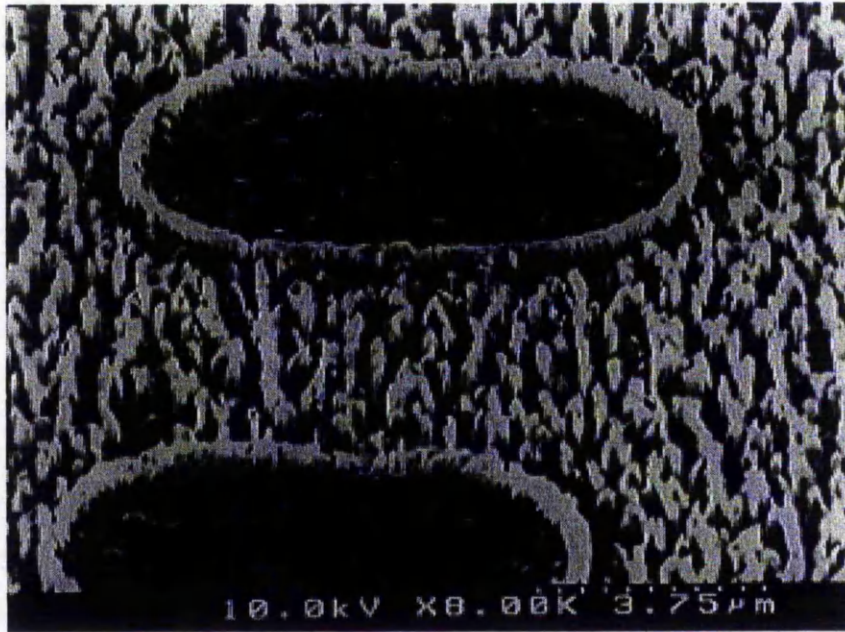
Figure 4.11 SEM of Al electrode with "spikes" protruding up from the surface.

The spikes in figure 4.11 could be pure aluminium or possibly aluminium oxide. If they are Al then they could be formed by the thermal expansion and reflowing of the Al during heating. Aluminium has a thermal expansion coefficient of 25 × 10^{-6} °C^{-1} [4]. Therefore at a raised temperature 300 °C, for example, the volume of Al increases. The extra volume could reflow to form the spikes. This reflow phenomenon has been previously utilised to form via holes during multi-layer ASIC production[16]. If no reflowing occurs there would be a build up of internal stress in the Al. This could lead to delamination of the film. No delamination of the Al film was observed, therefore, it may be assumed that reflow is the mechanism responsible for the spikes. The heating, which could cause reflow, could be generated either during the deposition of the sacrificial mask material, or

due to any substrate heating during the ion milling. The sacrificial mask materials are deposited at 300 °C.

If the spikes are aluminium oxide they could be formed by a chemical reaction between the aluminium and the oxygen from the nitrous oxide during the deposition of the sacrificial mask material. Aluminium has a high affinity towards oxygen, so the Al would readily react with any oxygen in the atmosphere, especially at a raised temperature, to form Al_2O_3.

To examine this effect further, 300 nm of Al was deposited onto a Si substrate. The sacrificial mask materials were then deposited and patterned, again utilising the conditions detailed in tables 4.6 and 4.7 respectively. The Al was then patterned by RIE detailed in table 4.4. The samples were split into two and the mask material was removed by RIE from half of each sample. SEM analysis revealed the presence of the spikes on all of the samples, a further example is shown in figure 4.12. It may thus be concluded that the spikes were formed during the sacrificial mask material deposition and patterning and not during the ion milling process.
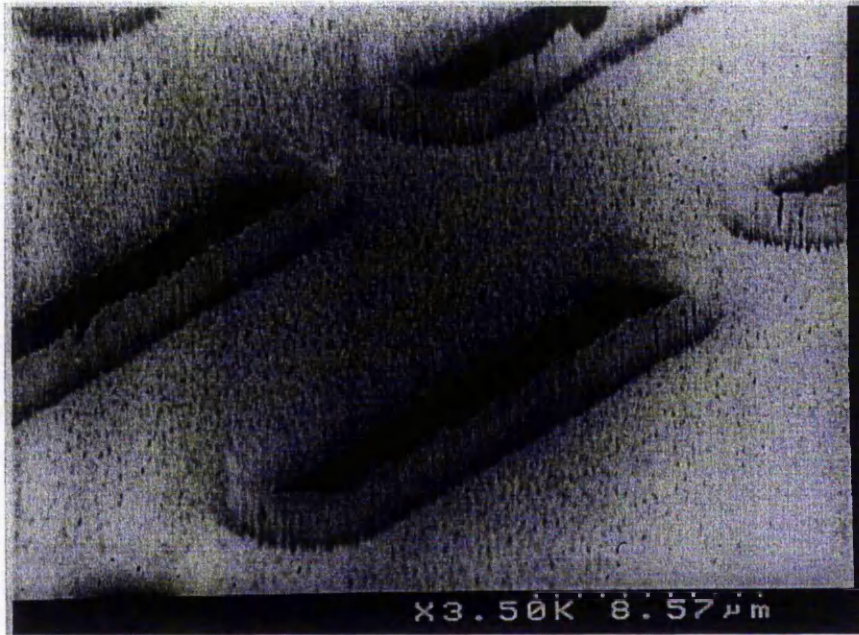
Figure 4.12 Further SEM evidence of the "spikes" formed during the deposition and RIE of the sacrificial mask material.

As seen in figures 4.11 and 4.12, under SEM analysis the spikes appear to be brighter than the surrounding Al. This phenomenon is characteristic of a dielectric material, due to it's ability to store the charge from the electrons in the SEM beam. If the material is metallic no charge would be stored as the sample is electrically grounded during SEM inspection. It may be concluded that the spikes are Al_2O_3. However, the process of spike formation could in fact be two fold. With Al expansion due to the heating during the sacrificial mask processing and a reaction with the O_2 present in the SiO_2, SiO_xN_y or in fact the Y_2O_3 to form Al_2O_3.

To address this, it was concluded that a barrier was required between the aluminium and the insulator and the aluminium and the sacrificial mask. In ASIC fabrication aluminium electrodes are typically sandwiched between two thin films

of Titanium/Tungsten (Ti/W)[17] which could be used here to provide the barrier. The deposition and RIE of Ti/W is a standard process and therefore required no optimisation of the deposition or RIE techniques before use in the LETFEL device structure. Table 4.8 details both the deposition and RIE conditions for the Ti/W thin films. Ti/W is a hard refractory metal. If successful it would form a physical barrier to prevent the spikes penetrating either the insulator or sacrificial mask films. It was also decided to RIE the first level metalisation level prior to the sacrificial mask deposition, to reduce any thermal expansion effects. Ti/W could not be utilised alone as it's resistivity is 6.5×10^{-7} Ωm^{-1} [17] which is too high to form a suitable electrode, compared to 2.417×10^{-8} Ωm^{-1} for Al[4]. Also Al in the bond pad region is required to enable wire bonding.

Process	Gases and Flow /sccm	Pressure /mT	Power /Watts	Rotation /revs min^{-1}	Deposition / Etch Rate /nm min^{-1}
Ti/W Deposition	Ar - 10	5	2000	5	20
Ti/W RIE	CF$_4$ - 40 O$_2$ - 10	70	120	-	85

Table 4.8. The deposition and RIE conditions for Ti/W at Qudos Ltd.

To examine the effect of using a Ti/W/Al/Ti/W electrode, test devices were fabricated utilising the fabrication route detailed in section 4.2, with the addition

of the stages shown in figure 4.13 replacing stages 6 to 8 in figure 4.6. Test ion milling for five minutes was again utilised. Use of this refined electrode fabrication resulted in reliable devices. That is, devices exhibiting a sharp luminance - voltage characteristic, a high luminance at Vth + 50 V, a lifetime in excess of 12 hours on the probe station and allowing successful wire bonding. To enable wire bonding the Ti/W was removed in the bond pad region and a second layer of 800 nm of Al was deposited in this region. Figure 4.14 shows an example of a luminance - voltage characteristic from a device fabricated using this refined electrode definition.
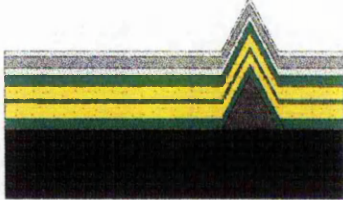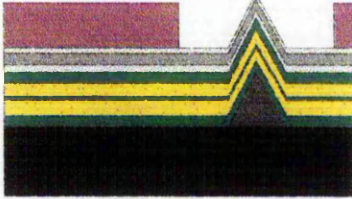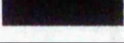
Process Number	Process Name / Location	Process Details	Aperture Configuration
6	First level metalisation (Qudos)	Deposition of tri-layer first level metalisation	
7	First layer metal definition (Qudos)	Photolithography mask to define the electrode and hence the aperture shape and size	
8	First layer metal etch (Qudos)	RIE of tri-layer first level metalisation and removal of photoresist	
9	Sacrificial mask deposition (Qudos)	Deposition of 2µm thick sacrificial mask	

Aluminium		Polyimid	
ZnS:Mn Phosphor		Photoresist	
Insulator		Si_3N_4	
SiO_2		Sacrificial Mask	
Silicon		Ti/W	

Figure 4.13 The replacement stages in the initial fabrication route to enable Ion Milling.

Process Number	Process Name / Location	Process Details	Aperture Configuration
10	Sacrificial mask definition (Qudos)	Photolithography mask to define the sacrificial mask	
11	Sacrificial mask etch (Qudos)	RIE of sacrificial mask and removal of photoresist	
12	Ion Milling (Qudos)	Definition of aperture profile. (Only test ion milling carried out in this investigation)	

Aluminium		Polyimid	
ZnS:Mn Phosphor		Photoresist	
Insulator		Si_3N_4	
SiO$_2$		Sacrificial Mask	
Silicon		Ti/W	

Figure 4.13 The replacement stages in the initial fabrication route to enable Ion Milling.

Figure 4.14 L-V Characteristic from initial test device fabricated in section 4.3

4.4 Final Fabrication Route

As detailed in section 4.3 the problems with metalisation and sacrificial mask deposition have been addressed. However, SEM analysis of the final device fabricated in section 4.3 showed a 1.5 μm miss-alignment in the processing, shown in figure 4.15. This is undesirable since a progressive miss-alignment repeated throughout the alignment processes would result in unusable devices. Even minor miss-alignment is a problem, since the emitting apertures are only 3 μm across. Therefore a reduction in the number of masking procedures is desirable, both for the reduction in miss-alignment and to save processing time.
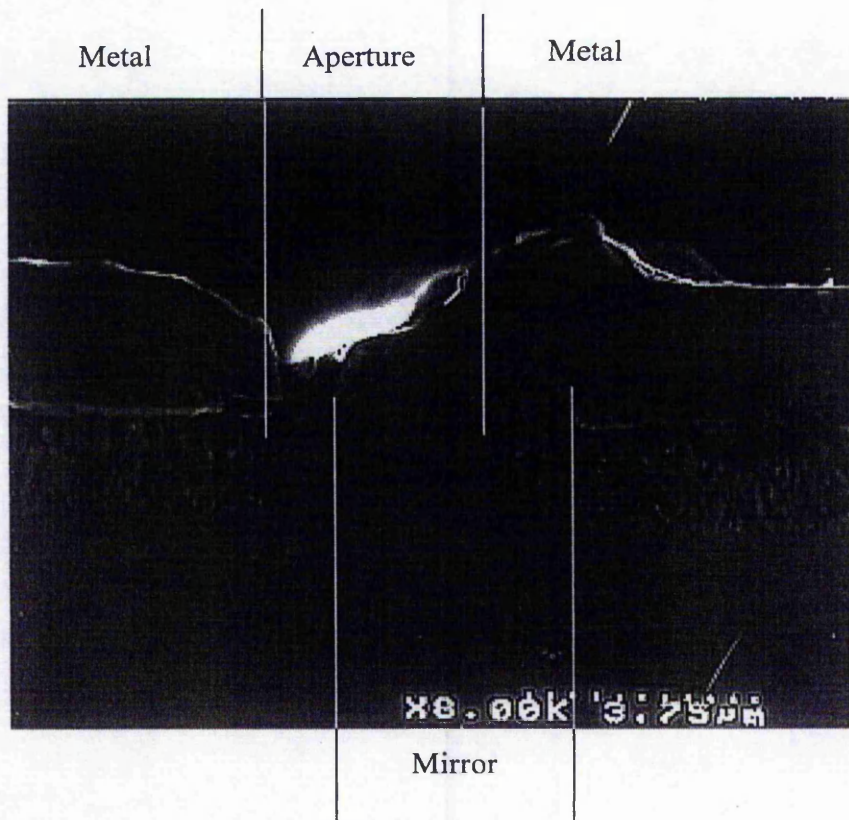
Figure 4.15 SEM cross-section of a micro-mirror aperture showing misalignment during processing.

It has been proposed in section 4.3 to define the electrodes before the deposition and patterning of the sacrificial mask, due to the possible problems caused by the thermal expansion of the Al during the deposition of the sacrificial mask. The same mask is then utilised to pattern the metals and the sacrificial mask. If the sacrificial mask could be deposited before the electrodes are etched it would consequently reduce the masking steps by one. A further advantage is due to the RIE selectivity's of the materials used. Table 4.9 shows the etch rates of the five

materials involved at this stage of the fabrication route under the two different RIE conditions utilised. This table shows that under the RIE conditions for the etching of the Al, none of the other materials in the table are etched. Also under the RIE conditions for the etching of the SiO_2, SiO_xN_y and Ti/W, the Al is not etched. The Y_2O_3 insulator is not etched under any of these RIE conditions. Therefore a degree of over etching can be incorporated to ensure the full etching of the materials required.

Material	Etch Rate Under Al Etch Conditions /nm min^{-1}	Etch Rate Under Oxide Etch Conditions /nm min^{-1}
Al	40	0
SiO_2	0	44
SiO_xN_y	0	44
Ti/W	0	10
Y_2O_3	0	0

Table 4.9 RIE etch rates for the materials involved in the processing at Qudos Ltd. Note the selectivity's, enabling an amount of over etching.

To determine if thermal expansion of the Al was indeed a problem and if a single masking procedure would be adequate, two devices were fabricated. The first utilised the double masking procedure detailed in section 4.3 and the second utilised the single masking procedure described above. Both of these device were successful, i.e. they were reliable and bonding was successful. A comparison of the luminance-voltage characteristic of these devices is given in figure 4.16. The threshold voltage, steepness of response and final luminance is comparable for both sets of devices. Therefore the single masking route was adopted. The final full fabrication route for a LETFEL device structure is shown in figure 4.17. This

route allows the fabrication of successful devices with the opportunity of any aperture shaping and optimisation.
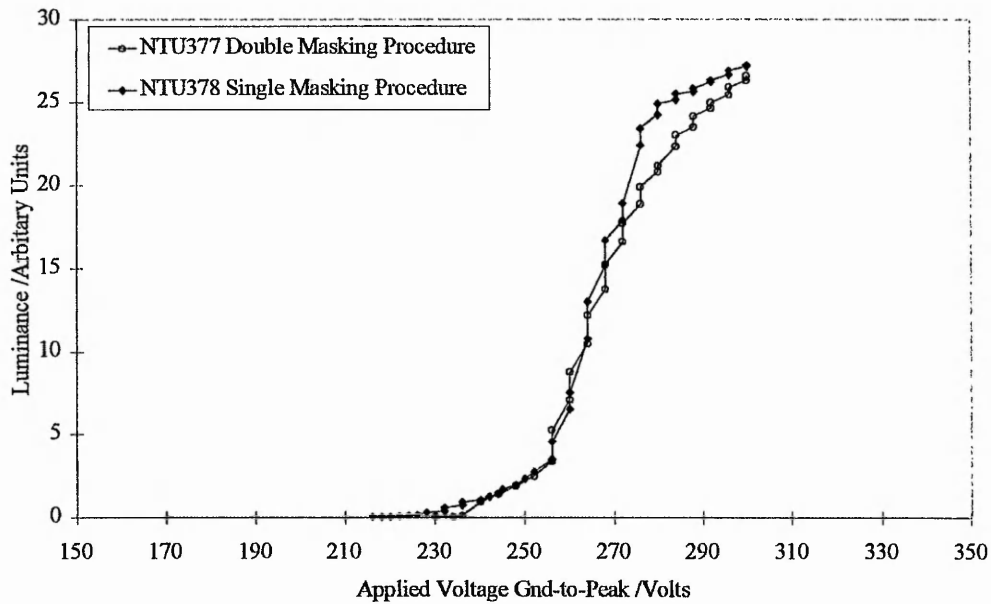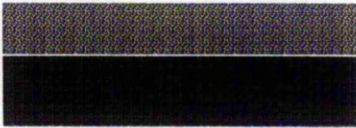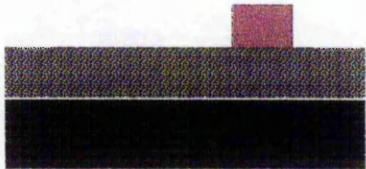
Figure 4.16   Comparison of L-V characteristics of two identical devices. NTU377 was fabricated with the double masking procedure described in section 4.3 and NTU378 was fabricated with a single masking procedure detailed in section 4.4.

Process Number	Process Name / Location	Process Aim	Aperture Configuration
1	Plain Si substrate (NMRC)	N -Type 2 - 6 Ohm/cm 100 ± 0.5 mm Diameter 525 ± 50 µm Thick	
2	Micro-mirror material deposition (NMRC)	Deposition of 1.5 µm SiO_2 utilising PECVD	
3	Micro-mirror definition (NMRC)	Photolithography to define the shape and location of the micro-mirrors	
4	RIE of micro-mirrors and photoresist strip (NMRC)	RIE of SiO_2 to form mirrors with 45 - 55 ° Side walls, then the photoresist mask is removed	

Aluminium		Polyimid	
ZnS:Mn Phosphor		Photoresist	
Insulator		Si_3N_4	
SiO_2		Sacrificial Mask	
Silicon		Ti/W	

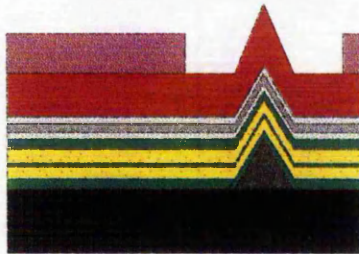Figure 4.17 The final fabrication route for the LETFEL device structure.
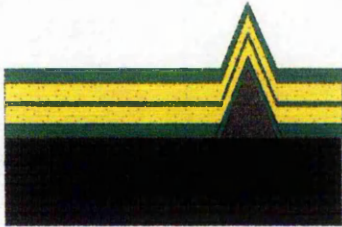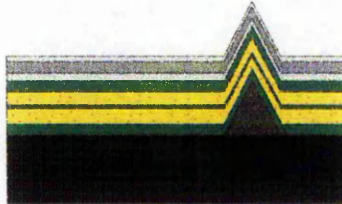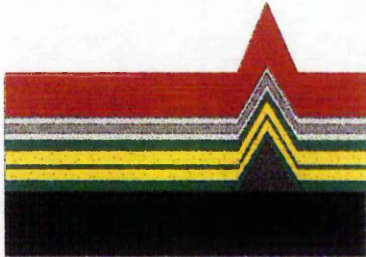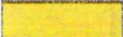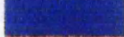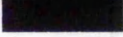
Process Number	Process Name / Location	Process Details	Aperture Configuration
5	LETFEL material deposition (NTU)	Deposition of 5 layers of insulator and phosphor thin films and post deposition annealing	
6	First level metalisation (Qudos)	Deposition of tri-layer first level metalisation	
7	Sacrificial mask deposition (Qudos)	Deposition of 2µm thick sacrificial mask by PECVD	
8	Sacrificial mask and first layer metalisation definition (Qudos)	Photolithography mask to define the sacrificial mask and electrode and hence the aperture shape and size	

Aluminium		Polyimid	
ZnS:Mn Phosphor		Photoresist	
Insulator		Si_3N_4	
SiO_2		Sacrificial Mask	
Silicon		Ti/W	

Figure 4.17 The final fabrication route for the LETFEL device structure.

Process Number	Process Name / Location	Process Details	Aperture Configuration
9	Sacrificial mask and first layer metal etch (Qudos)	RIE of sacrificial mask, first level metalisation and removal of photoresist	
10	Ion Milling (Qudos)	Definition of aperture profile. (Only test ion milling carried out in this investigation)	
11	Passivation (Qudos)	Deposition of Si_3N_4 to seal in the device layers and give environmental protection	
12	Passivation definition (Qudos)	Photolithography to define bond pad region on the device	

Aluminium		Polyimid	
ZnS:Mn Phosphor		Photoresist	
Insulator		Si_3N_4	
SiO$_2$		Sacrificial Mask	
Silicon		Ti/W	

Figure 4.17 The final fabrication route for the LETFEL device structure.

Process Number	Process Name / Location	Process Details	Aperture Configuration
13	Passivation etch (Qudos)	RIE of Si_3N_4 and Ti/W in the bond pad region to give access to the Al and removal of photoresist	
14	Second level metalisation deposition (Qudos)	Deposition of Aluminium to thicken bond pad region to enable wire bonding	
15	Second level metal definition (Qudos)	Photolithography to define bond pad region on the device	
16	Second level metal etch (Qudos)	RIE of second level metal and removal of photoresist	

Aluminium		Polyimid	
ZnS:Mn Phosphor		Photoresist	
Insulator		Si_3N_4	
SiO$_2$		Sacrificial Mask	
Silicon		Ti/W	

Figure 4.17 The final fabrication route for the LETFEL device structure.

Process Number	Process Name / Location	Process Details	Aperture Configuration
17	Contrast layer fabrication (NTU)	Deposition and patterning of a black polyimide contrast layer	

Aluminium		Polyimid		
ZnS:Mn Phosphor		Photoresist		
Insulator		Si₃N₄		
SiO₂		Sacrificial Mask		
Silicon		Ti/W		

Figure 4.17 The final fabrication route for the LETFEL device structure.

4.5 Experimental Procedure

To determine the full characteristics of a substrate of high resolution LETFEL devices and the success of the full fabrication route a series of substrates have been fabricated using the final route detailed in figure 4.17.

In summary, an initial substrate with micro-mirrors was produced by the NMRC. The barrier layer LETFEL device structure consisting of :-

Y_2O_3(300 nm)/ZnS:Mn(400 nm)/Y_2O_3(10 nm)/ZnS:Mn(400 nm)/Y_2O_3(300 nm)

was deposited by RF magnetron sputtering, full deposition parameters in table 4.1, and post deposition annealed at 700 °C at NTU.

The substrate was transported under vacuum to Qudos. Here the final processing was undertaken, including the metalisation, test ion milling and passivation. The

substrate was then returned to NTU for testing and deposition of the contrast layer.

4.6 Characterisation Procedure

There are three main types of characterisation of interest here. These are the luminance-voltage characteristic, (L-V), the uniformity of the L-V response across the substrate and the lifetime of the devices. From these measurements, the variance in the threshold voltage and maximum luminance can be obtained. Also a measure of both the steepness of response of the L-V characteristic and the yield of the devices can be determined.

All of the characterisations were undertaken utilising the main probe station facility at NTU. This is shown both pictorially and schematically in figure 4.18a and 4.18b respectively. In summary, a computer is utilised to control the output from a Tektronic AFG5501 function generator. This signal is amplified and applied across the device. The luminance is directly measured by the use of a Minolta LS110 luminance meter, which can be used to focus on a 1.1 mm diameter of the emitting area of the device. The 0 to 1V analogue output from the Minolta LS110 is also recorded by the computer. The applied voltage is increased in a series steps and at each step both the applied voltage and the measured luminance is recorded. The computer programme was written in Lab View in such a way to produce a data output file containing the voltage and luminance readings at each step of the characterisation. The computer programme also allows the variation of both the drive waveform and the frequency of that

waveform. This makes the system very versatile and multiple characterisations utilising different frequencies and/or drive waveforms without changing the sample are possible.
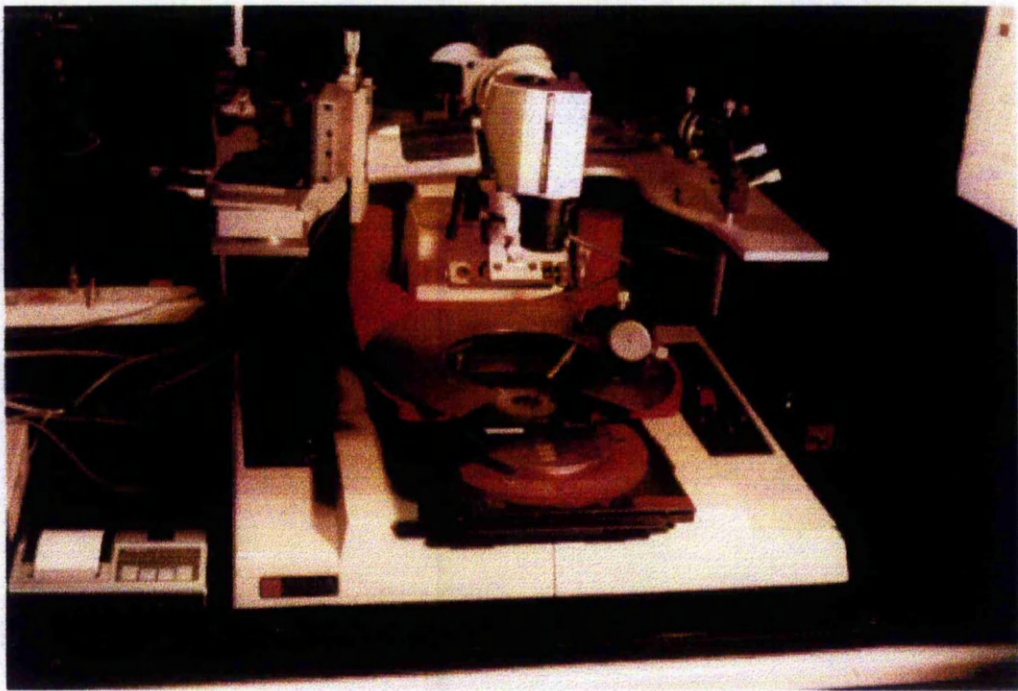
(a)
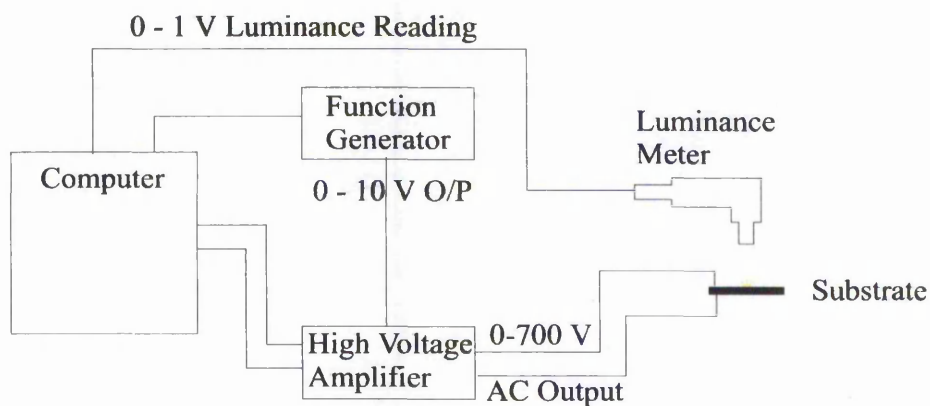
(b)

Figure 4.18 a and b. Probe station set-up used to characterise LETFEL devices.

4.7 Results

The results detailed in this section are the summary of a full characterisation of substrate NTU383. This substrate was fabricated utilising the full fabrication route detailed in figure 4.17.

The three sets of characterisation tests detailed in section 4.5 were undertaken. Figure 4.19 shows a typical L-V response from one of the set of ten devices characterised. It can be seen that the device exhibits a threshold voltage of 190 V and a switching voltage of 40 V. The switching voltage is defined as the additional voltage required to turn the device from the off state, just below Vth, to the on state, just above the top knee of the response. The uniformity of the threshold voltage, Vth, across the substrate was determined to be 180 V ± 5.5 %.

Figure 4.20 shows the uniformity of the maximum luminance across the substrate. This shows that the uniformity is ± 9 % for 80 % of the substrate.

The decay in luminance, the ageing, of a device for the first 90 minutes of operation is shown in figure 4.21. The luminance is seen to drop by 25 % in the first 30 min and then only by a further 18 % of the next 60 min.
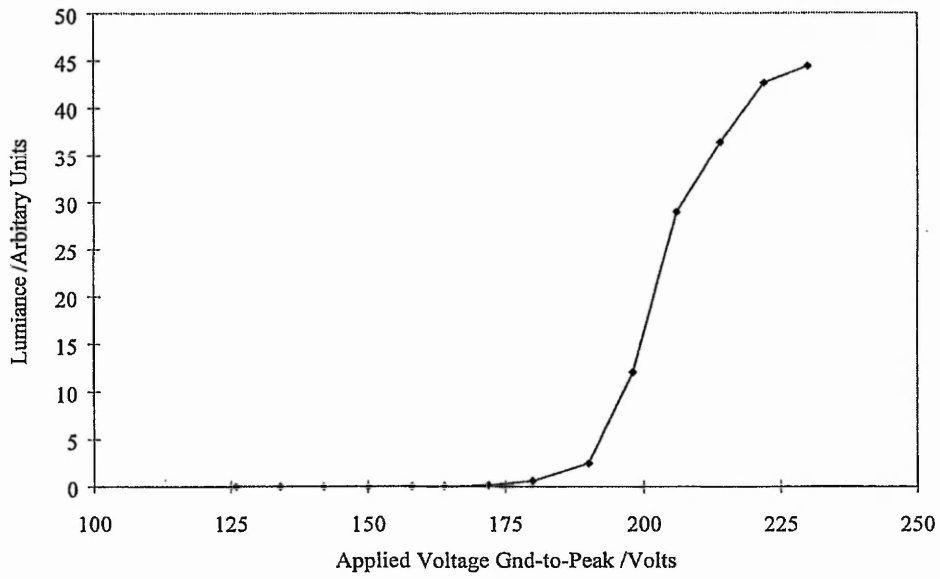
Figure 4.19 A Typical L-V response from a fully fabricated display device on wafer NTU383.
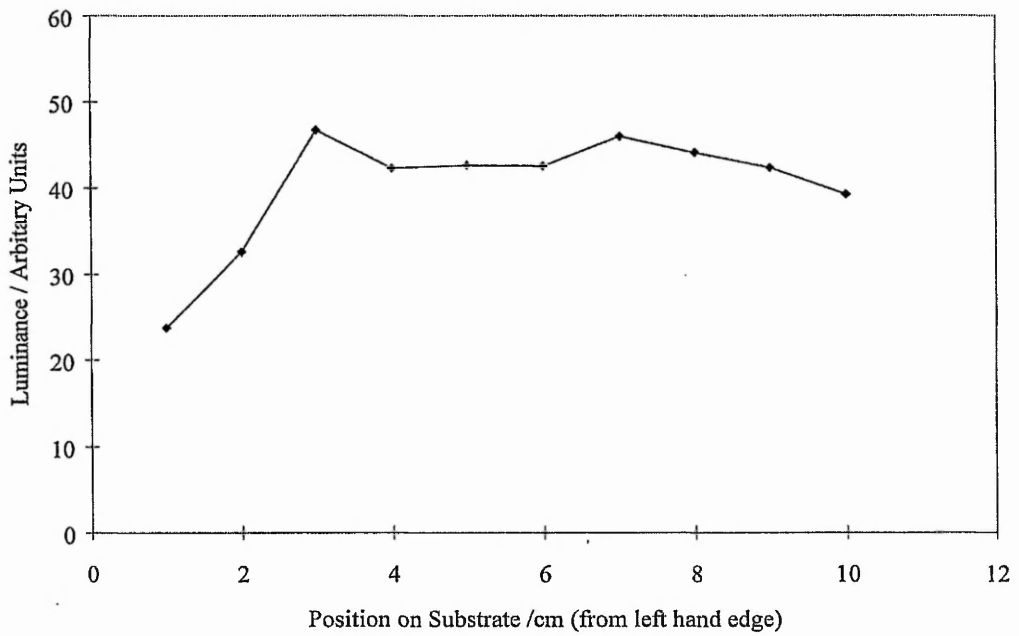
Figure 4.20 Uniformity of luminance at Vth + 30V across the 4" Substrate of wafer NTU383.
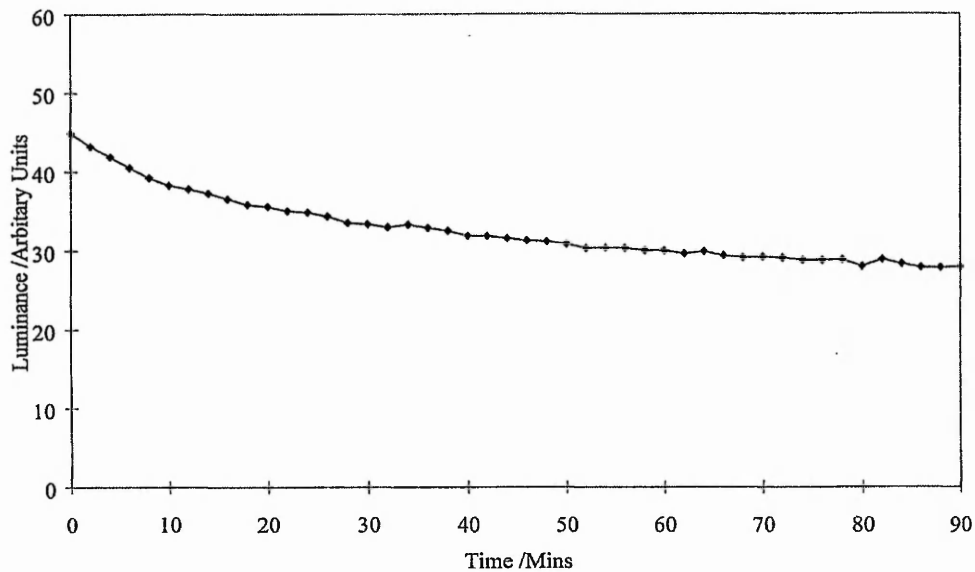
Figure 4.21 Initial decay in luminance with time for a LETFEL device on wafer NTU383.

4.8 Conclusions

The results detailed in section 4.6 are very satisfactory. They prove that the utilisation of the final fabrication route produces devices which are stable, uniform across the substrate, exhibit high luminance and satisfactory ageing characteristics. Since the determination of the final fabrication route approximately 20 substrates have been fabricated to produce high luminance displays.

It can be concluded that the full deposition and fabrication route to produce high luminance LETFEL displays has been optimised. The final fabrication route allows the further investigation into the optimisation of the aperture shape to continue. The problems associated with the use of ion milling have been identified and overcome.

Specifically, the initial miss-alignment problems have been overcome by utilising a new source of micro-mirrors. The metalisation of the device has now been optimised to utilise standard ASIC procedures, namely a tri-layer first metalisation level. Final devices have been characterised to show the success of the route including test ion milling.

4.9 References

1   D. Sands; *Ph.D. Thesis*, University of Bradford, (1987).

2   C. B. Thomas, R. Stevens, W. M. Cranton, I. P. McClean, M. R. Craven and A. H. Abdullah, *Society for Information Display Digest*, 1995 p887.

3   C. King, *Society for Information Display Digest,* 1994 p69.

4   D. R. Lide, *Handbook of Chemistry and Physics*, (CRC Press, Boston) 1992.

5   K. Sreenivas and A Mansingh, *Applications of Surface Science,* 22/23 (1985) p670.

6   Private Communication R.Stevens.

7   W. M. Cranton PhD. Thesis University of Bradford (1995).

8   C. B. Thomas, I. P. McClean, R. Stevens and W. M. Cranton, *IEE Electronics Letters*, 30 (16) 1994 p350.

9   M. R. Craven, *Investigation into the performance of wet etched Thin Film Electroluminescent Deivecs (TFEL's),* Final Year Project, University of Bradford 1994

10   R. Stevens, I. P. McClean and M. R. Craven, *IEEE Transactions of Semiconductor Manufacturing*, 9 (2), 1996 p241.

11   S. Otero Barros PhD. Thesis The Nottingham Trent University (2000)

12   R. Stevens PhD. Thesis University of Bradford (1994)

13   W. M. Cranton, C. B. Thomas, R. Stevens, M. R. Craven, S. O. Barros, E. Mastio and P. S. Theng, *Proceedings Electronic Information Displays Conference,* 1997

14   R. Stevens, C. B. Thomas and W. M. Cranton, *IEEE Electron Device Letters*, 15 (3) 1994 p97.

15   J. L. Vossen and W. Kern; (1978) *Thin Film Processes* (London: Academic Press)

16   Private Communication Andy Stevens Pilkington Optronics.

17   Private Communication. D. White Qudos Ltd.

Chapter 5 Conclusions and Further Work

5.1 Introduction

In order to achieve the aim of improving the performance of LETFEL devices, there were four major objectives behind the programme of research for this thesis, namely: -

1) Investigation into the use of a higher dielectric constant material as a replacement for the Y_2O_3 insulator thin films in the LETFEL device structure.

2) Deposition and characterisation of test LETFEL devices utilising the new insulator material characterised in 1 above to examine potential improvements due to enhanced waveguiding.

3) Development of a first order geometric model based on the step index planar dielectric waveguide structure.

4) Optimisation of the LETFEL device fabrication route to allow the shaping of the emitting aperture by the ion milling technique.

Each of these four objectives have been successfully investigated and the final conclusions from each investigation are summarised below.

5.2 Dielectric Characterisation

One of the major aims of this research was to identify, deposit and characterise a dielectric material to be used as the insulator in the LETFEL device to replace the Y_2O_3 thin films. The use of Y_2O_3 thin films is limiting due to a relatively low dielectric constant and the absence of a reactive ion etch recipe. Following a review of available dielectric materials, $BaTiO_3$ was identified as a material that had the potential for use. The literature study showed that $BaTiO_3$ thin films deposited under certain conditions could exhibit the required characteristics for use as the insulator in the LETFEL device structure, this also showed that improvements in the devices would be expected relative to the use of Y_2O_3 thin films. These characteristics include a dielectric constant, $\varepsilon_r > 16$, a refractive index, $n < 2.35$, a breakdown strength of at least 3 $MVcm^{-2}$ yielding a figure of merit (the charge storage capacity (C.S.C.)) of at least 3 μCcm^{-1}. A full investigation has been performed to determine the optimum conditions for the deposition of $BaTiO_3$ thin films by RF magnetron sputtering. The justification being to determine the optimum deposition conditions with respect to the characteristics of the thin films required for the LETFEL device.

The investigation into the $BaTiO_3$ thin films took the form of an extensive study into the effect of the deposition and post deposition annealing conditions on the aforementioned characteristics of the resultant thin films. The variation of the concentration of O_2 in the Ar sputter atmosphere, the pressure during deposition, the applied RF power density to the target and the range of post deposition

annealing temperatures from 400 to 800 °C have all been investigated to produce the optimum thin films. The optimum deposition and post deposition annealing conditions are summarised in table 5.1. These conditions yield films with the characteristics summarised in table 5.2, showing that BaTiO$_3$ thin films are suitable for use as thin film insulators in the LETFEL device structure.

Material	Ts - Substrate Temp °C	Power Density W cm^{-2}	Sputter Pressure mT	% Oxygen in Argon	Ta - Annealing Temp °C
BaTiO$_3$	200	2.62	7	30	700

Table 5.1 Summary of the optimum RF magnetron sputter deposition and annealing conditions for BaTiO$_3$ thin films.

Material	Dielectric Constant ε_r	Refractive Index n	Breakdown Field $E_{b/d}$ MV/cm	Charge Storage Capacity C.S.C. UC/cm
BaTiO$_3$	26	2.1	2.5	5.5

Table 5.2 Summary of BaTiO$_3$ thin film characteristics deposited and annealed utilising the optimum conditions given in table 5.1.

5.3 Simple Test LETFEL Devices

Simple test devices, of the structure in figure 5.1, including $BaTiO_3$ thin film insulators have been fabricated utilising the optimum deposition and post deposition annealing conditions detailed in table 5.1.
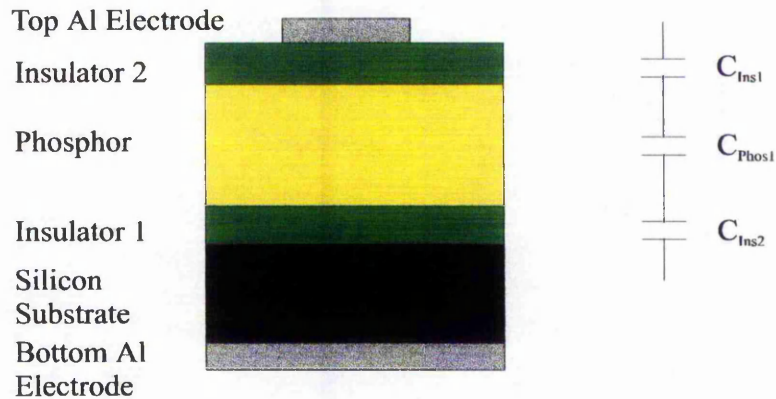
Figure 5.1 Basic LETFEL test device structure with its equivalent circuit. (This equivalent circuit is only valid for an applied voltage less than the threshold voltage of the device).

The investigation, for simplicity, was divided into two sections. The first stage was to determine the optimum structure with regards to both the exhibited luminance and the reliability. Four different device structures detailed in table 5.3 were fabricated.

Substrate Number	Insulator 1		Insulator 2		Reasoning
	Material	Thickness /nm	Material	Thickness /nm	
124	Y_2O_3	300	Y_2O_3	300	Control
120	$BaTiO_3$	300	Y_2O_3	300	$BaTiO_3$ Bottom
126	Y_2O_3	300	$BaTiO_3$	300	$BaTiO_3$ Top
125	$BaTiO_3$	300	$BaTiO_3$	300	$BaTiO_3$ Both

Table 5.3 Structural details of four initial device structures fabricated. Showing the variation of insulator material and position.

It was found that the optimum device structure was that of $Si/BaTiO_3/ZnS:Mn/Y_2O_3/Al$. This structure yielded devices with the highest ever reported luminance for a LETFEL device. Indeed, with a measured luminance of in excess of 270,000 fL (driven with a 250 V ground to peak 5 KHz sine wave), this is, to the author's knowledge, the highest reported luminance for any thin film AC TFEL device. The other two $BaTiO_3$ based structures, numbers 125 and 126, delaminated if exposed to air for over 2 hours, and thus were unsuitable for further investigation. The delamination can be attributed to one of two factors. The first factor being due to absorption of water from the atmosphere which has been reported as a disadvantage of $BaTiO_3$ elsewhere [1]. The second factor could be due to residual stress in the films. In devices 125 and 126 the top $BaTiO_3$ insulator film is exposed to the atmosphere whereas the successful device, 120, the $BaTiO_3$ insulator is sealed against the atmosphere by the phosphor and Y_2O_3 top insulator films. This gives a degree of support to the theory that the delamination is due to the absorption of water from the atmosphere rather than due to any residual stress in the films.

The second stage of this investigation was to vary the thickness of the $BaTiO_3$ insulator layer. The aim for this stage was to investigate any relationship between the cladding thickness and the measured luminance and/or the measured attenuation coefficient of the device structure. The increase in cladding thickness from the standard 300 nm was possible due to the increase in dielectric constant of

BaTiO$_3$ (ε_r = 26) over Y$_2$O$_3$ (ε_r = 16) without any increase in drive voltage. Figure 5.2 shows both the increase in measured luminance and the decrease in measured attenuation coefficient with an increase in cladding thickness. Here a novel method for the measurement of the attenuation coefficient was utilised. This method is based on the phenomena that the light emitted from the edge of a LETFEL device can be observed to decrease away from the emitting edge. In summary a CCD image of the device is captured. A software package is then used to measure the intensity of the luminance at set points away from the emitting edge. The intensity away from the emitting edge decreases exponentially. Utilising a curvefitting routine and equation 5.1, a value for the attenuation coefficient of each device was determined. For evaluation of this alternative method, rigorous checks were made against the more traditional increase in device length method of attenuation coefficient measurement technique. The results from both methods were shown to be within 5 % of each other for the same device structure (full details are given in section 3.5.2).
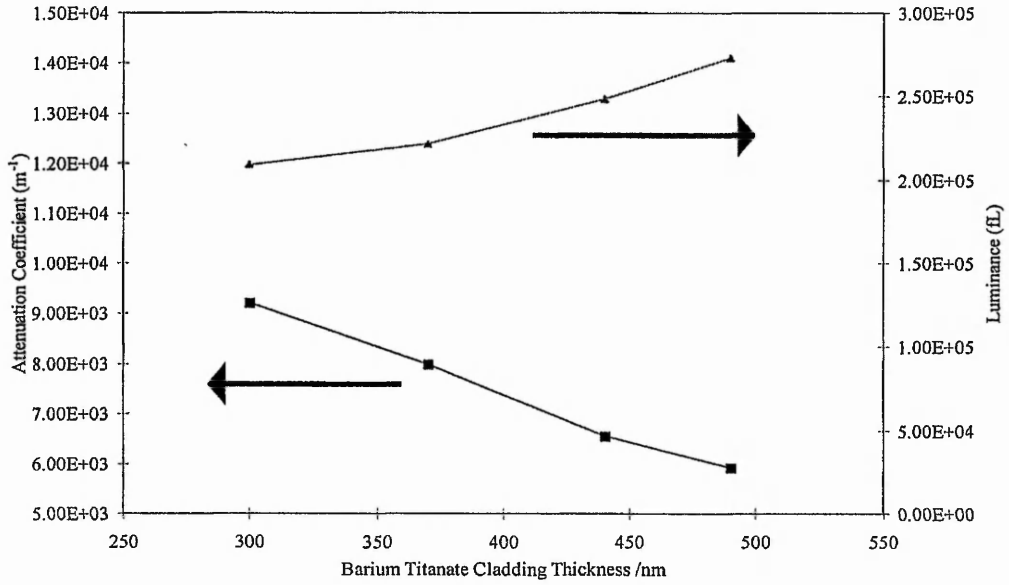
Figure 5.2 Increase in measured luminance and decrease in measured attenuation coefficient with an increase in BaTiO$_3$ cladding thickness (driven by a 5 KHz sine wave at V = Vth + 50 V). The device structure was BaTiO$_3$ (x nm)/ZnS:Mn (800 nm)/Y$_2$O$_3$(300 nm)

$$L = L_0 exp^{-\alpha x} \qquad \text{Eq. 5.1}$$

As expected, when the attenuation coefficient of the device decreases the observed luminance increases. Theoretically, the luminance should increase linearly with an increase in device length as more phosphor material (emitting centres) is contributing to the emission. In practice however there is a limit to this length due to the attenuation of the device. Hence, an "attenuation length" may be defined as the distance required for the luminance to drop to 10% of it's initial value. Therefore, the decrease in measured attenuation coefficient facilitates more effective emitting volume of phosphor material to contribute to the observed luminance. Typically, the attenuation length of a device is limited to the region of 166 to 200 μm [2]. Here, it has been shown that by utilising a BaTiO$_3$ insulator the

attenuation length of the device is increased to 390 μm. This yields an attenuation length improvement factor of 2.34. The increase in attenuation length for LETFEL devices is particularly important in the application of electrophotographic printing. For this application there is no effective limit to the length of the device contributing to the emission. However, in the case of a helmet mounted display the length of active material may be restricted by the device geometry, but an increase in attenuation length will lead to a decrease in losses in the device structure. Therefore the luminance observed from the same geometry device would be expected to be greater for the BaTiO$_3$ based device over the Y$_2$O$_3$ based device. Thus successful devices utilising BaTiO$_3$ thin film insulators have been fabricated, recording the highest reported value of luminance for any TFEL device.

5.4 First Order Geometric Model

Presented in chapter 3 is a first order geometric model for the LETFEL device structure. The model has been developed from the principles of the step index planar dielectric waveguide. However, due to the physical nature of the device structure, i.e. where the cladding thickness of the device at typically 300 nm is less than the wavelength of the emitted light, 585 nm for ZnS:Mn, energy may be lost due to evanescent outcoupling from the structure. An estimate of the effect of such an evanescent loss has consequently been investigated via consideration of the first order geometric model. Since energy loss is predicted to occur with a cladding thickness of less than at least 600 nm, it follows that by increasing the

cladding thickness, the confinement of light and hence lateral emission should be improved. In comparison to an optical fibre for example the cladding thickness is typically at least twice the wavelength of the transmitted light for maximum confinement. The increase in light confinement in a LETFEL device with an increase in cladding thickness has, for the first time, been shown to be true. This leads to the conclusion that the LETFEL device structure behaves similarly to that of a planar dielectric waveguide. Figure 5.2 shows the increase in measured luminance and the decrease in attenuation coefficient obtained as the thickness of the cladding material is increased. Further to this figure 5.3 shows the relationship between the decrease in the light theoretically lost due to evanescent outcoupling and the decrease in attenuation coefficient. These are shown to follow the same trend and hence give further evidence that the LETFEL device structure is in fact behaving as a lossy planar dielectric waveguide.
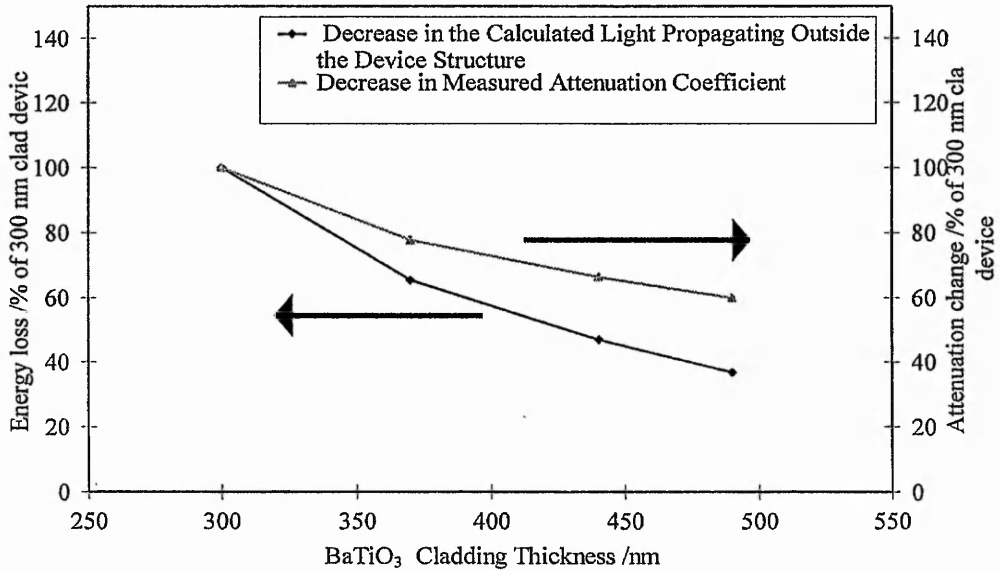
Figure 5.3 Relative change in characteristics with an increase in cladding thickness. All calculated with respect to the 300 nm clad device

In order to test the application of this performance improvement to miniature displays, a series of devices utilising the optimum device structure, i.e. $BaTiO_3(490$ nm$)/ZnS:Mn(800$ nm$)/Y_2O_3(300$ nm$)$ were deposited on micro-mirror substrates. Unfortunately all of the devices suffered from delamination after two to three hours out of vacuum storage. The problem could be due to lack of adhesion of $BaTiO_3$ to SiO_2 or in fact residual stress in the $BaTiO_3$ thin films when deposited on micro-mirrors. Previous experience with Y_2O_3 based devices on micro-mirrors has led to the introduction of a pre-deposition bake of the substrate. The premise being to drive out any moisture from the micro-mirror structures. This method was also used for the $BaTiO_3$ based devices, but with no success. For $BaTiO_3$ devices to be successful, the delamination problem has to be overcome. Firstly, an investigation into the use of a thin buffer layer of another

material to coat the micro-mirrors prior to BaTiO$_3$ deposition should be investigated. If adhesion is the problem this may be solved by the pre-sputtering of the substrate before the deposition of the BaTiO$_3$ insulator. This would roughen the SiO$_2$ surface and may help adhesion. However, the roughening of the mirror surface may also reduce the reflectivity of the mirror.

With regards to residual stress the best way to relieve this would be to deposit the device onto plain Si and then etch the aperture and finally deposit the micro-mirror into the aperture. This theory is discussed further in section 5.7.2. The final solution to this problem could be in fact to take a step back and look into an alternative high dielectric constant insulator material (see section 5.7.1). Now that it has been conclusively shown that increasing the cladding thickness leads to an increase in observed luminance there is sufficient evidence to continue the search into more high dielectric constant insulator materials. The choice of insulator material is discussed in more detail in section 5.7.1.

5.5 Fabrication Route

The fabrication route determined by R. Stevens during 1994 involved the fabrication of the micro-mirrors by AMPi, Taiwan. The substrates were then shipped to NTU for the deposition of the EL layers and then to Qudos Ltd., Oxford for the final metalisation and passivation stages. This fabrication route did in fact produce LETFEL devices exhibiting satisfactory characteristics. The limits on this fabrication route did not allow the shaping of the aperture by ion milling, which is the subject of a parallel investigation[3]. It was also desirable to find an

alternative source for the micro-mirrors due to delays in delivery. Therefore, there were two aims for the optimisation of the fabrication route. Firstly, an alternative source for the fabrication of micro-mirrors was required to allow the amount of shipping to be reduced. Secondly, the route had to be developed to allow ion milling to be utilised for the shaping of the aperture.

With the fabrication of the micro-mirrors taking place in Taiwan the delivery of finished substrates could be anything up to 3 months after placing an order. A secondary problem utilising this route included the use of a different contact mask aligner in Taiwan to the one at NTU. This led to miss-alignment across the substrate. Specifically, it was not possible to align more than 75% of the device structures on each substrate. The remaining devices showed miss-alignment of up to 3 μm. This of course reduces the final yield of the devices prior to any other fabrication. The problem is compounded at each lithographic stage. Also the risk of the substrates being held up or lost somewhere was very high. To solve this problem the fabrication of the micro-mirrors was switched to the National Micro-Electronics Research Centre (NMRC), Cork. This was beneficial due to the use of an identical mask aligner (A Cannon PLA 500 F), reducing miss-alignment to 1 μm (the tolerance of the aligner) and the reduction of the time lag between order and delivery to as little as 1 week.

The second stage, the inclusion of ion milling, was a larger problem to solve. The usual method to define regions in semiconductor processing is to use a photolithographic mask. In summary, a film of photoresist is deposited and patterned on the device substrate. During etching of the required materials the photoresist masks the areas where the materials are required. After etching the

photoresist is removed chemically or by RIE. This was used initially but during the ion milling process the photoresist polymerised. This made it impossible to remove after the etching process. Therefore a solution was devised utilising a sacrificial mask of SiO_2. However, the problem with this was that during the deposition of the SiO_2 by PECVD, spikes were formed in the Al electrode, as shown in figure 5.4.
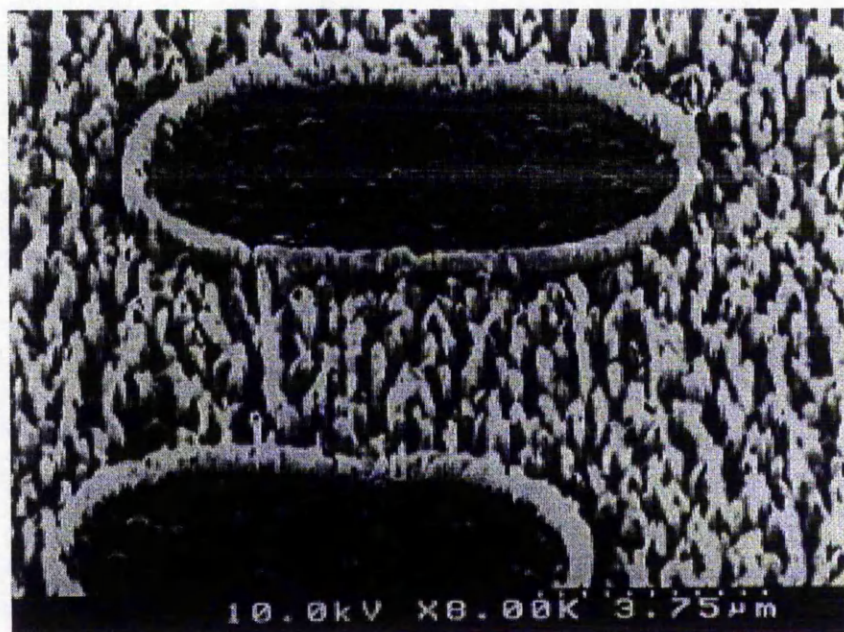
Figure 5.4 SEM of Al electrode with "spikes" protruding up from the surface.

The spikes in figure 5.4 could be pure aluminium or possibly aluminium oxide. If they are Al then they could be formed by the thermal expansion and reflowing of the Al into any pin holes or weak points in the SiO_2 during heating, SiO_2 is deposited at 300 °C. This reflow phenomenon has been previously utilised to form via holes during multi-layer ASIC production[4]. If the spikes are aluminium

oxide they could be formed by a chemical reaction between the aluminium and the oxygen from the nitrous oxide during the deposition of the sacrificial mask material. Aluminium has a high affinity towards oxygen, so the Al would readily react with any oxygen in the atmosphere, especially at a raised temperature, to form Al_2O_3.

The devices fabricated with the spikes exhibited failure at a low drive voltage, around 270 V peak-to-peak, and furthermore no wire bonding was possible to the bond pads. It was assumed that if the spikes came up from the electrode they could also penetrate into the Y_2O_3 insulator. This would cause the device to fail at a low voltage. The lack of bonding was due to either an increase in surface roughness or the inability to bond to Al_2O_3. Therefore a switch to a three layer first level metalisation was made. The Al electrode was sandwiched between two thin films of Ti/W. The Ti/W provided a physical barrier to inhibit either any reaction between the Al and the nitrous oxide, or any unwanted reflowing. The three layer metalisation and the use of an SiO_2 sacrificial mask are both standard processes in ASIC production[5]. To date at least 20 substrates have followed this revised fabrication process, resulting in a series of devices exhibiting high luminance stable characteristics.

5.6 Summary of Conclusions

In summary, various conclusions can be drawn from the work presented here. $BaTiO_3$ thin film insulators are currently not suitable for use in the LETFEL device. This is due to the problem of delamination. However, the principle for

the use of a high dielectric constant material has been proved. It has also been shown for the first time that the LETFEL device does behave in a similar way to the model developed from that of a step index planar dielectric waveguide. It has been shown that in the simple device format an improvement in performance is obtained when utilising a thicker insulator film. An improved fabrication route utilising Y_2O_3 insulators has been developed which can be easily updated to include any of the solutions detailed in the further work section. However, ion milling of the device aperture can not be regarded as an ideal solution for the shaping of the aperture. This method increases the number of fabrication stages and hence lengthens the fabrication time. Solutions to this problem are also proposed in the following further work section.

5.7 Further Work

5.7.1 Dielectric Materials

From this work it has been shown that a replacement dielectric for Y_2O_3 is still required. It has been shown here that an increase in cladding thickness leads to an increase in measured luminance. In comparison to a fibre optic cable the ideal thickness of the cladding should be at least two or three times greater than the wavelength of the emitted light. Therefore until a suitable material, with a suitable dielectric constant, has been characterised to give an insulator film

thickness greater than 1 μm, further research will be necessary. Unfortunately, the devices utilising $BaTiO_3$ insulators and micro-mirrors failed during the fabrication process due to delamination. Therefore, to enable the use of either thicker insulators or in fact to lower the operating voltage of the devices more studies need to be undertaken into some of the dielectric materials. Referring back to the initial literature study in section 1.6.2, an investigation into some more of the materials listed should be carried out. To ease this investigation it is now possible to obtain samples of some of the films commercially. For example SiO_2, Si_3N_4 and SiO_xN_y are available from Qudos Technology Ltd, Oxford and PZT (Lead Zirconate Titanate) is available from Cranfield University to mention just a few alternative materials.

A second alternative would be to investigate the use of a stacked insulator film for TFEL devices. Such a structure is shown in figure 5.5. The use of multiple layers has been shown to yield bright and stable devices [6]. The premise behind the reported research was to simply try to reduce the switching voltage, i.e. increase the sharpness of the L-V response, by using a multi-layer series of insulators of high and low resistivity materials in the device structure [6]. SiO_2 was used as both the high and low resistivity material. The difference in resistivity was obtained by the deposition of SiO_2 using different methods. Specifically, e-beam deposited SiO_2 has a low resistivity ($\sim 10^9$ ohm cm) and RF sputtered SiO_2 has a high resistivity ($\sim 10^{13}$ ohm cm). Table 5.4 details the characteristics of these films. Both devices were driven by a 1 KHz sine wave at 200 volts ground to peak. The

multi-layer device showed a sharper L-V response with approximately 10% improvement in maximum luminance.

Top Electrode
Top Insulator (High Resistivity)
Top Insulator (Low Resistivity)

Phosphor

Bottom Insulator (Low Resistivity)
Bottom Insulator (High Resistivity)
Transparent Electrode

Transparent Substrate

Surface
Emission
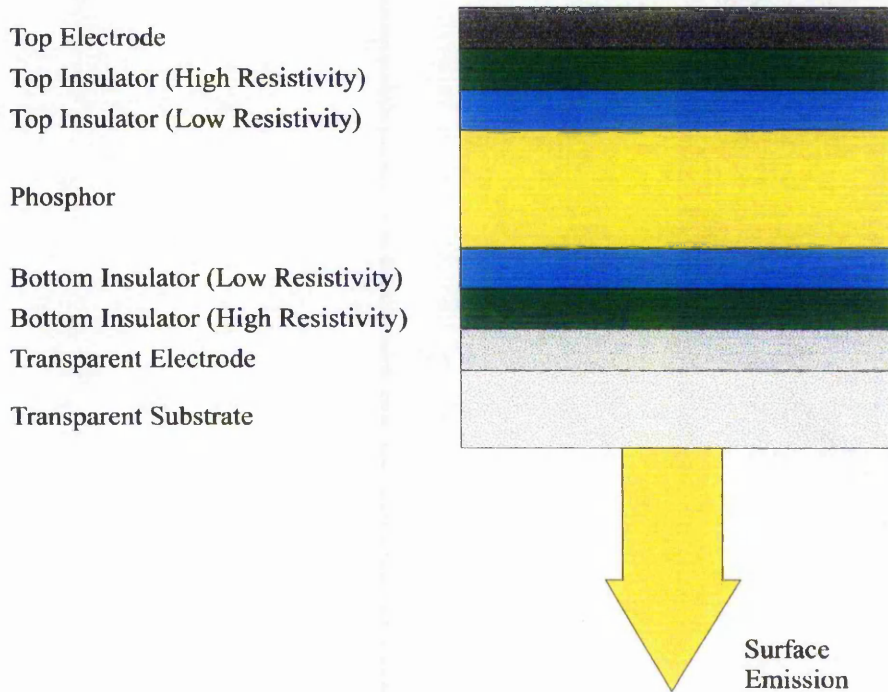
Figure 5.5 Stacked insulator TFEL device structure

Material	Resistivity ohm cm	Dielectric Constant	Deposition Method	Reference
SiO$_2$	10^9	5 to 10	E – Beam Evaporation	6
SiO$_2$	10^{13}	3 to 4	RF Sputtering	6

Table 5.4 Characteristics of high and low resistivity SiO$_2$ thin films

If SiO$_2$ was utilised it would have one benefit over the Y$_2$O$_3$ thin films currently employed as the insulator, that is there is a known reactive ion etch process, a mixture of CHF$_3$ and C$_2$F$_6$. This would make the ion milling of the aperture region obsolete. This would benefit the overall fabrication route, as the process time would be greatly reduced, as the requirement for a sacrificial mask would no

longer be there. If the search for a new dielectric material is pursued then the requirement for a reactive ion etch method must be considered.

5.7.2 Fabrication Route

The fabrication route detailed in chapter 4 has successfully streamlined the process to fabricate a LETFEL device. This route has also been demonstrated to be successful for the fabrication of test fixed legend displays, as shown in figures 5.7 and 5.8.
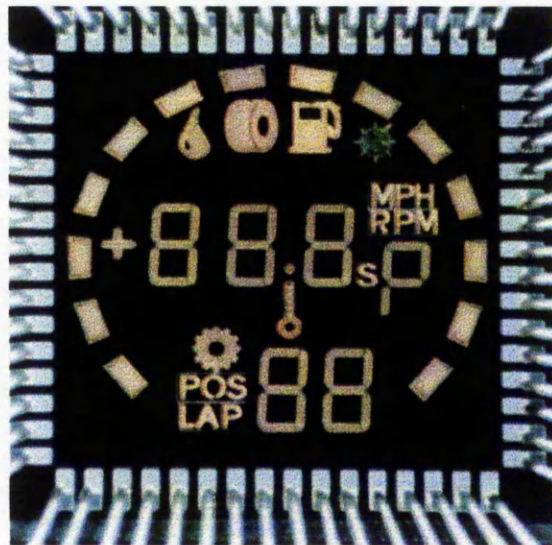
Figure 5.7 A fixed legend LETFEL display.
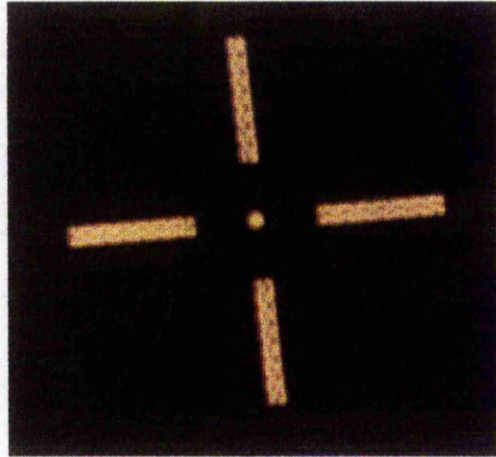
Figure 5.8 Segment of a fixed legend display. Each line of the cross is 34 microns wide.

Recently an attempt has been made to fabricate high resolution VGA type displays. As expected with the fabrication of a new device, problems have been encountered. The initial problem was the quality of micro-mirrors supplied from NMRC, Cork. The previous process configuration was designed for fixed legend displays, that is devices with a low density of micro-mirrors. The same process, calibrated for the low density of micro-mirrors, was used to define the high density micro-mirrors. On inspection of these mirrors it was seen that the definition had been lost. At the same time it was discovered that the tolerance of the contact mask aligner utilised in the fabrication route was too large for these displays. This two-fold problem is currently being investigated. The photolithographic alignment has been switched to a GCA stepper aligner and the process of the fabrication of the micro-mirrors is now contracted to Qudos Ltd, Oxford. Current outstanding problems include a degree of miss-alignment caused by blurring of the alignment key of up to 2 μm. The alignment key is a 1.6 μm cross. Due to the polycrystalline nature of the Y_2O_3 insulator over the alignment

key scattering of the incident light from the camera on the stepper is produced. This decreases the tolerance of the alignment process. This problem can only be solved by removing all of the material on the alignment key during the processing. As discussed in chapter 4 the reduction of the number of photolithographic masking and alignment processes is desirable. This is due to a reduction in the chance of misalignment and of course processing time. One method to reduce the processing steps is to utilise RIE for the shaping of the aperture region of the device as opposed to utilising the ion milling technique. RIE is only possible with the correct choice of insulator material.
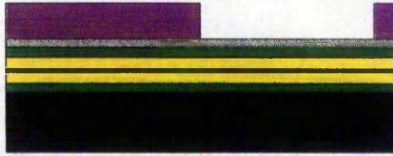
5.7.3 Device Structure

Improvements to the device structure have been discussed above, these include the choice of insulator material to enable RIE to be utilised as opposed to ion milling for the shaping of the aperture region. Recent results from the ion milling investigation have revealed that the further the device aperture is etched, the observed luminance is increased and also an increase in reliability has been observed[7]. One thought behind the increase in reliability is that the removal of the material reduces the stress in the thin film structure. The material removal also reduces the area of high field regions, i.e. over the micro-mirrors.

As discussed in section 5.4 delamination has been experienced when $BaTiO_3$ is utilised as the insulator in micro-mirror devices. This could be due to residual stress in the films. Equivalent devices deposited on Si substrates with no micro-mirrors do not suffer from this problem. Optical micrographs of the current Y_2O_3

insulator have shown microscopic cracking. This all tends to indicate that the thin films are stressed when deposited on micro-mirrors. A novel solution to this would be to deposit the EL structure on Si substrates with no micro-mirrors, etch the aperture and then add the micro-mirrors, see figure 5.9. This would open up the opportunity to try different methods of micro mirror fabrication.

A recent development in the field of micro engineering has been the fabrication of micro-lenses which may be suitable to replace the micro-mirrors. The process of fabrication is a simple coat and lithographic process. The final structures could even be coated with a highly reflective material, chrome or nickel for example. The effect of these may increase the luminance to a greater value than utilising the current micro mirrors. If micro-mirrors are to be used in their current format an investigation into the effect of both the density of micro-mirrors and the resultant wall angles is required. This investigation has never been completed and utilising the GCA stepper a variation in these parameters can be fabricated on the same substrate, this giving an easy and direct comparison.

Process Number	Process Name / Location	Process Aim	Aperture Configuration
1	Plain Si substrate (NTU)	N -Type 2 - 6 Ohm/cm 100 ± 0.5 mm Diameter 525 ± 50 μm Thick	
2	LETFEL material deposition (NTU)	Deposition of 5 layers of insulator and phosphor thin films and post deposition annealing	
3	Metalisation (Qudos)	Deposition of Aluminium	
4	Electrode and aperture definition (Qudos)	Photolithography mask to define the electrode and hence the aperture shape and size	
5	Electrode and aperture etch (Qudos)	RIE of Electrode , Aperture and removal of photoresist	
6	Deposition of micro - mirrors	Deposition and shaping of micro-lens material for use as micro-mirrors	
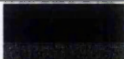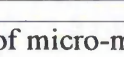
Silicon SiO$_2$ Insulator ZnS:Mn Phosphor		Aluminium Micro - Lens Material Photoresist	

Figure 5.9 Proposed alternative process route for the fabrication of micro-mirrors.

5.7.4 Process Control

The overall aim of the displays research group at NTU is to investigate the underlying mechanisms of TFEL devices in order to promote improvements, and ultimately to produce bright and reliable prototype HMD's and LETFEL devices. The goal is to produce a commercial device in collaboration with Qudos Technology Ltd. For this to happen a series of controls and quality analysis needs to be implemented, as would be included in a commercial production process. These controls should include regular characterisation of the thin films used. In the case of the insulator and phosphor films, the quality control characterisations must include the dielectric constant, the breakdown field strength, the refractive index, an optical study to determine the defect density and photoluminescent characterisation of the device prior to the metalisation. For final evaluation of a substrate, a process control monitor, or PCM, must be included in each new mask set. The PCM would consist of a set of devices to enable characterisation of the devices at different stages of the processing. For example, a set of critical dimension devices, CD's, to monitor any over-etching, a device to measure the luminance at various stages to evaluate each substrate and a meander to measure the resistivity of the structure. This would enable direct comparison between substrates both during and after the fabrication route.

5.8 Final Conclusions

The identification of an alternative dielectric material for use as an insulator in the simple form of LETFEL device has been successfully completed. This has led to the development of a model based on the step index planar waveguide structure to explain the fundamental optical operation of the device. For the first time a relationship between the LETFEL device and the first order waveguide has been determined. A new streamlined fabrication route has been characterised to allow the ion milling of the device aperture. A series of problems have been defined with proposed solutions to allow the fabrication of prototype devices. When these solutions have been fully characterised a full set of design and processing conditions will be known for the successful deposition and fabrication of AC TFEL devices. This will lead to the production of initial prototype devices and then the move to production can be initiated.

5.9 References

1   B. Chornik, V. A. Fuenzalida, C. R. Grahmann and R. Labbe; *Vacuum,* 48 (2) (1997) p161-164.

2   R. Stevens PhD. Thesis University of Bradford (1994)

3   S. Otero Barros PhD. Thesis The Nottingham Trent University (2000)

4   Private Communication Andy Stevens Pilkington Optronics.

5   Private Communication David White, Qudos Technology.

6   Y. Sekido, M. Koizumi, J. Mita, T. Hayashi, M. Kazama and K. Nihei; *Digest of the SID,* 1986 p171-174.

7   S. Otero Barros PhD. Thesis The Nottingham Trent University (2000)

APPENDIX 1

Full Deposition Record For Wafers Deposited and Fabricated by the Author At NTU

Wafer Number	System	Structure	Use	Comments
001	1	YO	First Growth	Test Deposition
002	1	ZnS:Mn	First Growth	Test Deposition
003	1	ZnS:Mn	First Growth	Test Deposition
004	1	ZnS:Mn	First Growth	Test Deposition
005	2	$BaTiO_3$	First Growth	Test Deposition
006	1	Y/Z/Y	PL Test Growth	Test Deposition
007	2	$BaTiO_3$	Characterisation	2 mT Ar
008	1	Y/Z	PL Testing	HETFEL Base Layer
009	2	$BaTiO_3$	Characterisation	4 mT Ar
010	2	$BaTiO_3$	Characterisation	4 mT Ar
011	1/2	Y/Z/Y/Al	ACEL Device	HETFEL Base Layer
012	2	$BaTiO_3$	Characterisation	4 mT Ar
013	2	$BaTiO_3$	Characterisation	4 mT Ar with TORSEAL for uniformity
014	2	$BaTiO_3$	Characterisation	4 mT Ar Distance/uniformity
015	2	$BaTiO_3$	Characterisation	4 mT Ar uniformity
016	2	$BaTiO_3$	Characterisation	10 mT Ar Ceramics/uniformity
017	2	$BaTiO_3$	Characterisation	15 mT Ar
018	2	$BaTiO_3$	Characterisation	15 mT Ar Heating/Grow/Heating
019	2	Al:Si	First Growth	100 W
020	2	Al:Si	Characterisation	200 W
021	2	Al:Si	Characterisation	100 W Thickness
022	2	Al:Si	Characterisation	
023	1/2	Y/Z/Y/Al	ACEL Test Device	HETFEL Base Layer
024	2	Al:Si	Characterisation	Milky
025	2	Al:Si	Characterisation	Baked Chamber not milky
026	2	Al:Si	Characterisation	
027	2	Al:Si	Characterisation	
028	2	Al:Si	Characterisation	
029	2	Al:Si	Characterisation	
030	2	$BaTiO_3$	First Growth after Al Deposition	
031	2	Al:Si	Characterisation	

032	2	B/AL	Characterisation	Sputtered Al for Capacitors
033	2	$BaTiO_3$	Characterisation	Ar/O_2 90/10
034	2	$BaTiO_3$	Characterisation	Ar/O_2 80/20
035	2	$BaTiO_3$	Characterisation	Ar/O_2 70/30
036	2	$BaTiO_3$	Characterisation	Ar/O_2 95/5
037	2	$BaTiO_3$	Characterisation	Ar/O_2 85/15
038	2	$BaTiO_3$	Characterisation	Ar/O_2 90/10
039	2	$BaTiO_3$	Characterisation	Ar/O_2 90/10
040	2	$BaTiO_3$	Characterisation	Ar/O_2 90/10
041	2	$BaTiO_3$	Characterisation	Ar/O_2 90/10
042	1	YO	Characterisation	HETFEL Base Layer
043	2	$BaTiO_3$	Characterisation	Ar/O_2 90/10
044	2	$BaTiO_3$	Characterisation	80 W
045	2	$BaTiO_3$	Characterisation	120 W
046	1	ZnS:Mn	Characterisation	Plain Si Anneal/crazing affects
047	2	$BaTiO_3$	Characterisation	400 anneal
048	1/2	Y/Z/Y/Z/Y /Al	ACEL Device	New Base Layer Set 3
049	2	$BaTiO_3$	Characterisation	500 anneal
050	2	$BaTiO_3$	Characterisation	600 anneal
051	2	$BaTiO_3$	Characterisation	700 anneal crazed
052	1/2	Y/Z/Y/Z/Y /Al	ACEL Test Device	Mirrors
053	2	$BaTiO_3$	Characterisation	700 anneal/crazing ok
054	1/2	Y/Z/Y/Z/Y /Al	ACEL Device	Phosphor PT 200
055	1/2	Y/Z/Y/Z/Y /Al	ACEL Device	PT 200 no crazing on mirrors
056	1/2	Y/Z/Y/Z/Y /Al	ACEL Device	PT 200 no crazing on mirrors
057	1	$BaTiO_3$	Characterisation	700 anneal for 5 hours
058	1/2	Y/Z/Y/Z/Y /Al`	ACEL Device	.43 phosphor on HETFEL
059	1/2	SiN/Al	First growth	
060	1/2	SiN/Al	Test SiN	
061	1	Y/Z/Y/Z/Y	ACEL Device	.43
062	1/2	SiN/Al	Characterisation	
063	1/2	Y/Z/Y/Z/Y /Al	ACEL Device	
064	1/2	Y/Z/Y/Z/Y /Al	ACEL Device	
065	1	ZnS:43	Laser Annealing thin film	For RAL
066	1	ZnS:43	RAL	Target sputtered through

067	1	ZnS:43	RAL	
068	1	Y/Z:43	RAL	
069	1/2	Y/Z/Y/Al	RAL	
070	2	Al:Si	Wentworth	To be etched for probe card
071	2	Al:Si	Wentworth	
072	1/2	Y/Z/Y/Z/Y /Al	ACEL device	
073	1	YO	RAL	
074	1	Y/Z:43	RAL	
075	1/2	Y/Al		
076	1/2	Y/Z/Y/Z/Y /Al	PBL	
077	1/2	Y/Z/Y/Z/Y /Al/SiN	PBL	
078	1/2	Y/Z/Y/Z/Y /Al/SiN	PBL	
079	1/2	Y/Z/Y/Z/Y /Al/SiN	PBL	
080	1/2	Y/Z/Y/Z/Y /Al	PBL	
081	1/2	Y/Z/Y/Z/Y /Al/SiN	PBL	
082	1/2	Y/Z/Y/Z/Y /Al/SiN	PBL	
083	2	$BaTiO_3$	Characterisation	First Hot Growth
084	2	$BaTiO_3$	Characterisation	200 dep
085	2	$BaTiO_3$	Characterisation	Ar/O_2 90/10 200 °C
086	2	$BaTiO_3$	Characterisation	Ar/O_2 80/20 200 °C
087	2	$BaTiO_3$	Characterisation	Ar/O_2 70/30 200 °C
088	2	$BaTiO_3$	Characterisation	Ar/O_2 95/5 200 °C
089	2	$BaTiO_3$	Characterisation	Ar/O_2 85/15 200 °C
090	2	$BaTiO_3$	Characterisation	Ar/O_2 60/40 200 °C
091	2	$BaTiO_3$	Characterisation	Ar/O_2 75/25 200 °C
092	2	$BaTiO_3$	Characterisation	Ar/O_2 70/30 3mT
093	2	$BaTiO_3$	Characterisation	3 mT
094	2	$BaTiO_3$	Characterisation	5 mT
095	2	$BaTiO_3$	Characterisation	10 mT
096	2	$BaTiO_3$	Characterisation	12 mT
097	2	$BaTiO_3$	Characterisation	12 mT
098	2	$BaTiO_3$	Characterisation	7 mT 400 anneal
099	2	$BaTiO_3$	Characterisation	500 anneal
100	2	$BaTiO_3$	Characterisation	600 anneal
101	2	$BaTiO_3$	Characterisation	700 anneal
102	2	$BaTiO_3$	Characterisation	800 anneal

103	1	YO	First Growth	
104	1	ZnS:43	First in Clean System	
105	1	Y/Z/Y	ACEL Device	
106	1/2	Y/Z/Y/Al/SiN	ACEL Device	
107	2	SiO	No Growth	
108	2	SiO	Characterisation	70/30 Ar/O
109	2	SiO	Characterisation	
110	2	Al/SiO	Characterisation	
111	1/2	Y/Al	Characterisation	
112	2/1	B/Z/Y	ACEL Device	800 anneal of bottom before EL deposition
113	1	Y/Z/Y/Z/Y	ACEL Device	
114	1	Y/Z		
115	2/1	B/Z/B	ACEL Device	800 anneal then 700 aftewr El dep Wafer Crazed
116	2/1	B/Z/Y	ACEL Device	800 then 500 total annealing
117	1/2	Y/Z/Y/Z/Y /Al/SiN	ACEL Device	Set 2 or 3 ?
118	1/2	Y/Z/B	ACEL Device	700 anneal total
119	2/1	B/Z/Y	ACEL Device	700 anneal of base layer only
120	2/1	B/Z/Y	ACEL Device	700 total anneal
121	2	Al/SiN	Characterisation	
122	1	Y/Z/Y	ACEL Device	700 anneal
123	2/1	B/Z/B	ACEL Device	Power lost in lab lost wafer
124	1	Y/Z/Y	ACEL Device	700 anneal
125	2/1	B/Z/B	ACEL Device	Crazed
126	1/2	Y/Z/B	ACEL Device	700 anneal
127	1/2	Y/Z/Y/Z/Y /Al/SiN	ACEL Device	Cork BL
128	2	SiO	Characterisation	
129	2	SiO	Characterisation	
130	1	Y/Z/Y/Z/Y	ACEL Device	Set 2 BL
131	2/1	B/Z/B	ACEL Device	Crazed
132	1/2	Y/Z/Y/Z/Y /Al/SiN	ACEL Device	Cork PBL
133	2/1	B/Z/Y/Z/Y	ACEL Device	
134	2	SiO	Characterisation	
135	1	ZnS:200	RAL	
136	1	ZnS:200	RAL	
137	1	ZnS:200	RAL	
138	1	ZnS:200	RAL	

139	1	ZnS:200	RAL	
140	1	ZnS:200	RAL	
141	1	Y/Z200/Y	RAL	
142	1/2	Y/Z.43/B	ACEL Device	4400 B
143	1/2	Y/Z.43/B	ACEL Device	Crazed
144	1/2	Y/Z.43/B	ACEL Device	3700 B
145	1/2	Y/Z.43/B	ACEL Device	3300 B
146	1/2	Y/Z/Y/Z/Y /Z/B	ACEL Device	Double Barrier Layer
147	1	YO	RAL	
148	1	ZnS:200	RAL	
149	1	YO	RAL	
150	1	ZnS:200	RAL	
151	1	ZnS:200	RAL	
152	1	YO	RAL	
153	1/2	Y/Z/B	ACEL Device	Thickness B Device
154	1/2	Y/Z/B	ACEL Device	Thickness B Device
155	1	Y/Z/Y	ACEL Device	
156	1/2	Y/Z/B	ACEL Device	Thickness B Device
157	2/1	B/Z/Y	ACEL Device	Mirrored B Device
158	2/1	B/Z/Y/Z/Y	ACEL Device	Target Through
159	2/1	B/Z/Y/Z/Y	ACEL Device	
160	1	Y/Z:200/Y	ACEL Device	RAL
161	1	Y/Z:200/Y	ACEL Device	
162	1	Y/Z:200	RAL	
163	1	Y/Z:200/Y	RAL	
164	1	Y/Z:200	RAL	
165	1	Y/Z/Y/Z/Y	Metaled mirrors	Met PBL
166	2/1	B/Z/Y	ACEL Device	
167	1	Y/Z/Y/Z/Y	Cork Set 3	
168	1	Y/Z/Y	Set 2	
169	1	Y/Z/Y/Z/Y	Cork Set 3	
170	2/1	B/Z/Y	Set 2	
171	1	Y/Z/Y/Z/Y	Cork PBL	
172	1	Y/Z/Y/Z/Y	Set 3	
173	1	Y/Z/Y/Z/Y	Set 2	
174	2/1	B/Z/Y/Z/Y	Set 2	
175	1	Y/Z/Y/Z/Y	Set 3	
176	1	Y/Z/Y/Z/Y	Set 3	
177	1	Y/Z/Y	Set 2	
178	1	Y/Z/Y	Set 2	
179	1	Y/Z:198		No P Deposition
180	1	Y/Z:199/Y		Commercial Phosphor

181	1	Z:199/Y	Cranfield	
182	1	Y/Z		Target Sputtered Through
183	1	Y/Z		
184	2/1	B/Z:198/Y		
185	1	ZnS:199		
186	1	Y/Z:198/Y		Commercial Phosphor
187	1	Y/Z:199/Y		Commercial Phosphor
188	1	Y/Z:199	RAL	
189	2/1	B/Z/Y		
190	1	Y/Z:200/Y		Commercial Phosphor - Crazed
191	2/1	B/Z/Y/Z/Y		
192	1	Y/Z:200/Y		Commercial Phosphor
193	1	Y/Z:116/Y		Commercial Phosphor - Crazed
194	1	Y/Z:116/Y		Commercial Phosphor - Crazed
195	1	Y/Z:116/Y		Commercial Phosphor
196	1	Y/Z:117/Y		Commercial Phosphor
197	1	YO		Target Arching - Scrapped
198	1	Y/Z:118/Y		Commercial Phosphor
199	2/1	B/Z:117/Y	ACEL Device	Test for B in pure Ar For Crazing
200	1	Y/Z:199	RAL	
201	1	ZnS:199	RAL	
202	1	Y/Z:199/Y		Plain Si For CCD Images
203	2	BaTiO3	RAL	500 in pure Ar
204	1	Y/Z/Y/Z/Y	PBL	POGS 4000 YO
205	1	Y/Z/Y/Z/Y	PBL	POGS 3500 YO
206	1	Y/Z/Y/Z/Y	Set 3	POGS 3500 YO
207	1	Y/Z/Y/Z/Y	Set 3	P171 3500 YO
208	evap	Al	Plain Si	Uniformity of evap Al 1500
209	1	Y/Z/Y	Set 2	P199 3000 YO
210	1	Y/Z/Y	Plain Si	P199 3000 YO
211	1	Z	Plain Si	P171
212	2	$BaTiO_3$	Plain Si	
213	1	Y/Z/Y + bl	Set 3	P172
214	1	Y/Z	Set 3	P 173 Phos Target Through
215	1	Y/Z	Set 3	P 174 Phos Target Through
216	1	Y/Z/Y	Set 2	P 200
217	1	Y/Z/Y	Set 2	P 118
218	1	Y/Z/Y	Plain Si	RAL SARA
219	1	Y/Z/Y	Plain Si	P 116 Cold ZnS:Mn dep
220	1	Y/Z/Y	Plain Si	P 116 Hot ZnS:Mn Dep
221	1	Y/Z/Y	Plain Si	CRAZED

222	1	Y/Z/Y	Plain Si	P 116 SARA
223	1	Y/Z/Y	Set 2	P 116 Test etching here
224	1	Y	Plain Si	RAL - SARA
225	1	Z	Plain Si	CRAZED
226	1	Y/Z/Y	Plain Si	ME
227	2	B	Plain Si	test dep
228	1	Z	Plain Si	No Anneal
229	1	Z	Plain Si	500 Anneal
230	1	Z	Plain Si	500 Anneal
231	1	Y/Z	Plain Si	No Anneal
232	1	Y/Z	Plain Si	Z burnt through
233	2/1	B/Z/B	Set 2	500 Anneal
234	1	Y/Z	Plain Si	500 Anneal
235	1	Y/Z/Y	Plain Si	500 Anneal
236	1	SiON/Z/Y	Plain Si	500 Anneal
237	1	SiN/Z/Y	Plain Si	500 Anneal
238	1	SiON/Z/Y	Plain Si	CRAZED
239	1	SiN/Z/Y	Plain Si	Very Thin Phosphor
240	1	Z	Plain Si	Target Burnt Through
241	1	Z	Plain Si	No Anneal
242	1	Z	Plain Si	500 Anneal
243	1	Y/Z	Plain Si	500 Anneal
244	1	Y/Z	Plain Si	No Anneal
245	1	Y/Z/Y	Plain Si	400 Anneal
246	1	Y/Z/Y	Set 3	400 Anneal
247	1	Y/Z/Y	Metallised Set 3	400 Anneal
248	1	SiON/Z/Y	Plain Si	500 Anneal
249	1	Y/Z/Y	Plain Si	Crazed
250	1	SiN/Z/Y	Plain Si	500 Anneal
251	1	Y/Z/Y	Plain Si	500 Anneal
252	2/1	B/Z/Y	Plain Si	500 Anneal
253	1	SiON/Z/Y	Plain Si	500 Anneal
254	1	PZT/Z/Y	Plain Si	500 Anneal
255	2/1	B/Z/Y	Plain Si	500 Anneal
256	1	PZT/Z/Y	Plain Si	500 Anneal
257	1	Z/Y	Plain Si	No Anneal
258	1	Y/Z/Y/Z/Y	PBL 1	500 Anneal
259	1	Y/Z	Plain Si	No Anneal
260	1	Y/Z/Y/Z/Y	PBL 1	700 Anneal
261	1	Y/Z/Y/Z/Y	PBL 1	700 Anneal
262	1	Y/Z/Y	Plain Si	1.2um Z 500 Anneal
263	1	Y	Plain Si	Y test wafer 500 Anneal
264	1	Z	Plain Si	PL test wafer P116 500 Anneal

265	1	Z	Plain Si	PL Test Wafer P171 500 Anneal
266	1	Y/Z	Set 2	Target burnt through
267	2	Y:Eu	Plain Si	25% test PL wafer
268	1	Z	Plain Si	PL Test Wafer P117 500 Anneal
269	Evap	Al	SiN	Capacitor test wafer
270	Evap	Al	SiON	Capacitor test wafer
271	Evap	Al	PZT	Capacitor test wafer
272	1	Y/Z/Y	Set 2	P117 test El wafer 500 Anneal
273	1	Y/Z/Y	Set 2	P116 Test EL wafer 500 Anneal
274	1	Y/Z	Set 2	Target through P171
275	1	Z	Plain Si	P117 PL test wafer 500 Anneal
276	1/2	Y/Y:Eu 35%	Plain Si	Y:Eu 35% test PL wafer
277	1	Z	Plain Si	500 Anneal test etch wafer
278	1	Z	Plain Si	500 Anneal test etch wafer
279	1	Z	Plain Si	500 Anneal test PL wafer P118
280	1	Z	Plain Si	500 Anneal test PL wafer P199
281	1	Z	Plain Si	500 Anneal PL test wafer P198
282	1	Y	Plain Si	500 Anneal test etch wafer
283	1	Y	Plain Si	500 Anneal test etch wafer
284	1	Y/Z/Y	Set 2	500 Anneal P198 test El wafer
285	1	Y/Z/Y	Set 2	500 Anneal P118 test EL wafer
286	2	BaTiO$_3$	Plain Si	Dropped
287	1	Y/Z/Y	Set 2	500 Anneal P199 test EL wafer
288	2/1/2	B/Z/B	Set 2	500 Anneal
289	2/1	B/Z/Y	Plain Si	500 Anneal
290	1	Z	Plain Si	500 Anneal PL test wafer P200
291	1	Z	Plain Si	500 Anneal PL test wafer POGS
292	1	Y/Z/Y	Set 2	500 Anneal EL test wafer P200
293	1	Y/Z/Y	Set 2	500 EL test wafer POGS

294	2/1	B/Z/Y	Plain Si	500 Anneal
295	1	Y/Z/Y	Set 2	500 Anneal EL test wafer P171
296	1	Y/Z/Y/Z/Y	Set 3	500 Anneal
297	2	BaTiO$_3$	P type	For Vili
298	1	Z	P Type	For Vili
299	1	Y/Z/Y/Z/Y	Set 3	600 Anneal
300	1	Y/Z/Y/Z/Y	Set 3	700 Anneal
301	1	Y/Z/Y/Z/	PBL 1	500 Anneal
302	1	Y/Z/Y/Z/Y	PBL 1	600 Anneal
303	1	Y/Z/Y/Z/Y	PBL 1	700 Anneal
304	1	Z	Plain Si	500 Anneal
305	1	Y	Plain Si	500 Anneal
306	1	Z	Plain Si	500 Anneal
307	2	Y:Eu	Plain Si	PL test wafer
308	1	Y	Plain Si	500 Anneal
309	2	Y:Eu	Plain Si	PL test wafer
310	2	Y:Eu	Plain Si	PL test wafer
311	2	Y:Eu	Plain Si	PL test wafer
312	2	BaTiO$_3$	Plain Si	
313	2	BaTiO$_3$	Plain Si	
314	1	Y	Plain Si	500 Anneal
315	1	Y/Z/Y	Plain Si	500 Anneal
316	1	Y/Z/Y	Plain Si	500 Anneal
317	1	Y/Z/Y	Plain Si	500 Anneal
318	1	Y/Z/Y	Plain Si	500 Anneal
319	1	Y/Z/Y	Plain Si	500 Anneal
320	1	Y/Z/Y	Plain Si	500 Anneal
321	1	Y/Z/Y	Plain Si	500 Anneal
322	1	Y/Z/Y	Plain Si	500 Anneal
323	1	Y/Z	Plain Si	No Anneal
324	1	Y/Z	Plain Si	No Anneal
325	1	Y/Z	Plain Si	No Anneal
326	1	Y	Plain Si	500 Anneal
327	1	Y/Z	Plain Si	No Anneal
328	1	Z	Plain Si	No Anneal
329	1	Z	Plain Si	500 Anneal
330	1	Z	Plain Si	500 Anneal
331	1	Z	Plain Si	No Anneal
332	1	Z	Plain Si	No Anneal
333	1	Z	Plain Si	No Anneal
334	1	Z(undoped)	Plain Si	No Anneal
335	1	Z(undoped)	Plain Si	No Anneal
336	1	Y	Plain Si	500 Anneal

337	1	Y	Plain Si	500 Anneal
338	1	Z	Plain Si	500 Anneal PL Test Wafer P116
339	1	Y/Z/Y	Set 2	500 Anneal EL test wafer P117
340	1	Y/Z/Y	Plain Si	500 Anneal
341	1	Y/Z/Y	Plain Si	500 Anneal
342	1	Y/Z/Y	Plain Si	500 Anneal
343	1	Y/Z/Y	Plain Si	500 Anneal
344	1	Y/Z/Y	Plain Si	500 Anneal
345	1	Y/Z/Y	Plain Si	500 Anneal
346	1	Y/Z/Y	Plain Si	500 Anneal
347	1	Y/Z/Y	Plain Si	500 Anneal
348	1	Y/Z/Y	Plain Si	500 Anneal EL test wafer P118
349	1	Y/Z/Y	Plain Si	500 Anneal EL test wafer P198
350	1	Y/Z/Y	Plain Si	500 Anneal EL test wafer P117
351	1	Y/Z/Y	Plain Si	500 Anneal EL test wafer P199
352	1	Y/Z/Y	Plain Si	500 Anneal EL test wafer POGS
353	1	Y/Z/Y	Plain Si	500 Anneal EL test wafer P200
354	1	Y/Z/Y/Z/Y	Set 3	700 Anneal
355	1	Y/Z/Y/Z/Y	Set 3	700 Anneal
356	1	Y/Z/Y/Z/Y	Set 3	700 Anneal
357	1	Y/Z/Y/Z/Y	PBL 1	700 Anneal PT mirrors removed
358	1	Y	Plain Si	500 Anneal
359	1	Y	Plain Si	500 Anneal
360	1	Z	Plain Si	500 Anneal
361	1	Z	Plain Si	500 Anneal
362	1	Y/Z/Y	Plain Si	CRAZED
363	1	Z	Plain Si	No Anneal
364	1	Z	Plain Si	No Anneal
365	1	Y/Z/Y/Z/Y	PBL 2	700 Anneal
366	1	Y/Z/Y/Z/Y	PBL 2	700 Anneal
367	1	Y/Z/Y/Z/Y	PBL 2	700 Anneal
368	1	Y/Z/Y	Plain Si	500 Anneal
369	1	Y/Z/Y/Z/Y	PBL 2	700 Anneal

370	1	Z	Plain Si	No Anneal
371	1	Y/Z/Y/Z/Y	Plain Si	700 Anneal
372	1	Y/Z/Y/Z/Y	Set 2	700 Anneal
373	1	Y/Z	Plain Si	No Anneal
374	1	Z	Plain Si	No Anneal
375	1	Y/Z/Y/Z/Y	PBL 1	700 Anneal
376	1	Y/Z/Y/Z/Y	PBL 1	700 Anneal
377	1	Y/Z/Y/Z/Y	PBL 1	700 Anneal
378	1	Y/Z/Y/Z/Y	PBL 1	700 Anneal