Feasibility of micro-mirror Laterally-Emitting Thin-Film Electroluminescent Devices for an Opto-Electronic Integrated Circuit

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Abstract

The design and development of micro-mirror Laterally-Emitting Thin-Film Electroluminescent (mmLETFEL) devices aiming at image bar array applications such as electrophotographic printing has been one of the main objectives for the Optical Device Engineering Group at The Nottingham Trent University. This thesis describes the work carried out in determining the potential and possibility of developing the current mmLETFEL technology as an integrated optical device. In particular, assessing the feasibility and commercial viability for a novel Opto-Electronic Integrated Circuit (OEIC) – the mmLETFEL device integrated with the corresponding drive circuitry.

The initial investigation explores the feasibility of the current LETFEL technology in producing sufficient emission for exposing a photoconductively charged photoreceptor. The luminance observed from the edge emission of a LETFEL test device, has been found to discharge a commercial photoconductive drum, at 50% gain, and at a print speed of 13 p.p.m.

The fabrication of mmLETFEL test devices that are suitable for integration has been successful. This includes pre-fabricating base electrodes of PolySi and TiW materials, defined prior to the deposition of the mmLETFEL structure, and with insulators of Y_2O_3 and Si_3N_4. Results from the electro-optical characterisation of these four configurations of mmLETFEL device structures have demonstrated that Y_2O_3 supersedes Si_3N_4 material as an appropriate dielectric, in that the luminance versus drive voltage (L-V) curve exhibits a comparatively steeper slope and lower device threshold, which are both desirable for mmLETFEL device activation. Characteristics of mmLETFEL test devices grown with base electrodes PolySi and TiW have been comparable, and this indicates that the deposition of these two materials have no significant effect on the mmLETFEL device performance.

SPICE modelling has been conducted on commercially available drivers from various fabrication houses based on the SPICE model parameters obtained from these manufacturers. Due to cost and technology accessibility, the 100V process DMOS device from Alcatel Mietec in Belgium has been selected for further investigation. Electrical characterisation and SPICE modelling have been performed on test dies (of the NDMOSHV model) obtained via EuroPractice. Comparison between the measured and simulated results shows a <10% error margin in the saturation region for the transistor output characteristics, and a <5% error margin for the transistor transfer characteristics.

This leads to circuit simulation using SPICE of the novel integrated mmLETFEL pixel – combining the developed mmLETFEL model and the optimised NDMOSHV model. By using previously characterised results of the mmLETFEL test devices to form a simple equivalent circuit, and the optimised SPICE parameters of the NDMOSHV model from Alcatel Mietec, the OEIC equivalent circuit has been developed and theoretically simulated for its performance.

Consequently, the processing route for an integrated mmLETFEL pixel is proposed, utilising the materials previously determined for the insulators and base electrodes. In addition, the results of the latest developments to the mmLETFEL technology from the aspects of fabrication, outcoupling efficiency, and overall performance, that are being investigated concurrently, have influenced the outcome of this research.

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Publications

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"Feasibility of Laterally-Emitting Thin-Film ElectroLuminescent (LETFEL) Devices for an Opto-Electronic Integrated Circuit (OEIC)"; P S Theng, W M Cranton, C B Thomas, C Tsakonas and R Stevens; *Proceedings of the Society of Information Displays Symposium (SID 2000), Long Beach, California, U.S.A.*

"An Integrated High-Resolution High-Intensity Micro-Mirror Laterally-Emitting Thin-Film Electroluminescent (mmLETFEL) Device for Electrophotographic Printing"; P S Theng, W M Cranton and C B Thomas; *under review at the time of writing.*

Statement of Work

Fabrication of the mmLETFEL test devices on silicon base wafers pre-fabricated with reflecting micro-structures and different base electrode materials, i.e. titanium/tungsten (TiW) and polysilicon (PolySi).

Optical (Luminance versus Drive Voltage) and Electrical (Charge versus Drive Voltage) Characterisation of the mmLETFEL test devices on silicon base wafers pre-fabricated with reflecting micro-structures, and with TiW and PolySi base electrode materials.

SPICE modelling of the mmLETFEL test devices and optimisation of the theoretical model, with the inclusion of the TiW and PolySi base electrode layers, using SmartSpice of the Virtual Wafer Fabrication (VWF) software from Silvaco International.

SPICE modelling of the various high-voltage drivers, which technologies and SPICE model parameters have been obtained from various fabrication houses, e.g. Holtek, UMC, Supertex, and Alcatel Mietec.

Electrical Characterisation of the selected Alcatel Mietec driver test die, obtained via EuroPractice, using the TECAP system from Hewlett-Packard in RAL, Oxford.

Optimisation of the SPICE model of the corresponding Alcatel Mietec driver test die obtained via EuroPractice.

SPICE modelling of the integrated mmLETFEL cell, consisting of an individual mmLETFEL test device with its corresponding drive circuitry, utilising the previously optimised model parameters.

Calibration and Optimisation of the dicing parameters for the Sola Basic Tempress diamond saw system for the dicing operation of mmLETFEL test devices.

Calibration and Optimisation of the wire-bonding parameters for the K&S wedge-bonder system for the wire-bonding operation of mmLETFEL test devices onto chip-carriers.

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List of Abbreviations

A.C.	Alternating Current
ACTFEL	Alternating Current Thin-Film ElectroLuminescent
AMEL	Active Matrix ElectroLuminescent
APCVD	Atmospheric Pressure Chemical Vapour Deposition
arb	Arbitrary
CAD	Circuit Aided Design (or) Cathodic Arc Deposition
CMF	Central Microstructures Facilities
CMOS	Complementary Metal-Oxide-Semiconductor
C-V	Capacitance-Voltage
CVD	Chemical Vapour Deposition
D.C.	Direct Current
DMOS	Diffused Metal-Oxide-Semiconductor
eeLETFEL	edge-emitting Laterally-Emitting Thin-Film ElectroLuminescent
EL	Electroluminescence
GRIN	Graded Refractive Index Number
HMD	Head-Mounted Displays
hvnMOS	high-voltage n-channel Metal-Oxide-Semiconductor
I.C.	Integrated Circuit
I-V	Current-Voltage
LED	Light Emitting Diodes
LETFEL	Laterally-Emitting Thin-Film ElectroLuminescent
LPCVD	Low Pressure Chemical Vapour Deposition
L-V	Luminance-Voltage
MBE	Molecular Beam Epitaxy
mmLETFEL	micro-mirror Laterally-Emitting Thin-Film ElectroLuminescent
MOCVD	Metal Organic Chemical Vapour Deposition
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	n-channel Metal-Oxide-Semiconductor
NMRC	National Microstructures Research Centre
OEIC	Opto-Electronic Integrated Circuit
PECVD	Plasma Enhanced Chemical Vapour Deposition
PL	Photoluminescence

List of Abbreviations (Continued)

PLZT	Lead Lanthanum Zirconate Titanate
PMOS	p-channel Metal-Oxide-Semiconductor
Q	Square waveform
Q-V	Charge-Voltage
r.f	Radio-Frequency
RAL	Rutherford and Appleton Laboratories
RIE	Reactive Ion Etching
S	Sinusoidal waveform
SEM	Scanning Electron Microscopy
SLA	SELFOC Lens Array
SOI	Silicon-on-Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
T	Triangular waveform
TAT	Tri-layer Titanium/Tungsten-Aluminium-Titanium/Tungsten
TECAP	Transistor Electrical Characterisation and Analysis Package
TFEL	Thin-Film ElectroLuminescent
TNTU	The Nottingham Trent University
UV	Ultra-Violet
vmLETFEL	vertical micro-structures Laterally-Emitting Thin-Film ElectroLuminescent
VWF	Virtual Wafer Fabrication

List of Symbols

Al	Aluminium
Ar	Argon
As_2Se_3	Amorphous Selenium
a-Si:H	Hydrogenated Amorphous Silicon
Au	Gold
$BaTiO_3$	Barium Titanate
BCl_3	Barium Chloride
CCl_3	Calcium Chloride
CF_4	Carbon Tetrafluoride
CHF_3	Freon 23
Cl_2	Chlorine
H_2	Hydrogen
He	Helium
ITO	Indium Tin Oxide
Mn	Manganese
N_2	Nitrogen
N_2O	Nitrous Oxide
Ne	Neon
NH_3	Ammonia
O_2	Oxygen
PolySi	polysilicon
Se	Selenium
Si	Silicon
Si_3N_4	Silicon Nitride
$SiCl_4$	Silicon Tetrachloride
SiH_4	Silane
SiO_2	Silicon Dioxide
SION	Silicon Oxynitride
TiW	Titanium/Tungsten
T_{OX}	Thermal Oxide
Y_2O_3	Yttrium Oxide

List of Symbols (Continued)

Zn	Zinc
ZnS	Zinc Sulphide
ZnS:Mn	Manganese doped Zinc Sulphide
ZnSe	Zinc Selenide

List of Units

Ω	Ohms
°C	Celsius
°F	Fahrenheit
A	Ampere
Å	Angstrom
a.u.	Arbitrary Unit
C	Coulomb
Cd	Candela
d.p.i.	Dots Per Inch
eV	Electron Volts
F	Farads
fL	Foot-Lamberts
Hz	Hertz
J	Joules
l	Litres
lm	Lumens
p.p.i.	Pixels Per Inch
p.p.m.	prints/pages per minute
sccm	Standard Cubic Centimetre
V	Volts
W	Watts

List of Constants & Variables

ρ	Resistivity of a given material
$\rho(x)$	Resistivity as a function of distance x into a given material
ε_0	Permittivity of Vacuum at 8.854×10^{-12} Fm^{-1}
η_{eff}	Luminous Efficiency
ε_i	Dielectric Constant of an Insulator
ε_p	Dielectric Constant of a Phosphor
ΔQ	Transferred Charge Density
ε_r	Relative Permittivity of a given material
Δw_a	Average Width of Emitting Aperture
Δx	Average Width of Aperture
A	Area
A_c	Area of Focusing Circle of luminance metre
A_{dpi}	Active Area of a given material at a given resolution in d.p.i.
A_{emit}	Area of mmLETFEL test device Emitting Aperture
BV_{diode}	Breakdown Voltage of the zener diodes
C	Capacitance
$C[v_L(t)]$	Dynamic Capacitance across the mmLETFEL test device
C_{dpi}	Capacitance of a given material at a given resolution in d.p.i.
C_i	Insulator Capacitance
C_{off}	Total Capacitance before device turn-on
C_{on}	Total Capacitance after device turn-on
C_p	Phosphor Capacitance
C_s	Sense Capacitor
d	Thickness of a given layer
D	Zener Diodes of a mmLETFEL equivalent circuit
d_i	Thickness of an Insulator
d_p	Thickness of a Phosphor
E_i	Electric Field of an Insulator
E_{in}	Input Energy Density
E_p	Electric Field of a Phosphor
f	Drive Frequency

List of Constants & Variables (Continued)

G	Gain or sensitivity of photoreceptor in percentage
h_l	Height of Microlens
h_{pl}	Height of Planarisation layer
i(t)	Instantaneous Current
I_{ds}	Drain-Source Current of a transistor
K	Factor of Luminance
l	Length of a mmLETFEL device
L	Luminance at any given voltage
L_{diff}	Luminance range between 'ON' and 'OFF' states
$L_{corrected}$	Corrected Luminance
$L_{measured}$	Measured Luminance
L_{Vm}	Luminance at a Modulated Voltage of V_m
P_{in}	Power Dissipation / Power Consumption / Input Power Density
Q	Charge
q(t)	Instantaneous Charge
Q'	Charge Density remaining after drive voltage goes to zero
Q_{pk}	Charge Density at the Peak Voltage of V_{pk}
Q_{th}	Charge Density at the Threshold Voltage of V_{th}
Q_{to}	Charge Density at the Turn-on Voltage of V_{to}
R_c	Sense Resistor
R_{dpi}	Resistance of a given material at a given resolution in d.p.i.
R_e	Resistance of top electrode of a mmLETFEL device
R_i	Insulator Resistance
R_m	Resistance of base electrode of a mmLETFEL device
R_p	Phosphor Resistance
R_s	Series Resistor
R_{sh}	Sheet Resistance of a given material
R_z	Resistance associated with hot-electron emission at interface states
S	Drum speed in p.p.m.
t_s	Travelling speed of photosensitive material under test
V_0	Initial potential of photosensitive material after charging
$v_1(t)$	Drive Voltage

List of Constants & Variables (Continued)

$v_2(t)$	Voltage at node of contact to mmLETFEL Top Electrode
$v_3(t)$	Voltage at node of contact to mmLETFEL Base Electrode
V_d	Discharged voltage of photosensitive material
V_{diff}	Switching voltage range for a hvnMOS device
V_{ds}	Drain-Source Voltage of a transistor
V_{exc}	Excitation/Drive Voltage
$V_{exc(pk\text{-}pk)}$	Peak-to-peak excitation/drive voltage
V_{gs}	Gate-Source Voltage of a transistor
$v_L(t)$	Voltage Drop across mmLETFEL Test Device
V_{letfel}	Voltage across a mmLETFEL device
$V_{letfel(pk\text{-}pk)}$	Peak-to-peak voltage across a mmLETFEL device
V_m	Modulated Voltage
V_p	Voltage Drop across the Phosphor Layer
V_{pk}	Peak Voltage
V_r	Residual voltage on photosensitive material after discharging
V_{th}	Threshold Voltage
$V_{th(pk\text{-}pk)}$	Peak-to-peak threshold voltage
$V_{th,ph}$	Threshold Voltage for the Phosphor Layer
V_{to}	Turn-on Voltage
W	Width of mmLETFEL test device
w	Width of a mmLETFEL device
w_a	Width of Emitting Aperture
w_{bp}	Width of Black Polyamide
w_d	Drain Width of a transistor
w_g	Pitch of Waveguides
w_l	Base diameter of Microlens
w_{mc}	Width of micro-mirror metallised coating
w_{mm}	Width of micro-mirror
w_s	Width of Sidewalls

Contents

1 Introduction

1 INTRODUCTION

Alternating Current Thin-Film ElectroLuminescent (ACTFEL) devices – consisting of a phosphor layer sandwiched between two insulating layers and from which light is produced upon application of an electric field across the structure – had been demonstrated to emit light laterally, at an order of magnitude greater than the conventional surface emission, due to the inherent wave-guiding property in these devices. [1]

As a result of this observation, edge-emitting TFEL devices had been proposed as an alternative low-cost optical image bar array in electrophotographic printing.[2, 3, 4] However, these edge-emitting devices required the formation of an emitting facet on a glass substrate, which can be problematic. Therefore, a more elegant and potentially more reliable technique would be to redirect this laterally emitted light from the substrate via reflecting microstructures, termed as Laterally-Emitting TFEL (LETFEL) devices. [5, 6, 7, 8, 9]

The outcoupling of this useful lateral emission using the micro-mirror Laterally-Emitting Thin-Film ElectroLuminescent (mmLETFEL) technology not only increases the overall luminance of the device, but with a significant reduction in the active area required to produce the same intensity, can lead to the achievement of higher resolution devices.[10, 11]

Thus, there is the potential of developing this mmLETFEL technology into high-intensity high-resolution linear bar arrays,[12] as the use of Silicon (Si) substrates and standard Si fabrication processes yields the potential for integration of driver electronics within the same device. This eliminates the need for external electronic drive circuits, minimising the cost of manufacture and assembly, as well as the complexity of external yield-damaging wire-bonds. Furthermore, continuous research has produced more efficient mmLETFEL devices, [13, 14, 15, 16] thereby providing the possibility of mmLETFEL devices being developed into high-intensity integrated light source as an alternative image bar array in electrophotographic printing.

Hence, the main objective of this research is to assess the feasibility and commercial viability of developing the current mmLETFEL technology into an integrated mmLETFEL device termed as the Opto-Electronic Integrated Circuit (OEIC) – consisting of a mmLETFEL pixel defined in the same device with its corresponding drive electronics.

The investigation into developing this OEIC for optical image bar applications, i.e. electrophotographic printing, is analysed and assessed by fabrication, characterisation and modelling of mmLETFEL test devices on Si wafers with pre-fabricated base electrodes, characterisation and modelling of commercially available drivers. Finally demonstration has been made of the overall working principle via theoretical simulation of the OEIC equivalent circuit.

The following sub-sections are introduced to give a brief review and understanding of the background surrounding the investigation to be undertaken, i.e. the electrophotographic printing process, ACTFEL and LETFEL technologies, and mmLETFEL printhead prototype development. The chapter concludes with an outline of the objectives of the research to be carried out and an overview of the contents of the remaining chapters in the thesis.

1.1 REVIEW OF ELECTROPHOTOGRAPHIC PRINTING

1.1.1 Background

In the 1930's, the only available copying method was the photostat process based on silver halide photography, where reproduction could take days and the availability of the service was limited. [17] The need for a simple and inexpensive device that would allow any type of document to be copied led to the invention of electrophotography by Chester Carlson in 1937.[18] His review[19] in the history of charged powder development from Selenyi[20] to as far back as Lichtenberg,[21] gave him the idea of forming electrostatic latent images using photoconductivity to selectively discharge a surface-charged insulator; and of developing this latent image by dusting with powders charged electrostatically.

During the 1950's and 1960's, major companies such as Xerox, Eastman Kodak, IBM and RCA, recognised the potential of Carlson's discovery and were primarily interested in copying. However, IBM was soon interested in developing faster computer printers and was then licensed by Xerox for research and development in electrophotography targeted at printer applications. IBM concentrated research on organic photoreceptors, mono-component development systems and a means of electro-optically forming the latent image on the photoconductive surface.

In 1973, Xerox introduced the first modern electrophotographic printer, the model 1200. By 1975, and 1976, IBM and Canon introduced the first laser-based electrophotographic computer printer, the model IBM 3800 with a speed of 215 pages per min (ppm), and the model Canon LBP2000 C1 operating at 31 ppm,[22] with both using HeNe gas lasers to address the photoconductive drum. By then, it was thought that the electrophotography technology had matured, and research had ceased.

However, in the late 1970's, interest in further research in electrophotography was fueled by the development of other alternative technologies to challenge the laser electrophotography, such as ionography (research and manufacture by Delphax Systems),[23] and magnetography (work by Bull Peripheriques),[24] hence renewing the attention and significantly heightening the commercial value of electrophotographic technology.

Further, a fourth printing technology, bubblejet (produced by Canon and Hewlett-Packard in the early 1980's),[25] introduced the use of semiconductor lasers in place of gas lasers, which can be packaged in transistor-size containers and can be modulated by current-control.

By the mid-1980's, the laser-spinning polygon system was found to be able to be replaced with an all-solid-state device. An array of liquid crystal shutters was used to address the photoreceptor, with a uniform light source behind the shutters and a SELFOC Graded Refractive Index Number (GRIN)[26] lens in the front for the imaging.

The first products using this light shutter technology were manufactured by Epson and Casio, but only up to 7 ppm and 9 ppm respectively.[27, 28, 29] Then, Oki Electric and NEC introduced printers utilising light-emitting diode (LED) arrays, with a print speed of 10 ppm and 8 ppm respectively.[30, 31] IBM and Eastman Kodak too, introduced their new LED printers at 12 ppm, and 92 ppm respectively.[32, 33] In order to compete with the laser-polygon systems, these "image bar" technologies had to maintain a sufficient light uniformity and the interconnection of light elements to driver electronics at an affordable cost.

1.1.2 Electrophotographic Printing Process

Electrophotography is defined as those processes involved that utilise the interaction of light and electricity as basic elements for image formation.[34] Xerography describes those processes involved in the creation of electrostatic charge patterns on surfaces of photoconducting insulators.

The electrostatic image is formed by first charging and then exposing a photoconductive insulating surface to a light pattern. The image is developed, transferred to paper, and then fused onto it. The photoconductive insulator can be used many times to produce thousands of prints. **Figure 1-1** shows a typical configuration of an electrophotographic printer in its cross-sectional view.

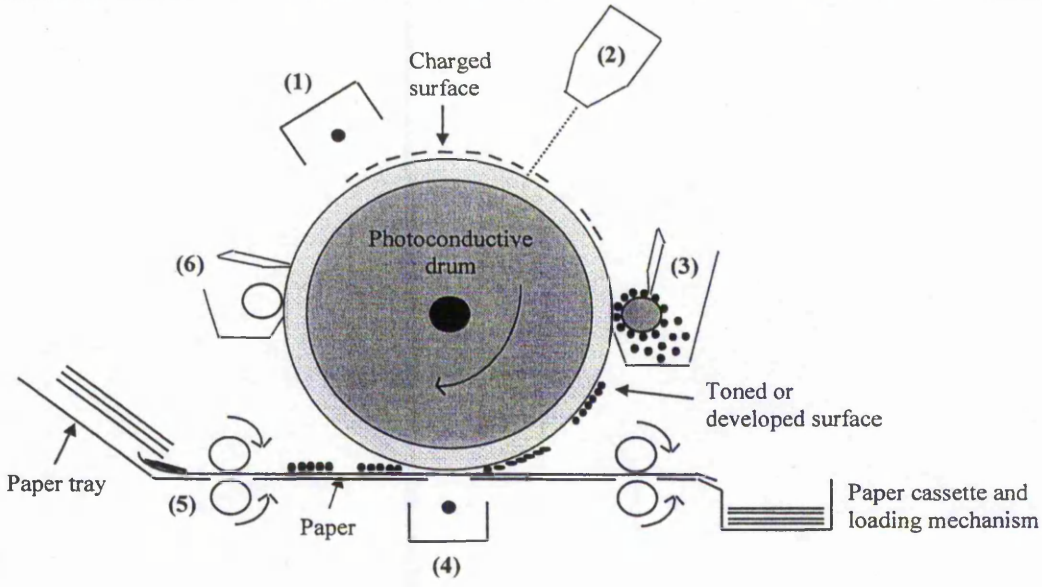


Figure 1-1: Six distinct steps of the electrophotographic printing process

There are six distinctive steps to the process, and a brief description is given in the following, where the numbers correspond to the ones in bold brackets in **Figure 1-1.**

1. *Charge*

   A corona discharge caused by air breakdown uniformly charges the cleaned surface of the rotating photoconductive drum.

2. *Expose*

   Light discharges the insulating photoconductive drum, producing a latent image. At selected positions along the drum (at any one time), regions are either exposed or not. Photons absorbed by the photoconductive drum generate electron-hole pairs, and when these free carriers are swept to the respective anode or cathode, charge recombination occurs. Selective reduction of surface charge across the drum builds up the electrostatic latent image.

3. *Develop*

   In regions where the Coulombic force is sufficient, the electrostatically charged toner particle is attracted to the photoconductive surface, i.e. the electrostatic latent image, thus transforming it into a real image.

4. *Transfer*

   The back of the paper is first corona charged with a charge opposite to that of the toner particles. Another Coulombic force pulls the paper against the toned photoconductor surface, thus allowing transfer of the toner from the drum to paper.

5. *Fuse*

   The transferred toner, which is electrostatically held on the paper, is fused onto the paper permanently by heating the back surface in a heated roller system. The toner becomes soft and flows into the matrix of the paper. The perceived blackness of the image is due to the decreased reflectance of the paper caused by the toner.

6. *Clean*

   Before the drum is reused, any excess toner left on the photoconductive drum is cleaned out by discharging and physically cleaning it using a cleaning blade.

As a result, an electronically stored image is printed onto normal untreated paper.

1.1.3 Photoreceptors

There are 2 types of photoreceptors: inorganic photoreceptors and organic photoreceptors.

The very first inorganic photoreceptors used in copying machines were amorphous selenium (Se), however above 550nm wavelength, its sensitivity decreases significantly.[35] Developed later was a new inorganic photoreceptor – hydrogenated amorphous silicon (a-Si:H), a material produced by r.f. glow discharge decomposition of SiH_4.[36] Advantages reported include good sensitivity over a broad range, i.e. 450 nm – 750 nm, and due to its hardness, a longer lifetime compared to amorphous Se photoreceptors.

Organic photoreceptors for electrophotography were first introduced by IBM.[37] It is made of a 2-layer structure; a thin photogeneration layer (usually of <1μm thickness), and a transport layer (usually of ≈20μm) made from doped polymer. Manufacturers have different materials systems; thus various polymers were developed and used as the transport layers for these organic photoreceptors.

As semiconducting lasers was developed and used as the light source for electrophotography, their output wavelength at 800nm required further development into infrared-sensitive photoreceptors. Research was revolved around searching for alternative photoreceptors by either extending the spectral response of inorganic photoreceptors, or finding new photogeneration molecules for organic photoreceptors.

Therefore, depending on the light source used in electrophotographic printers, and their respective output wavelengths, the photoreceptors to be used as printer drums must have the corresponding and suitable spectral response range.

1.1.4 Light Sources

In a further review to Section 1.1.1 on the background of the electrophotography technology, the various generations of light sources being utilised in laser printers can be summarised as follows.

The very first low-cost laser printers utilised the HeNe gas laser as the light beam, and the electro-optic modulator. By the late 1970's, semiconducting lasers were feasible in replacing these gas lasers; and in 1983, Canon produced a printer utilising a semiconducting laser, equipped with associated lens and a spinning polygon system.

Following this, the image bar exposure system emerged, where linear arrays of light controlling emitting elements were focused across the full length of the photoconductive drum. This light was imaged optically onto the drum by using the SELFOC Graded Refractive Index Number (GRIN) lens. The GRIN lens array technology is composed of one or two rows of SELFOC graded-index micro-lenses; each with equal dimensions and optical properties. It is a simplified optical system used as a scanning device for copiers, facsimiles and printers; giving a 1:1 focusing with an acceptance angle (viewing angle) of 6°-20°.[38]

At present, there are 2 types of image bars: non-emissive and emissive. Apart from the Liquid Crystal Shutter arrays mentioned earlier,[27, 28, 29] other alternative non-emissive image bars have been investigated which are based on Lead Lanthanum Zirconate Titanate (PLZT) Ceramic Shutter arrays,[39, 40] Magneto-Optic Shutter arrays,[41, 42] and Linear Spatial Light Modulators.[43, 44, 45] However, these non-emissive image bar arrays require an additional uniform light source behind the array. Thus, this accounts for the increase in size as well as the cost of such systems.

An emissive image bar array utilising the Light-Emitting Diode arrays,[30, 31, 32, 33] has been an approach adopted by Oki Electric, NEC, IBM and Eastman Kodak. However, coupling efficiency is low and external electrical connections between each LED element and its driver die results in yield-damaging wirebonds, and thus maintaining a sufficient and uniform light source along the length of the array proved to be a challenge. Although these problems have been overcome, there is still the issue of LED lifetime and interconnection techniques.

Edge-Emitting Technology on Glass arrays,[46, 47, 48, 49, 50, 51] a technique of fabricating edge-emitting ACTFEL structures onto a glass substrate, is another emissive technology researched by Westinghouse, later known as Edge-Emitting Technology Inc.

As with the LED image bar array technology, the high number of high density wire-bonds needed for interconnection between each individual light source and its corresponding driver electronics poses problems for manufacturing higher resolution and yet low cost systems. An additional problem is the difficulty in defining the edge-emitting facet on a glass substrate, thus affecting the light outcoupling from the element to the photoconductive printer drum via the imaging GRIN lens.

Hence, to overcome such problems, research here has been concerned with developing an image bar array based on Alternating-Current Thin Film Electroluminescent (ACTFEL) for Laterally-Emitting TFEL (LETFEL) devices, but aiming at using standard Si fabrication processes in an attempt to reduce problems associated with fabrication on glass substrates. Also, the possibility of integrating these LETFEL devices with their individual driver die can prove to be a breakthrough in reducing the density and complexity of interconnects which otherwise would conventionally be unavoidable.

The background and research details of work carried out so far on both the ACTFEL and LETFEL technologies aiming at image bar arrays are discussed in the following subsections.

1.2 Review of Alternating Current Thin-Film Electroluminescent Devices

1.2.1 Introduction

The effect of a non-thermal generation of light resulting from the application of an electric field to a substance is called ElectroLuminescence or EL. This phenomenon was first discovered by a French physicist, Destriau, in 1936.[52] He observed that light was emitted when a large electric field was applied to a ZnS compound.

Initially, efforts to utilise this phenomenon of EL were focused on powder EL devices, but with the introduction of thin-film process technology in the 1960's, as well as reports on the high-luminance and long-lifetime of a.c. thin-film EL devices in 1974,[53] the majority of the development efforts have since then been concentrated on thin-film EL devices.

Primarily, as in this investigation, EL is referred to as high-field electroluminescence where light is generated by impact excitation of a light-emitting centre by high-energy electrons.

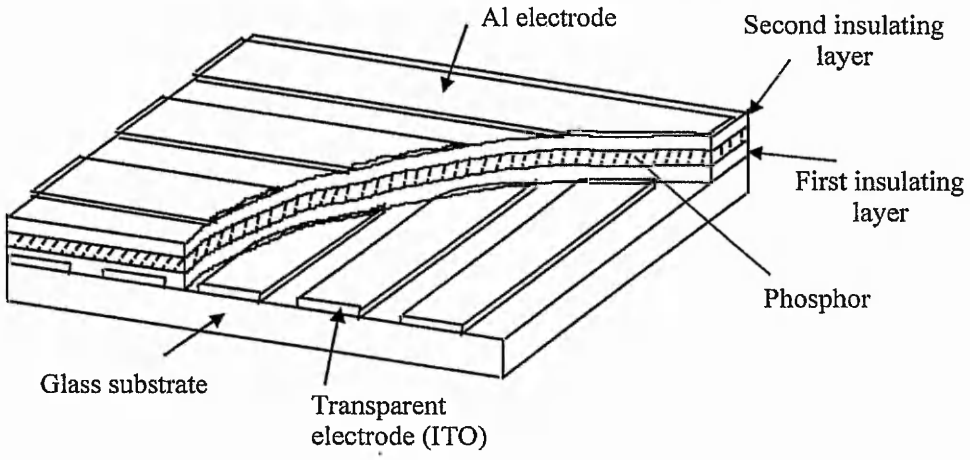


Figure 1-2: Structure of a double-insulating-layer type ACTFEL device

The thin-film EL structure is made up of basically three layers: the phosphor layer sandwiched between two insulating layers (which act as current-limiting layers thus realising a more reliable device), fabricated onto a glass substrate. When an electric field is applied across it, EL emission is realised and observed. The conventional structure of the ACTFEL is shown in **Figure 1-2**, which was used to form a flat panel display.[54]

In a conventional double-insulating-layer type thin-film EL device, the lower electrode is usually of transparent indium tin oxide (ITO) and the upper electrode is of Aluminium (Al) – at least one set of the electrodes being transparent to allow the emitted light be viewed. The total thickness of this thin-film structure is no more than 2μm, thus giving a low diffuse scattering of ambient light.

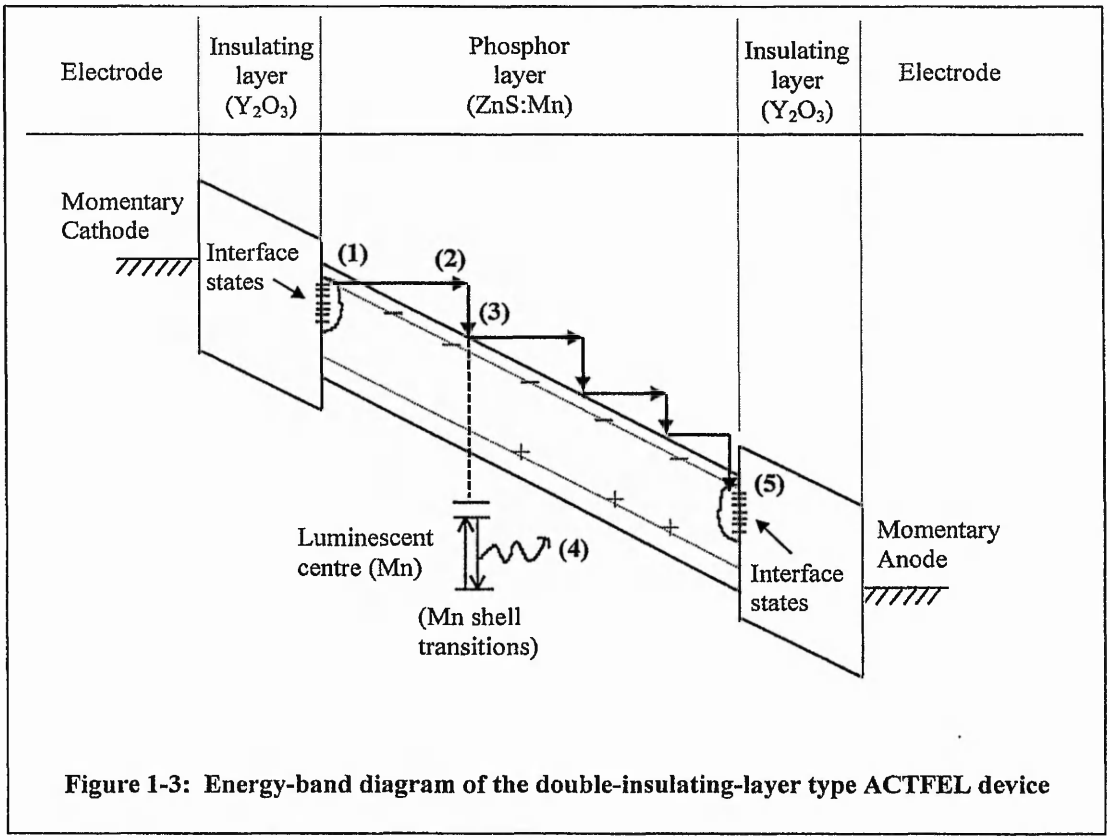


Figure 1-3: Energy-band diagram of the double-insulating-layer type ACTFEL device

The emission mechanism of an ACTFEL device, which is generally accepted for ZnS-based EL devices, [1, 55, 56, 57, 58] can be explained with reference to **Figure 1-3**, where the following numbers correspond to the ones in bold brackets in the corresponding figure:

1. *Tunnel Emission*

   When the applied voltage across the device exceeds the threshold voltage, electrons are injected from the insulating/phosphor layer interface states by high-field assisted tunnelling. Field emission of the electrons from donor traps occurs at the interface appropriate to the momentary cathode of the device.

2. *Acceleration*

   The injected electrons are then accelerated. The large kinetic energy gained (>2.4eV) during this process is sufficient to excite the luminescent centres (or host lattice).

3. *Impact Excitation*

   These high-energy electrons (or hot electrons) directly excite the luminescent centres through the impact-excitation mechanism.

4. *Radiative Decay of Mn Centres*

   The kinetic energy is transferred to the potential energy of a valence electron in the Mn shell. When these electrons in the excited states make radiative transitions to the ground state, EL emission is realised.

5. *Electron Capture by Interface States*

   When the hot electrons travel through the phosphor layer and reach the momentary anode, they are trapped by trapping centres at the phosphor/insulator layer interface states. These electrons accumulate at the interface for a period of time. As a result, internal polarisation occurs.

When the polarity of the a.c. voltage waveform is reversed (the next half cycle), the effective internal electric field is increased by additive polarisation due to the superposition of the previous counter polarisation. The same process occurs in the opposite direction.

1.2.2 Previous Work on ACTFEL devices as image bar arrays

Due to Smith's observation[1] of the higher component in lateral emission, a proposal was made that this laterally emitting light produced within the phosphor layer and decoupled in a direction parallel to the thin-film plane, be outcoupled onto the photoconductive drum of an electrophotographic printer. Thus, the edge-emitting technology was created by the people at Westinghouse in 1986, and these edge-emitting device structures have since then been covered by a series of patents.[59] **Figure 1-4**(a) shows the edge-emitter concept, and **Figure 1-4**(b) shows the edge-emitter array, where the light is being emitted at the edge of every pixel.

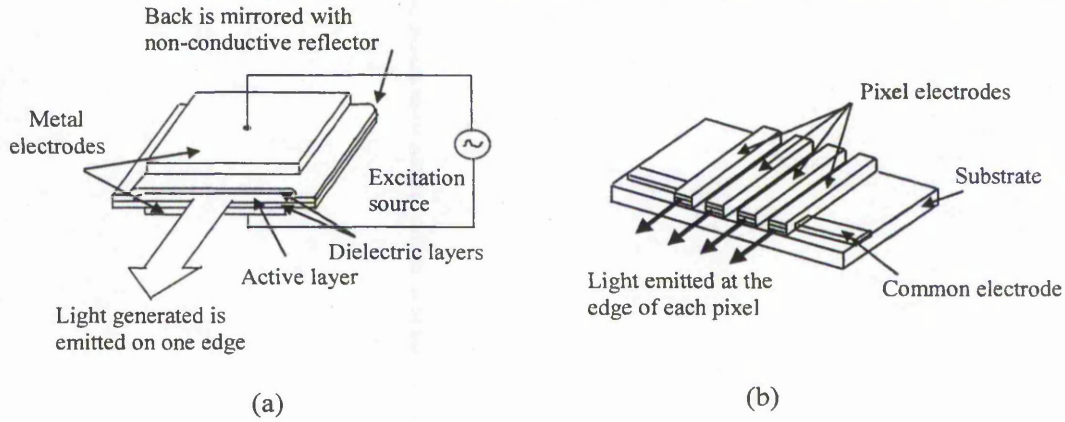


Figure 1-4: (a) Schematic illustration of the TFEL edge-emitter concept (b) Schematic arrangement of an edge-emitter array

The formation of these devices with such an edge-emitting facet, however, caused problems in obtaining good outcoupling of light at the edge-emitting aperture. The scattering of light that was observed limited the efficiency that could be obtained. Due to these problems, an alternative test printhead was investigated utilising the LETFEL devices pre-fabricated on micro-mirrors instead.

1.2.3 Current Work on Active Matrix Electroluminescent Displays

It has been reported that the combination of active matrix circuitry and thin-film electroluminescent technology is ideal for head-mounted displays (HMD's) applications due to the advantages of obtaining a high resolution, light weight, and low power device.[60] The AMEL device is realised by fabrication of the driver electronics for the display on an IC wafer, i.e. using Silicon-on-Insulator (SOI) technology, and then overlaying the thin-film EL structure on the top to produce a fully integrated emissive display. This method of integration using SOI technology can overcome the limitation of achieving a minimum pitch of the interconnects to external drive electronics since the driver electronics are now fabricated onto the wafer, thus forming the substrate for the AMEL device. The AMEL device structure is briefly illustrated in **Figure 1-5**.

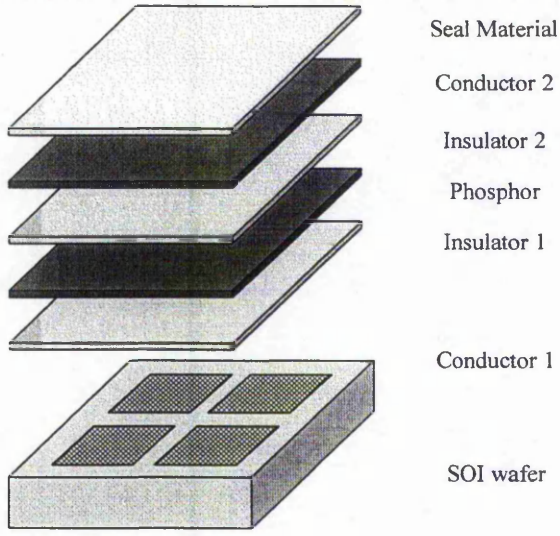


Figure 1-5: The active matrix thin-film EL (AMEL) device structure

SOI wafers have good isolation capabilities, making it possible to effectively isolate high voltage structures in each pixel from each other. At the same time, it is also able to isolate high voltage illumination lines from the low voltage logic lines in a typical display configuration. However, one major constraint is the packing density limitation of the SOI technology, thus restricting very small pixel pitch to be achieved with this method. Although there have been reports on the basic requirements of the driver but there is insufficient documentation on how the design has been achieved. Since the mmLETFEL to be investigated for integration purposes are the linear array devices, thus research into the development of an integrated mmLETFEL with commercial drivers is proposed.

1.3 Review of Laterally-Emitting Thin-Film Electroluminescent Devices

1.3.1 Introduction

Observation has been reported previously that the luminance of the laterally emitted light of an ACTFEL device is more intense by at least a factor of three.[3, 10, 11] Only about 10% of the generated light was actually emitted and observed as surface emission, while the rest was contained within the phosphor layer, and guided laterally within the step index multimode planar waveguide.[61]

As such, the concept of a micro-mirror structure – fabricated prior to the deposition of the conventional 3-layer thin-film EL device – to permit emission of this lateral light, was conceived; and these devised structures have been covered by various patent applications.[5, 6, 7]. Consequently, the proposed micro-mirror structure to be fabricated within the thin-film EL – micro-mirror LETFEL (mmLETFEL) technology – was developed. This facilitates the use of the laterally transmitted light by way of reflection off the micro-mirror structures via a defined emitting aperture, hence providing higher intensity surface emission.

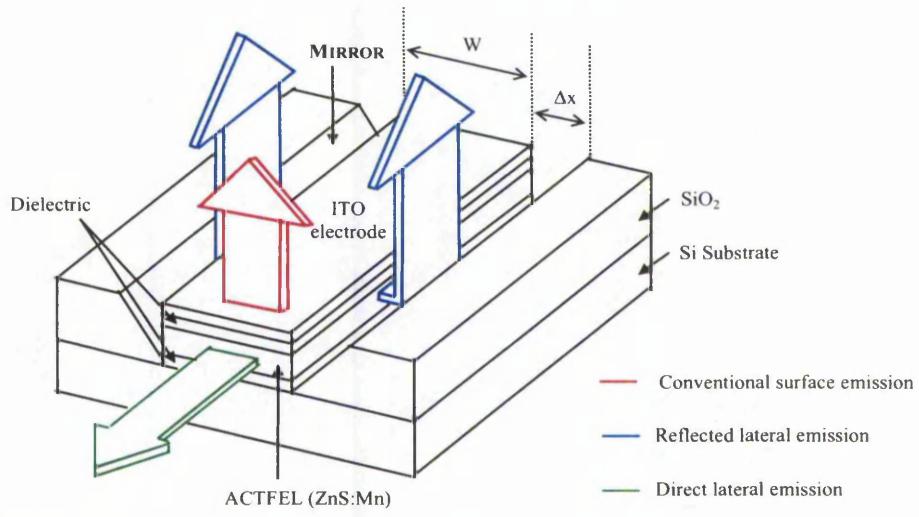


Figure 1-6: A mmLETFEL device with micro-mirrors to reflect the lateral emission (W is the device width, and Δx is the aperture width)

A schematic diagram of a single mmLETFEL pixel is shown in **Figure 1-6**, where the conventional surface, reflected lateral, and direct lateral, emissions, have been indicated. From the diagram, when viewed from the top of the device, the lateral emission component increases the overall luminance of the device. The lateral emission is reflected by the micro-mirrors fabricated at the edges of the pixel, facilitating the addition of two useful light components: laterally-emitting and surface-emitting. With the device configuration illustrated above, higher resolution pixels can be fabricated, specifically for displays application, as shown below in **Figure 1-7**.

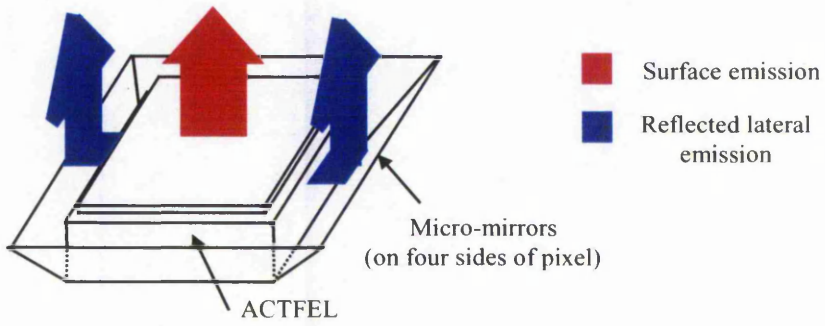


Figure 1-7: ACTFEL pixel structure utilising reflected lateral emission for high resolution display devices

Essentially, a mmLETFEL linear-array device, specifically for electrophotographic printing application, consists of two ACTFEL pixels feeding into one micro-mirror where lateral emission is outcoupled at the reflecting micro-structure aperture. This device configuration eliminates the need for defining an edge-emitting facet, as the light is being wave-guided within the device and outcoupled via the defined emitting aperture. Moreover, this wave-guiding effect of the mmLETFEL device can be fully utilised by increasing the active light-emitting volume, i.e. the active material length, thus increasing the luminance at the aperture.

Thus far, the mmLETFEL device structure consists of a ZnS:Mn phosphor layer at 0.8μm thickness, the two Y_2O_3 dielectric layers on either side at 0.3μm thickness, and a top Al electrode at 0.8μm thickness. This structure is fabricated on a silicon wafer pre-fabricated with a layer of PECVD SiO_2 at 1.5μm thickness to form micro-mirrors with a base width of 3μm, thus yielding a reflecting angle of 45°.

Recent developments to the technology yielded an improved structure containing a 'barrier-layer' phosphor.[14] The inclusion of this 'barrier-layer', typically a 100Å Y_2O_3 dielectric layer, enables hot electron tunnelling to occur at the barrier-layer, causing the energetic electrons to tunnel into the adjacent phosphor region. This mechanism has been shown to be responsible for a two-fold increase in luminance, with only a 10% increase in threshold voltage.[62] Shown in **Figure 1-8** is the enhanced 'barrier-layer' phosphor mmLETFEL device structure with micro-mirror technology.

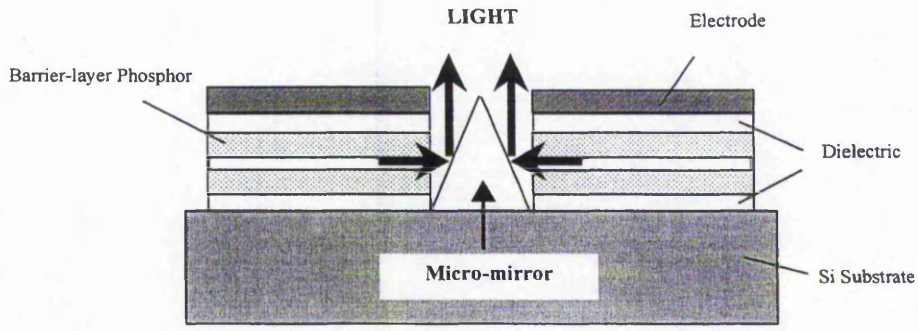


Figure 1-8: The enhanced 'barrier-layer' phosphor mmLETFEL device

Concurrently, the following are the prime concerns of the TNTU Optical Device Engineering Research Group pertaining to the overall performance of the mmLETFEL technology, and hence are being explored simultaneous to this research programme:

1. The overall luminance achieved with this structure - which is heavily dependent on the fabrication route of the mmLETFEL technology.[63]
2. The outcoupling efficiency of these devices via the reflecting mirror structures - the ion-milling technique has been proposed for the aperture definition process.[64]
3. The annealing step necessary for device light activation – due to the high temperature involved in thermal annealing, an alternative is to use laser annealing.[65, 66]
4. The degradation mechanism of these devices – electrical and lifetime characteristics of these devices are being examined.[67]
5. Alternative etching technique, i.e. reactive ion etching (RIE) for definition of the emitting aperture.[68]

The details of the results of these investigations are included in the concluding chapter where appropriate and where these findings have influenced the outcome of this particular investigation.

1.3.2 Previous Work on mmLETFEL linear-array devices

Research and development on mmLETFEL devices have thus far been targeted primarily at head-mounted displays, however, the development of the prototype of the mmLETFEL image bar array for electrophotographic printing application has also occurred.

There had been two main considerations for the design of the mmLETFEL linear-arrays: the optical power requirements of commercially available photosensitive drums needed for light discharge in order to form a latent image on the drum, and the brightness requirements of mmLETFEL devices needed for such a discharge to occur.

Previous research work has resulted in a prototype mmLETFEL test linear-array with a resolution of 600 d.p.i. and a die dimension of 4.1 mm x 1.2 mm, fabricated with features which include active material lengths of 250μm on either side of the micro-mirror, micro-mirror structure with a base width of 3μm and a height of 1.5μm, emitting aperture of 3μm in width and of 32.3 μm in length, and a pixel pitch of 42.5μm. A description and view of the mmLETFEL linear devices and test devices on a test wafer is detailed in Chapter 3, where the characterisations of these devices are included.

Although the proposed printhead utilising mmLETFEL devices can eliminate the need for edge-emitting facet formation, the problem with yield-damaging wire-bonds still persists. In order to overcome the many interconnections needed for external drive circuitry, an integrated mmLETFEL printhead is proposed. And this forms the core of the investigation to be carried out in this research programme.

1.4 OVERVIEW

1.4.1 Objectives of the Investigation

It has been demonstrated thus far, that the current mmLETFEL technology which involves utilising micro-mirrors fabricated within the device structure to reflect the lateral component, can be developed into high-intensity and high-resolution linear bar arrays.

To maintain high resolutions for printing, aperture dimensions of the defined mmLETFEL emitting facets should be small, and brightnesses should be high. In practice, however, achieving the optimum feature of a mmLETFEL structure to produce maximum brightness at minimum loss (maximum efficiency) involves taking into account several factors, such as the light outcoupling efficiency and the light confinement within the structure. Therefore, mmLETFEL test devices will be fabricated with various device features for characterisation of these test devices to take place.

Correspondingly, methods have been devised for optimisation of the micro-mirror, and eventually micro-lensed,[69, 70] LETFEL structure, aimed at electrophotographic printing application. The following **Table 1-1** lists the various considerations taken into account and the differing features employed, in developing the mmLETFEL test devices – where italicised, the stated mmLETFEL feature has yet to be implemented.

Considerations	**Methods employed**
Optical Confinement	Sidewalls (width)
Brightness Optimisation	Active Material (length)
Light Outcoupling Optimisation	(a) Aperture (width) (b) Micro-mirror (feature) *(c) Micro-lens (feature)*

Table 1-1: Methods to be employed for optimisation of mmLETFEL's efficiency

These fabricated mmLETFEL test devices will be characterised by measuring their luminance against driving voltages. By comparing the luminance obtained, deductions can be made for the optimum device feature and dimension in the manufacture of a high-intensity mmLETFEL device.

Upon realisation of an efficient mmLETFEL device, a further enhancement would be the development of an integrated mmLETFEL linear-array device targeted at electrophotographic printing application. Thus, not only are the intensity and efficiency of the devices increased; but the need for external drivers, and hence the high density of external wire-bonds, as well as the overall manufacturing and assembly costs, minimised. In addition, commercially available Si fabrication technology is also mature enough to be integrated effectively.

As such, by depositing an electrode material as the base electrode, for example metals, a contact between the mmLETFEL device and the open drain of a commercially available driver can be established. **Figure 1-9** illustrates in greater detail the structure of an ideally desired mmLETFEL device (where the microlens structure has also been included), whereas the device dimensions and descriptions are being featured in **Table 1-2** that follows. Here, the top and bottom electrode bond-pads are shown, indicating the contacts that can be made.

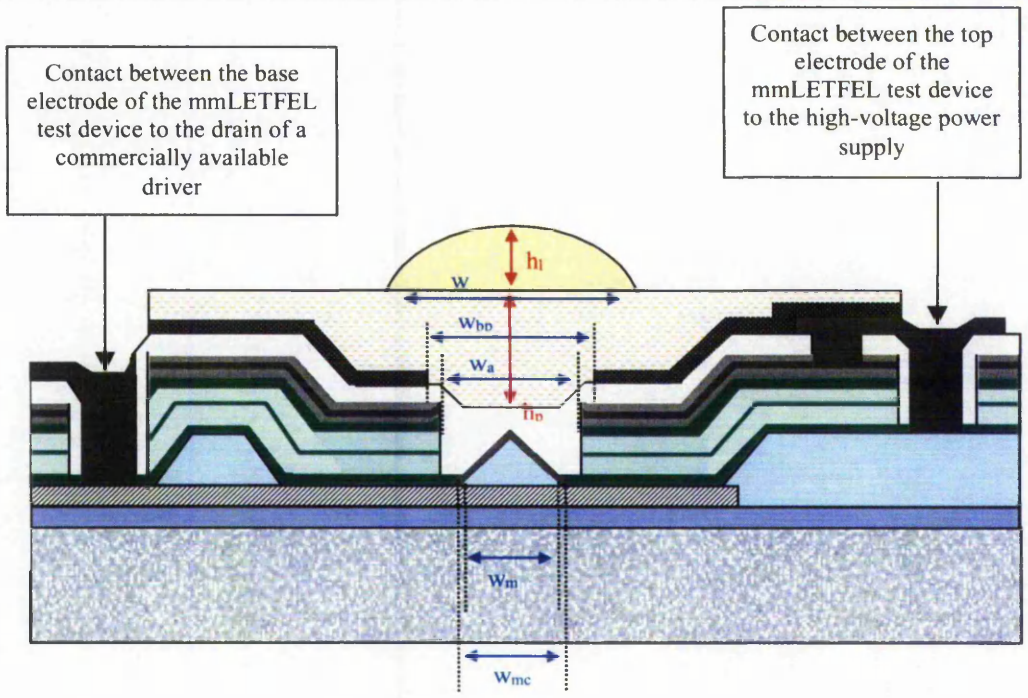


Figure 1-9: Cross-sectional view of a typical mmLETFEL test device structure, with indications to the top and bottom electrode contacts.

	Description
H_l	Height of micro-lens
H_{pl}	Height of planarisation
W_l	Base diameter of micro-lens
W_{bp}	Width of black polyamide
W_a	Width of emitting aperture
W_{mm}	Width of micro-mirror
W_{mc}	Width of micro-mirror coating

Layer	Description
	N-type Silicon
	Insulating Layer Material (Thermal Oxide, TOX)
	Base Electrode Layer Material (PolySilicon or Titanium/Tungsten)
	Micro-Mirror Layer Material (PECVD Silicon Dioxide, SiO_2)
	Metallisation Layer Material (Titanium/Tungsten, TIW)
	mmLETFEL Insulator Layer Material (Yytrium Oxide, Y_2O_3)
	mmLETFEL Phosphor Layer Material (Zinc Sulphide doped Manganese, ZnS:Mn)
	Metallisation Layer Material (Aluminium, Al)
	Passivation Layer Material (Silicon Nitride, Si_3N_4)
	Contrast Layer Material (Black Polyamide)
	Acrylic Planarisation Layer Material
	Acrylic Microlens Layer Material

Table 1-2: Description of the layers and denotations of the mmLETFEL device structure

The investigation into the feasibility of an integrated mmLETFEL device, i.e. the OEIC – a mmLETFEL pixel and a selected commercially available and suitable driver defined within the same device – will influence the eventual development of an integrated mmLETFEL linear printhead that can be utilised as an alternative high-intensity image bar array for electrophotographic printing applications. To illustrate the overall view of the final aim of this investigation, **Figure 1-10** exemplifies the general optical configuration of the integrated mmLETFEL printhead array for electrophotographic printing. When light generated within the active layer and guided laterally, reaches the micro-mirror for reflection off the emitting facet, it outcouples towards the SELFOC GRIN lens which is mounted at the object focal distance. The light projected onto the drum is then focused to expose an area where it is to be toned.

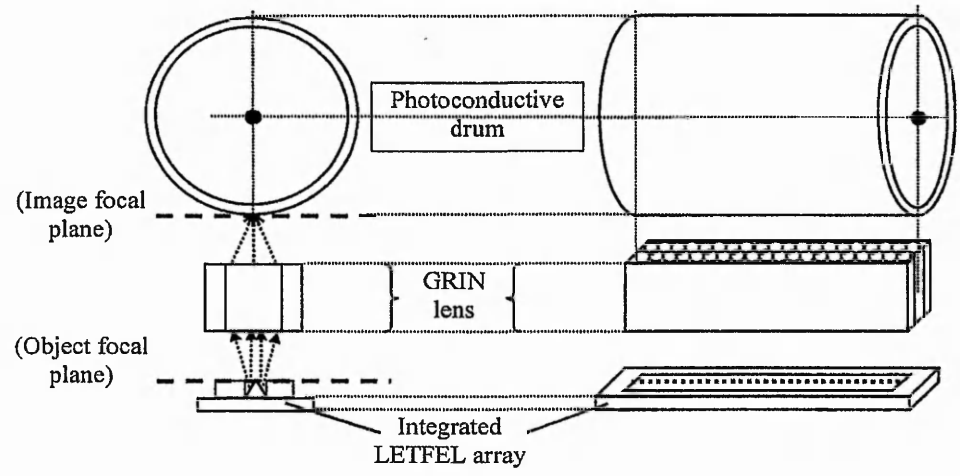


Figure 1-10: Simplified cross-sectional views of a general optical configuration utilising mmLETFEL devices

As such, the main investigation will involve:

1. Fabrication of the mmLETFEL test devices (both with and without metal or silicide materials deposited as the base electrodes)
2. Characterisation of the fabricated mmLETFEL test devices (with and without the presence of base electrodes)
3. Circuit Modelling of the mmLETFEL equivalent circuit (comparing the measured and simulated electrical quantities)
4. Characterisation of commercial drivers
5. Circuit Modelling of commercial drivers (comparing the measured and simulated electrical quantities)
6. Theoretical simulation of the OEIC – mmLETFEL device in series with a driver

However, prior to undertaking the main investigation, as a further affirmation to the possibility of developing an integrated mmLETFEL device, an initial investigation is carried out to ensure that the mmLETFEL devices fabricated would be bright enough for utilisation as an alternative light source in electrophotographic printing. The following section details a brief experiment conducted to test the ability of mmLETFEL devices in discharging a commercial photoconductive drum. In addition, the selection of a suitable material to be investigated as the base electrode in mmLETFEL devices is also included.

1.4.2 Preliminary Investigations

1.4.2.1 Photoreceptor Measurements

In order to ascertain that the mmLETFEL devices being fabricated have sufficient brightness to expose a commercial photoconductive drum of a printer, a test was conducted to measure the discharge voltage of the drum against time. This was carried out at Imperial College, Solid State Laboratory, in London.[71]

Due to the arrangement of the measurement system, shown in **Figure 1-11**, requiring light sources with an emitting aperture of no less than 8mm in length, a LETFEL device with an edge-emitting aperture at one end of the waveguide was used instead of the mmLETFEL device. Referring to **Figure 1-6**, by substituting Al as the top electrode, and without the presence of micro-mirrors, only direct lateral emission will be observed; and this was the light that was utilised and measured in this particular experiment. The LETFEL edge-emitter (eeLETFEL) was mounted together with a section of one SELFOC GRIN lens array SLA-20 (with acceptance angle of 6° and a focal distance of 4±0.1mm)[26] on a plastic support.

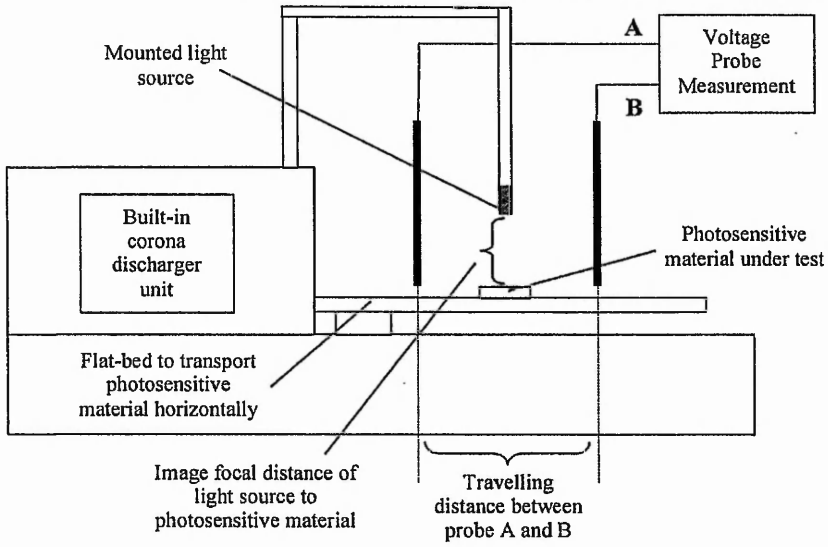


Figure 1-11: Simple block diagram of the measurement system used for the photoconductive drum discharge experiment

The eeLETFEL light source piece was then mounted at a distance to the drum corresponding to the image focal length of the GRIN lens. It was driven by a 10kHz square waveform with peak voltages of ±250V.

The commercial drum used here was the Fuji 9B-003, an organic photoreceptor. The measurement facility required the photoreceptor under test to be installed on a flat-bed which would travel horizontally across the unit. For this purpose, the drum had to be cut into several flat pieces. The photoreceptor was charged up as it passed through the corona discharger unit, and the initial charged voltage was measured by the first probe, A. As it travelled along the flat-bed, the eeLETFEL light source then exposed the drum, discharging the corresponding area. The voltage that was left after the discharge, was then measured by the second probe, B. The experiment was carried out 4 times, each with the photoreceptor set to travel at a different speed. The travel time from probe A to B, the initial voltage after charging, and the residual voltage after discharging, were measured and recorded.

From these measurements, the travelling speed of the photoreceptor can be calculated, and subsequently this can be converted to the actual speed of the drum as if in operation in a typical printer. At the same time, from the initial and residual voltages measured, the sensitivity of the printer drum can be calculated correspondingly to the calculated drum speed.

By appreciating that the length of an A4 page is 29.6cm, and the fact that the loading time for a printer is typically 30%,[72] then

$$1page = 1.3 \times 29.6cm = 38.48cm \qquad \textbf{Equation 1-1}$$

The travelling speed of the photoreceptor is the distance covered from probe A to probe B, divided by the time taken, t_S, to cover that distance, where the distance was measured at 6cm. Hence, the travelling speed, S, in terms of pages per minute,

$$S = \frac{6}{t_S} \times \frac{60}{38.48} \qquad \textbf{Equation 1-2}$$

Sensitometry[73] describes photoreceptor measurements that can be made with continuous exposure, or in this case, the flash exposure using the eeLETFEL light source. Therefore, the relationship between the surface potential and exposure can be determined, and the results are usually described by the sensitivity or the gain. Sensitivity is simply defined as the energy required to discharge the photoreceptor from an initial potential, V_0, to a residual voltage, i.e. the discharged voltage, V_d. This can alternatively be defined in percentage of discharge to the initial potential, i.e. the gain, G. Hence,

$$G = \frac{V_d}{V_0} \times 100\% \qquad \textbf{Equation 1-3}$$

The following **Table 1-3** tabulates the calculated results explained above.

Tests	Travelling time to cover 6cm t_S (sec)	Drum Speed S (p.p.m.)	Initial Potential V_0 (V)	Discharged Voltage V_d (V)	Sensitivity/ Gain G (%)
1	0.36	25	650	180	27.7
2	0.582	16	750	250	33.3
3	0.69	13	650	350	53.8
4	0.99	9	680	470	69.1

Table 1-3: The travelling time, corresponding drum speed and drum sensitivity are tabulated for the Fuji 9B-003

From the above results, it is evident that for a given light source of a known brightness, the sensitivity of the drum decreases with increasing drum speed. This indicates that in order to facilitate higher print speeds in printers, the brightness or overall luminance of the utilised light source must be high enough for the discharge to occur and thus the latent image can then be produced.

At a 50% gain (typical for sensitometry measurements of a photoreceptor),[35] the eeLETFEL light source with a recorded saturated brightness of 170kfL,[74] can be used for print speeds up to 13 p.p.m. Therefore, in a mmLETFEL device, the outcoupling of the lateral emission that is to be reflected off the pre-fabricated micro-mirrors must achieve a reasonable efficiency in order to obtain such print speeds.

1.4.2.2 *Electrode Materials Properties*

In order to establish a contact between the mmLETFEL device with its corresponding driver, base electrodes are to be pre-fabricated prior to the deposition of the thin-film EL structure. The material used must have a high melting point allowing thermal annealing after the fabrication process, a step that is necessary for device activation. As such, Al with a melting point of 660°C,[75] which is close to the annealing temperature used for mmLETFEL processing, cannot be considered for use as the base electrode, since it can diffuse into the dielectric, causing easy break-down of devices when driven.

Previous discussions with National Microelectronics Research Centre (NMRC) in Cork, Ireland, recommended that the metal available for fabrication of base electrodes prior to the deposition of mmLETFEL devices would be the alloy, Titanium/Tungsten (Ti/W). It is an already optimised process at NMRC, and would act as a starting point of the investigation into the feasibility of pre-fabricating base electrodes of mmLETFEL devices. For comparison purposes, the PolySi material, a deposition process that is also well-defined at NMRC, is also chosen for fabrication as the base electrodes of mmLETFEL devices. This is because standard MOSFET technology such as switching devices, utilise polysilicon as contacts.[76]

The process conditions of the Ti/W and PolySi materials will be detailed in Chapter 2, together with the recorded resistivity values measured at NMRC, while the characteristics of such successfully fabricated mmLETFEL test devices will be discussed in Chapter 3. Reviews from various sources,[77, 78] briefly summarises the separate properties of the two metals, titanium, and tungsten, as shown in **Table 1-4.** The high melting points of these metals indicate their suitability in sustaining the thermal annealing step that is necessary in mmLETFEL technology for device activation.

Metal	Resistivity (μΩ-cm)	Melting Point (° C)	Linear Thermal Expansion Coefficient (ppm/°C)
Ti	80	1690 ± 100	8.5
W	5.5	3380 ± 0.0	4.3

Table 1-4: Properties of metals, titanium (Ti) and Tungsten (W)

1.4.3 Summary of the Thesis

The main objective of the research is to assess and demonstrate the feasibility and commercial viability of developing an integrated electrophotographic light source utilising mmLETFEL technology and standard Silicon fabrication processes. This will be achieved by the fabrication and characterisation of mmLETFEL test devices with selected materials for the base electrode, characterisation of commercially available drivers, and circuit simulation of the proposed integrated mmLETFEL device. The general outline of the investigation is broken down into the following chapters:

Chapter 2

Fabrication of mmLETFEL Test Devices

Growth and deposition of the mmLETFEL test devices, with the inclusion of two base electrode materials being assessed, are detailed. Fabrication details of two different insulator materials for comparison purposes are also provided. The full processing sequence of the mmLETFEL technology is explained and discussed.

Chapter 3

Characterisation of mmLETFEL Test Devices

Electrical and optical measurements of fabricated mmLETFEL test devices – process details as provided in Chapter 2 – are explained. mmLETFEL test wafers grown with two base electrode materials and two insulator materials are characterised, and the corresponding results of these four different device configurations are detailed.

Chapter 4

Characterisation and SPICE Modelling of High-Voltage MOSFETs

The selection of a suitable MOSFET driver technology from various commercially available drivers is explained. Electrical characterisation and SPICE modelling on the test die of the selected technology obtained are performed. The measured and simulated data are then compared and analysed.

Chapter 5

SPICE Modelling of mmLETFEL Test Devices and the Integrated mmLETFEL Device

Development of the equivalent circuit for the mmLETFEL test device and SPICE simulation of the developed circuit, performed utilising theoretical values calculated, are explained. Measured data of mmLETFEL test devices obtained in Chapter 3 is used for subsequent simulation in optimising the model. Further, theoretical simulation on the proposed OEIC device configuration is also carried out, using this developed mmLETFEL SPICE model, and the SPICE model parameters obtained for the selected MOSFET technology from Chapter 4.

Chapter 6

Final Conclusions

A summary and conclusion of the work done, latest developments to the mmLETFEL device structure, and a proposal of the OEIC processing sequence as further work to the current programme, are detailed in this chapter.

Contents

2 Fabrication of mmLETFEL Test Devices

2 FABRICATION OF mmLETFEL TEST DEVICES

2.1 INTRODUCTION

To facilitate the simulation exercises which will be detailed in Chapter 5, fabrication of mmLETFEL test devices with suitable base electrode materials have to be investigated. Upon successful fabrication of these test devices, they are then characterised both electrically and optically. Analysis of these characteristics provide the optimum mmLETFEL structure compatible for integration with commercially available silicon MOSFET technologies.

In this chapter the sequence of a fully-fabricated mmLETFEL test device processing route is detailed. This encompasses all aspects of the fabrication process in each stage, i.e. deposition, masking and etching processes, including the process conditions applied. Prior to this, a general background review from information specific to the standard fabrication processes and operating mechanisms of the available deposition and etching techniques are detailed (Section 2.2 and Section 2.3). Section 2.4 details the specific process conditions of the mmLETFEL device fabrication, and towards the end of the chapter, a summary of the full fabrication route of the mmLETFEL test devices is given.

2.2 DEPOSITION TECHNIQUES

There are many and various kinds of deposition processes available for production of both thick films (>25μm) and thin films. However, a brief review of only the more popular and mature thin-film deposition techniques is given. Generally, these processes can be divided into three main categories: physical methods, chemical methods, and hybrid (physical-chemical) methods.

Examples of physical methods of deposition include:

1. Thermal Evaporation processes
2. Molecular Beam Epitaxy (MBE) which is a specialised form of evaporation
3. Sputtering techniques
4. Cathodic Arc Deposition (CAD) which combines both evaporation and sputtering techniques

Examples of chemical methods of deposition include:

1. Thermally induced Chemical Vapor Deposition (CVD)
2. Metal Organic CVD (MOCVD) which is a popular production technique for single-crystal-based quantum devices
3. Optically activated CVD involving direct writing of patterned thin films accomplished by focussed laser-assisted CVD
4. Deposition of sol-gel films prepared by controlled solution dipping processes followed by heat treatment.

The third category of deposition processes involves a technique that combines both the physical and chemical aspects. This includes:

1. Plasma-Enhanced CVD (PECVD) which involves CVD in a glow discharge
2. Formation of inorganic films by Remote PECVD in which the substrates are removed from the main part of the plasma
3. Selective deposition of thin-film patterns from precursor gases and vapors used in CVD by activating local areas of the substrate with various kinds of beams such as electron, ion, and laser.

In this instance however, only the types of deposition techniques or processes utilised in the fabrication of mmLETFEL test devices for this particular research and investigation will be discussed in further detail in the following sub-sections, i.e. d.c. and r.f. magnetron sputtering,[79]-[81] low-pressure CVD and plasma-enhanced CVD.[82]-[86]

2.2.1 Sputtering

The sputtering technique is one of the most commonly used methods for the deposition of thin films due to the simplicity and versatility of the physical processes involved. The flexibility for alteration and customisation are also its strong points. Sputtering techniques range from a simple d.c. glow discharge sputtering (limited to sputtering of conductive targets), to r.f. sputtering (where any target can be sputtered, regardless of its conductivity), to ion beam sputtering (where controlled deposition of material is possible). Other advantages are its high deposition rate and the fact that this sputtering process allows tailoring of the structure of the film by utilising available ions.

A disadvantage of sputtering is the low target material utilisation in certain configurations. For example, the region where the plasma is concentrated by the magnetic and electric field interaction in magnetron sputtering is a limited area of the total surface area of the target. Therefore, the target gets sputtered-through at the 'race-track' region while the rest of the target surface is barely eroded. However, there are ways to achieve a higher target utilisation: by rotating the target and/or magnets in order to have a more uniformly sputtered target; or, by flattening the magnetic field lines parallel to the target surface.

2.2.1.1 D.C. Sputtering

One of the simplest of sputtering techniques is d.c. sputtering, with the limitation that non-conductive targets cannot be sputtered. The target plate is made up of the material to be deposited and is connected to a d.c. power supply. The substrates face the target, and depending on the type of film, the substrates can be cooled or heated to the desired temperature. The system is then pumped down to the base pressure, and backfilled with the sputtering gas, Argon (Ar). A negative d.c. voltage is applied to the target to start the plasma. The target surface is bombarded with positive ions in the plasma, while the neutral atoms are ejected and condensed onto the substrate to form a film. In order to obtain an optimum sputtering condition for d.c. sputtering, there are a few variables to consider: electrode separation (typically a few centimetres), pressure (typically 20-100mTorr), applied voltage (typically 500-5000V) and composition of gas for reactive sputtering.[79]

The discharge voltage must be high enough to accelerate the ions so that upon impact on the target, secondary electrons are produced and with each secondary electron producing sufficient ions to produce one more electron from the target surface. The sputtering pressure can be increased to increase the sputtering rate at a given voltage, but not too high such that the ions are slowed down due to the inelastic collisions with the gas atoms and the gas scattering of the sputtered atoms occur. Electrode separation has to achieve an optimum region for the secondary electrons to undergo ionising collisions before reaching the anode, but not too large an area such that the collisions cause the generated ions to lose their energy upon reaching the cathode to produce more secondary electrons.

2.2.1.2 R.F. Sputtering

In the case of r-f sputtering, increasing the applied a.c. signal's frequency up to 50kHz does not make a substantial difference and the discharge is similar to the d.c. discharge, except for the fact that both the target and the substrates are sputtered due to the polarity reversal in each cycle. For frequencies above 50kHz however,[80] the electron oscillations can cause enough ionisation of the gas to sustain a discharge without necessitating secondary electron emissions. The r-f voltage can also be coupled through any kind of impedance, thus enabling an insulator to be sputtered in an r-f discharge.

At a typical r-f frequency of 13.56MHz,[80] ions are relatively immobile. Upon application of this r-f signal, electrons are drawn to the target in one half of the r-f cycle. For an insulator target, or a conductive target capacitively coupled to the r-f power supply, the second half of the cycle could not cause a similar amount of current to flow due to the mobility differences in the charge carriers, thus forming a net negative self-bias potential on the target.

Typically, r-f discharges can be maintained at 1-15mTorr,[80] considerably lower than pressures required for d.c. sputtering. This is because at high frequencies, oscillating electrons increase collisions, thus enhancing ionisation. Another reason is that because both electrodes are at negative potential to the plasma, secondary electrons are reflected back and forth, utilising their energy for ionisation, thus not many are lost prior to the ionisation process.

2.2.1.3 Magnetron Sputtering

In a conventional glow discharge, the electron loss occurs when they are recombined at the walls. The use of a magnetic field in a sputtering system results in the electrons producing more ionisation and reducing this loss. In a magnetron system, the magnetic field (typically 50-500 gauss) which is parallel to the target surface, enhances ionisation by reducing the velocity of the electrons towards the wall to zero, and hence reduces electron recombination losses.[81] The longer helical orbit formed increases the total path travelled by the electron thus causing more ionisation and excitation. By simultaneously applying an electric field perpendicular to this magnetic field however, the secondary electrons are caused to drift in a closed circuit or tunnel in front of the target surface. The electrons are trapped near the target from where they are emitted, and this confinement significantly increases the efficiency, and thus increases the ionising effect. As a result, a magnetron system can operate at low pressure (typically 1-3mTorr) and low voltage (typically 350V).[81]

However, as mentioned earlier, one of the disadvantages is poor utilisation of the target material (typically 20-30%).[81] This can be overcome by providing relative motion of the target with respect to the magnets. Magnetron sputter sources work well with both d.c. and r.f. power. The most common type of r.f. magnetron configuration uses the chamber and other grounded fixtures for the second r.f. electrode. Implementation of r.f. magnetron sputtering can be as easy as d.c. magnetron sputtering providing that there is ground shielding (which is conformal and as close as possible to the target), good ground return, and minimum length of cable from the matching box to the source.

Figure 2-1 shows the general features of a typical sputtering system and **Figure 2-2** the cross-sectional view of a typical magnetron sputter source.

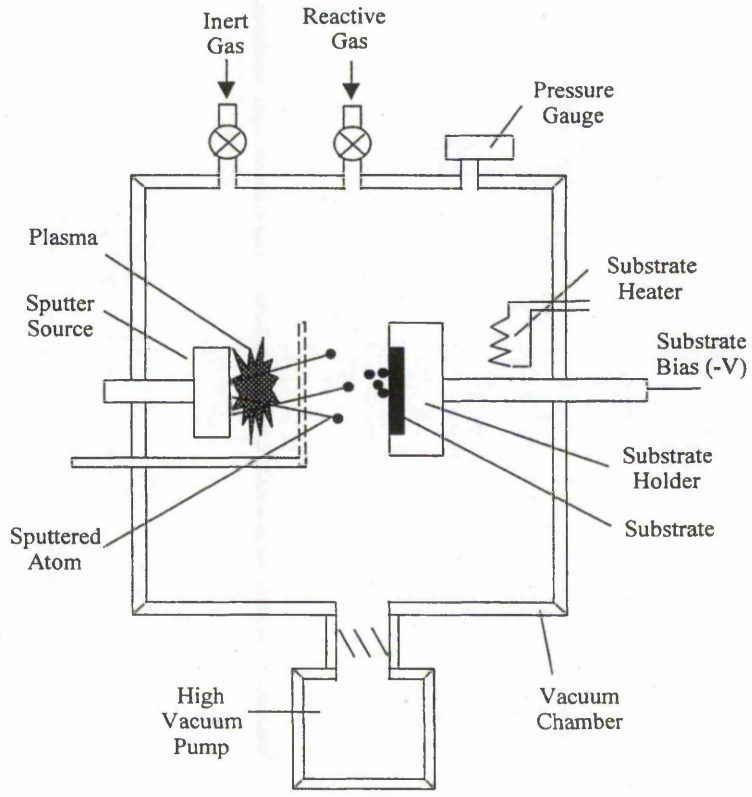


Figure 2-1: General features of a typical sputtering system

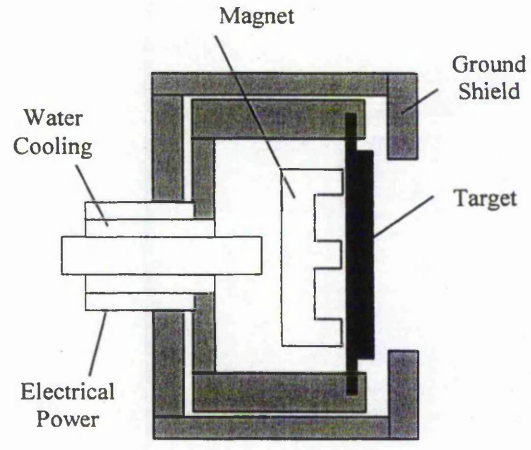


Figure 2-2: Cross-sectional view of a typical planar magnetron sputter source

2.2.2 Chemical Vapor Deposition (CVD)

CVD has also become a major method of film deposition in the fabrication of advanced semiconductor devices. CVD techniques are vapour deposition techniques based on homogenous and/or heterogeneous chemical reactions, and employ various gaseous, liquid and solid chemicals as sources of elements of which the film is to be made. In practice, these processes are used to deposit a large variety of single-crystalline, polycrystalline and amorphous thin films of IV, IV-IV, III-V, II-VI, metals, dielectrics and superconductors.[82]

Compared to other deposition techniques, the CVD method is the most complex as it requires numerous test runs to achieve suitable growth parameters.[83] Therefore, to be useful, the deposition rate for a CVD process must be reasonable and the deposited films should have reproducible and controllable properties such as purity, composition, thickness, adhesion, microstructure, and surface morphology. As device size decreases, and the complexity and level of integration increases, however, these introduce stringent limitations to the process. Another critical element is the thickness uniformity of a film in order to maintain the same characteristics across each substrate and from wafer to wafer. Also, CVD reactants must be pure and no by-products produced that can incorporate into the growing film, or react with other gas and reactor materials.

This method is particularly useful in the deposition of coatings in sites that are difficult to reach by other deposition techniques, and is capable of producing uniform, pure, reproducible and adherent films at low or high rates. Its disadvantage would be the chemical hazards caused by toxic, explosive, inflammable or corrosive gases.[83]

2.2.2.1 Low Pressure Chemical Vapor Deposition (LPCVD)

Compared to the Atmospheric-Pressure CVD (APCVD) that operate at high temperatures, LPCVD has many advantages. These include better step coverage, lower particle densities, and better film uniformity. As they operate under reduced pressure, they are all batch processors and are surface-reaction-rate controlled. Typically, the low pressures operated here are in the range of 0.2-2mTorr.[84]

2.2.2.2 *Plasma-Enhanced Chemical Vapor Deposition (PECVD)*

PECVD has become an increasingly important and established commercial technique for the deposition of important materials in integrated circuit fabrication. Among the major advantages include its lower temperature capability (roughly 250°C to 300°C is sufficient to deposit silicon nitride films which would normally need about 700°C to 900°C by thermal CVD), reasonable growth rates, and high quality.[85]

This lower temperature capability is possible because the thermal energy is being effectively substituted by electrical energy. This electrical energy is coupled into the gas by a plasma to promote chemical reactions, and this source of energy enhances the reaction rate, thus making it less sensitive to temperature. The most important PECVD dielectric and insulator films used primarily in microelectronic device fabrication include silicon nitride, silicon oxide, silicon oxynitride, and silicate glasses.[86] **Figure 2-3** illustrates a schematic diagram of a typical PECVD reactor being used commercially.

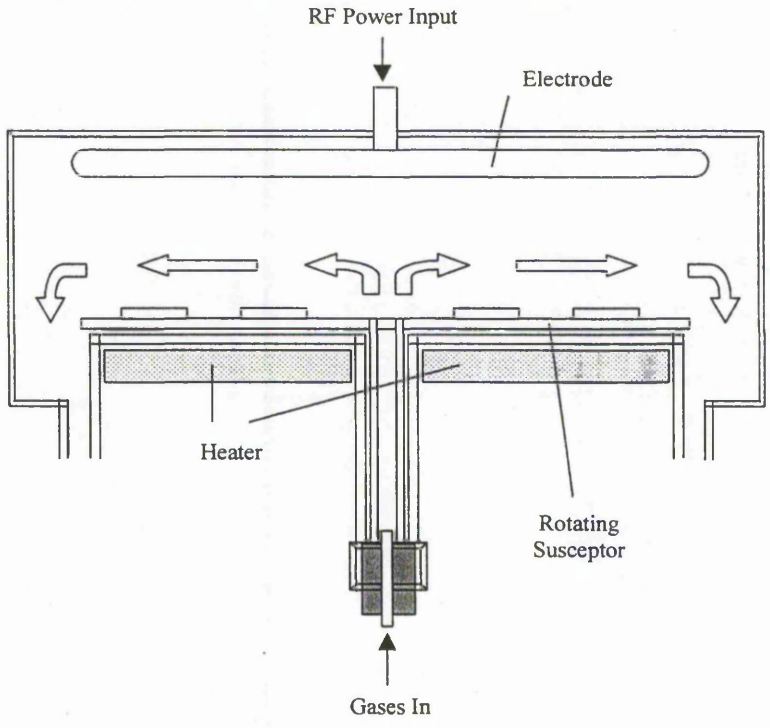


Figure 2-3: Major components/elements of a typical PECVD reactor with conventional parallel-plate electrode

2.3 ETCHING TECHNIQUES

More than three decades ago, virtually all semiconductor devices were etched in manually controlled wet-etchant baths, which involves immersion of wafers in aqueous-based etching solutions. Two of the basic major obstacles faced by this type of wet etching technology are isotropy, and displacement of manually controlled and operator-dependent processing techniques. [87]

Isotropy causes the amount of the lateral etch to approximate the depth in etch, thus resulting in an arc that sweeps from under the resist image to the silicon or substrate interface where the etched layer ends. This increases the cost of I.C. manufacturing. To overcome some of the isotropy problems, spray etching has emerged by directing the etch at the wafer and dissolving through the layer at a greater rate than the lateral etch rate. This gives greater uniformity and reduces undercutting, thus better etch quality.

However, due to the ever-shrinking device geometry that became a realistic production possibility as the integrated circuit technology matured, this highly operator-dependent batch-immersion process has since given way to a highly automated process. Dry etching technology which provides higher resolution and use of lower postbake temperature, is more compatible with positive photoresists and has better control of overetch. There are three distinct dry etching techniques:

1. Plasma Etching which is only cost-effective if needed for very fine-line definition ($<3\mu m$).[89]-[91]
2. Reactive Ion Etching (RIE) which is performed in low-gaseous plasma, involving both physical and chemical sputtering.[92]
3. Ion Beam Milling which utilises physical sputtering and has many similar elements to plasma etching except that the substrates are not immersed in a glow discharge, and is performed in vacuum.[93]-[94]

Other methods include sputtering which is performed in relatively low vacuum and generally used for surface cleanup, and high-temperature vapor etching generally used as an in situ cleanup before epitaxial depositions.[88] Here, plasma etching, RIE and ion beam milling will be reviewed in slightly greater detail as they are the main etching processes utilised in the fabrication of mmLETFEL test devices for this research.

2.3.1 Plasma Etching

One of the many advantages of plasma etching is its finer line-width resolution, as well as its adaptability to increased throughput and automation, and therefore this technique is commonly used in fine-geometry applications. While it also helps solve some of the problems associated with wet etching such as wetting, disposal, safety, and isotropy, however etch uniformity is still an issue and cannot be achieved without single-wafer etching.[89, 90, 91]

A few critical aspects of using the plasma etching technique would be the appropriate use of photoresist that is more resistant to plasma gases; improved thermal stability in resist systems and detection of the end point of the etch cycle where the etch does not have good selectivity. **Figure 2-4** shows the major components of a typical plasma etching system.

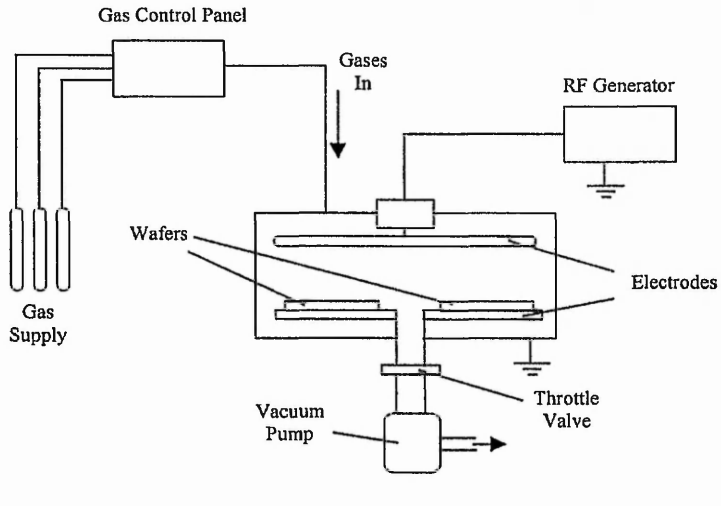


Figure 2-4: Major components/elements of a typical plasma etching system with parallel-plate electrodes

2.3.2 Reactive Ion Etching

RIE combines both chemical reactions and physical sputtering as part of the etching mechanism. It is an anisotropic dry technique which is performed in a planar plasma reactor and which replicates the photoresist pattern onto the coated film with high precision in the vertical direction. The reactivity of the ions that are formed is very high especially when chemical sputtering occurs. These ions are accelerated and directed to the substrate where atoms are displaced through two processes:

1. physical displacement
2. chemical reactions forming volatile by-products

RIE can also introduce high selectivity values which permit a certain amount of over-etch to be applied without damaging the pattern design. It is also dependent on chemical reactions at less than 0.1Torr pressures, thus use of lower-energy beams is possible because the potential energy is tied up in the ions themselves.[92] This results in lower processing temperature. A sketch of a typical RIE system is depicted in **Figure 2-5**.

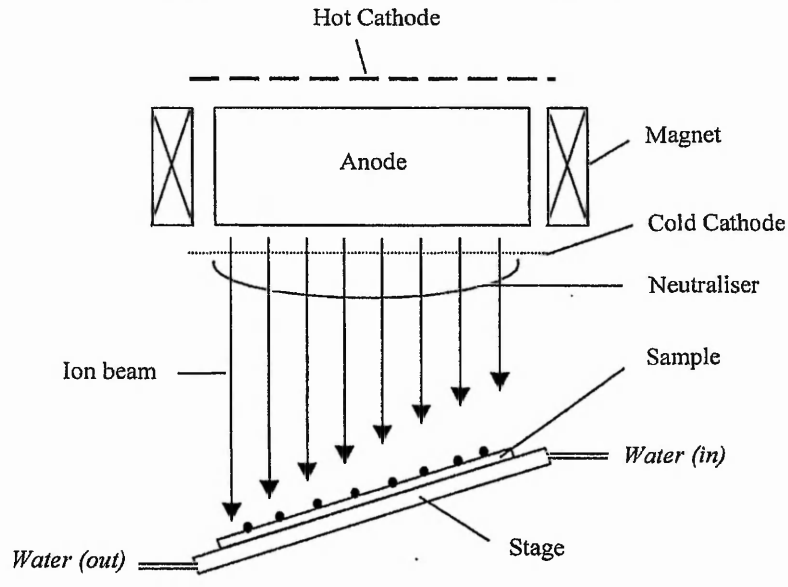


Figure 2-5: Major components/elements of a typical RIE system

2.3.3 Ion Beam Milling

The principal mechanism of ion-beam etching, or ion-beam sputtering, is one of directing high-energy ions towards a solid, therefore the prospect of anisotropic etching is good provided that control of its effect on the incident target is maintained. Since the particle sizes are in the ion and atom category, the resolution and aspect ratio (etch width to etch depth) potential is high. However, one of its major limitations is the high temperature generated during the ion-bombardment process, causing the resist to flow and making their removal extremely difficult.[93, 94]

This physical sputtering technique is one of an impact and energy transfer sputter etch process. The collimated beam of high-energy ions collide with the surface ions of a solid and the energy is transferred from the incident ion to the surface atoms of the solid. The surface atoms are displaced by the incident ion if the energy force binding the atoms of the solid is less than the energy force of the incoming ion. This energy required to dislodge an atom of a solid is referred to the threshold energy and is typically of 5eV to 40eV.[93] The range of threshold energies is dependent on the mass incident ion and the crystal orientation of the solid. **Figure 2-6** illustrates a typical ion-milling system.

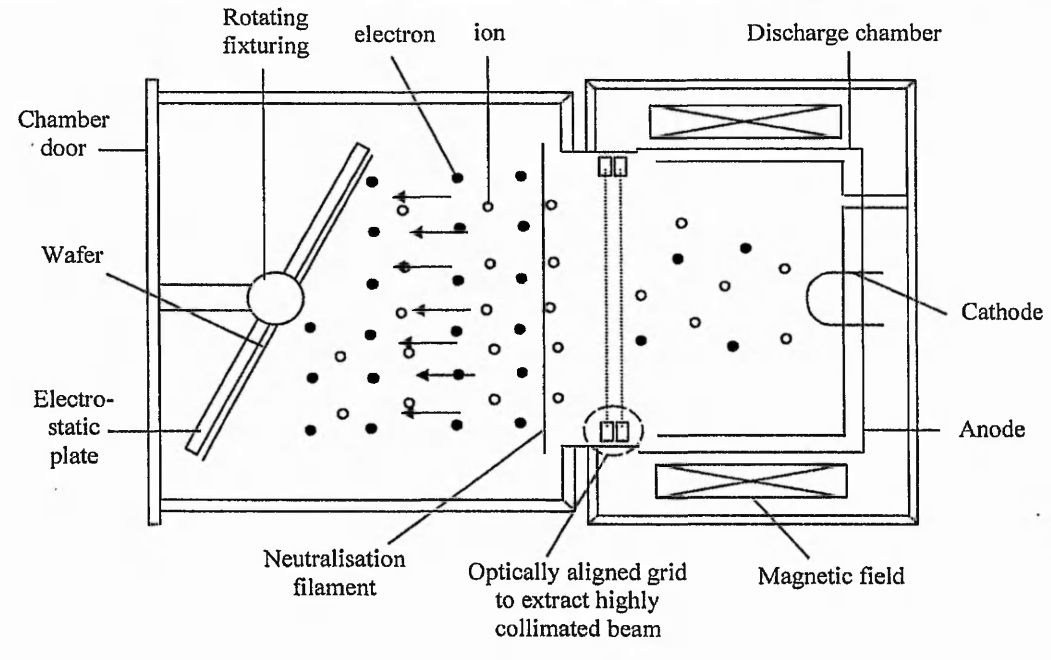


Figure 2-6: Major components/elements of a typical ion-milling system

2.4 PROCESS CONDITIONS FOR mmLETFEL FABRICATION

To summarise from previous sections, the deposition techniques used for the fabrication of the mmLETFEL test devices for this particular investigation are:

1. r.f. magnetron sputtering for the deposition of the TFEL stack, i.e. the insulator material, Y_2O_3, and phosphor material, ZnS:Mn.
2. d.c. magnetron sputtering for the deposition of the electrode materials, i.e. Al and TiW.
3. low-pressure CVD for the deposition of PolySi.
4. plasma-enhanced CVD for the deposition of the micro-mirror material, i.e. SiO_2, as well as for the deposition of an alternative insulator material, i.e. Si_3N_4.
5. plasma etching for the etching processes performed at NMRC, RIE for the etching of metallisation layers, and ion-beam milling for the etching of the mmLETFEL aperture.

The processing sequence of the mmLETFEL test devices can mainly be divided into four main categories:

1. Fabrication of the base electrodes [95]
2. Fabrication of the micro-mirror structures [95]
3. Fabrication of the TFEL devices [96]
4. Fabrication of the top electrodes [97]

The fabrication of the base electrodes and micro-mirrors took place at National Microstructures Research Centre (NMRC) in Cork, Ireland. Deposition of the electroluminescent thin-film structures was performed at The Nottingham Trent University (TNTU) in Nottingham. The fabrication of the top electrodes and the shaping of the emitting aperture were conducted at Qudos Ltd. and the Central Microstructure Facilities (CMF), both in the Rutherford & Appleton Laboratories (RAL), Oxford, but with the photolithography steps being performed at TNTU.

The following first four sub-subsections detail the process conditions utilised in both the deposition and etching processes, as well as the photolithography steps, for the full fabrication of the mmLETFEL test devices. The photolithography steps performed at TNTU for the top electrode etch and mmLETFEL aperture definition as well as a brief review of the mmLETFEL aperture profile definition via ion beam milling, are included in the subsequent two sub-sections.

Prior to this explanation of the mmLETFEL processing sequence however, the following table lists the mask set designed and used for the photolithography steps. It gives the corresponding information of the material layer that each mask name relates to, and also serves as a cross-reference to Section 2.5 where a summary of the mmLETFEL fabrication route is tabulated and illustrated graphically.

Mask Name	Layer Name
CP01	Thermal Oxide layer etch (T_{OX})
CP02	Base Electrode layer etch (TiW/PolySi)
CP03	Micro-Mirror structure etch (PECVD SiO_2)
CP04	*Waveguides structure etch (ZnSe)*
CP05	Metallised Micro-Mirror structure etch (TiW)
CP06	First Metallisation layer etch (top electrode definition - TiW/Al/TiW); and Aperture profile definition
CP07	Passivation layer etch
CP08	Y_2O_3 layer etch
CP09	Second Metallisation layer etch (bondpad region definition)
CP10	*Contrast layer etch (black polyamide)*
CP11	*Planarisation layer etch*
CP12	*Microlens definition*

Table 2-1: List of the names and their corresponding material layer of the mask set designed for photolithography of mmLETFEL fabrication (although CP04, CP10, CP11 and CP12 are listed, they are not used in the fabrication of mmLETFEL devices thus far in this investigation)

2.4.1 Fabrication of the Base Electrode

Since the base electrodes are being fabricated for electrical connections to individual LETFEL test devices, an underlying material insulating these base electrodes from the N+ Si wafers on which the LETFEL test devices are to be grown, has to be deposited first. This enables connection to the base electrode via the defined bondpads and insulates the TFEL material from the Si wafer. Three sections are described separately below relating to the fabrication of the insulating thermal oxide layer, and the two base electrode layers, i.e. TiW and PolySi.

2.4.1.1 Insulating layer: Thermal Oxide (T_{OX})

Deposition

A layer of oxide was deposited by thermal oxidation at 6l:3.7l of H_2:O_2 atmospheric pressure for 39 mins at 1100°C yielding an underlying insulator of thermal oxide with a thickness of 5,000Å. It was then subjected to a dehydration bake for 40 mins at 180°C.

Masking/Definition

A photoresist, OLiN HIPR 6512, was spun to a thickness of 1.2μm. The photomask CP01 was then aligned using Proximity Alignment. Upon UV exposure, the pattern was transferred, and then developed using HDRD 428 developer.

Etching

The thermal oxide layer was etched by plasma etching. An etch rate of 83Å/min was utilised; etching for approximately 1 hr, under 1000mTorr pressure and 250W of power. Gases used were CHF_3:O_2 at 88sccm:30sccm.

Resist Removal

The photoresist was stripped in 5l:100ml of Sulphuric:Peroxide acid at 150°C.

2.4.1.2 Base Electrode: PolySilicon (PolySi)

Deposition

A layer of PolySi was deposited using Low Pressure Chemical Vapor Deposition (LPCVD). A gas SiH_4 of 60sccm was used under a pressure of about 140mTorr at 620°C. A deposition rate of 90Å/min was determined and deposition took approximately 50 mins. It was then thermal diffused with $POCL_3$ and subjected to a dehydration bake for 40 mins at 180°C. This yielded a thickness of 4,500Å with recorded sheet resistance at 15.72 Ω/sq.

Masking/Definition

A photoresist, OLiN HIPR 6512, was spun to a thickness of 1.2μm. The mask CP02 was then aligned using Proximity Alignment. Upon UV exposure for 13.5sec, the pattern was transferred, and then developed using HDRD 428 developer.

Etching

The PolySi layer was etched by plasma etching. This process has three distinct steps, with applied r.f. power of 180W, 160W, and 100W for the three consecutive steps respectively. The gases Cl_2:He were kept at 50sccm:10sccm for all three steps, while 10sccm of CCl_3 was used only in the first process step.

Resist Removal

The photoresist was stripped in 5l:100ml of Sulphuric:Peroxide acid at 130°C.

2.4.1.3 Base Electrode: Titanium/Tungsten (TiW)

Surface Cleanup

Prior to the deposition of the base electrode materials, the target surface was cleaned using the r.f sputter etch technique. This was done in the sputtering chamber at 1kW for 25 mins.

Deposition

The TiW metal was deposited by d.c. magnetron sputtering. A given flow of Argon gas was injected at a temperature of 250°C, with an applied power of 1kW, and at a deposition rate of 133Å/min. This yielded a thickness of 3,000Å with recorded sheet resistance at 2.46Ω/sq.

Masking/Definition

A photoresist, OLiN HIPR 6512, was spun to a thickness of 1.2μm. The mask CP02 was then aligned using Proximity Alignment. Upon UV exposure for 13.5sec, the pattern was transferred, and then developed using HDRD 428 developer.

Etching

The TiW metal layer was etched by plasma etching. Gases used were Cl_2:BCl_3 at 2sccm:50sccm, under 1,000mTorr pressure and 115W of power.

Resist Removal

For the removal of the photoresist, a proprietary chemical is used instead, as sulpuric peroxide which was used in the etching of PolySi as mentioned before, would erode a metallised layer.

2.4.2 Fabrication of the Micro-Mirror Structure

Micro-mirror structures can be fabricated at an angle of anywhere between 45° to 65°. In this current investigation however, the micro-mirrors have been formed at 55°-65° angle, with the dimensions of 1.5μm height and 3μm base width. **Figure 2-7** shows an SEM picture of the angles of the micro-mirror structures successfully formed in NMRC, and on which the mmLETFEL test devices have been fabricated.

2.4.2.1 Micro-mirror Structure: Silicon Dioxide (SiO_2)

Deposition

The micro-mirror structure material was deposited by Plasma-Enhanced CVD (PECVD). Gases used were N_2O:Silane at 2000sccm:100sccm, under a process pressure of 750mTorr at 300°C and a power of 430W. This yielded a layer of Silicon Oxide (SiO_2) at a thickness of 15,000Å. It was then subjected to a dehydration bake for 40 mins at 180°C.

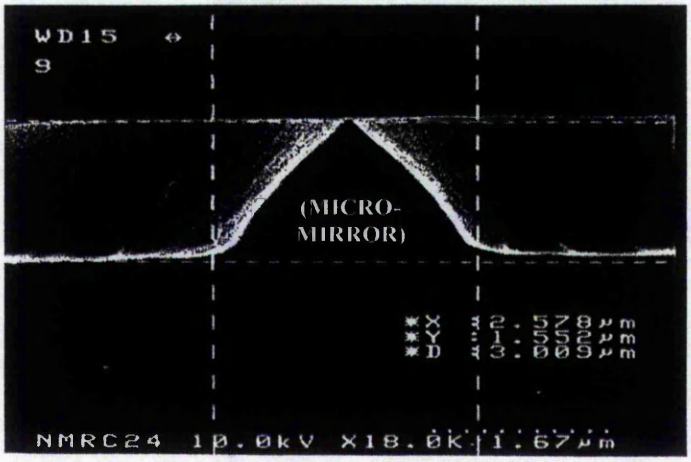


Figure 2-7: A cross-sectional view of the successful formation of a micro-mirror structure being fabricated at NMRC

Masking

A photoresist, OLiN ASPR 5503, was spun to a thickness of 3μm. The mask CP03 was then aligned using Proximity Alignment, UV exposed to transfer the desired pattern, and then developed using HDRD 428 developer.

Etching

The etching conditions for this is similar to the process utilised for etching of the insulating layer, T_{OX}. An etch rate of 83Å/min was utilised; etching for approximately 3 hr, under 1000mTorr pressure and 250W of power. Gases used were CHF_3:O_2 at 88sccm:30sccm.

Resist Removal

Depending on whether the underlying material of the micro-mirror structures was PolySi or TiW, the appropriate chemical was used for the removal of the photoresist.

2.4.3 Fabrication of TFEL Devices

Fabrication of the TFEL devices can be divided into two main sections, i.e. growth and deposition of the phosphor and insulator materials, ZnS:Mn and Y_2O_3, respectively. The deposition of these materials was by rf-magnetron sputtering, and the deposited mmLETFEL thin-film stack was subjected to a post-annealing process of 1 hr at 500°C under vacuum.

In this instance however, the LETFEL test devices under test and used for characterisation have been fabricated with a 'barrier-layer' phosphor. The deposition of a 'barrier-layer' phosphor includes a 100Å thickness of Y_2O_3 sandwiched in the middle of the 8000Å phosphor layer, ZnS:Mn. **Figure 2-8** shows the main chamber used for deposition of ZnS:Mn and Y_2O_3 thin-films in TNTU, Nottingham.

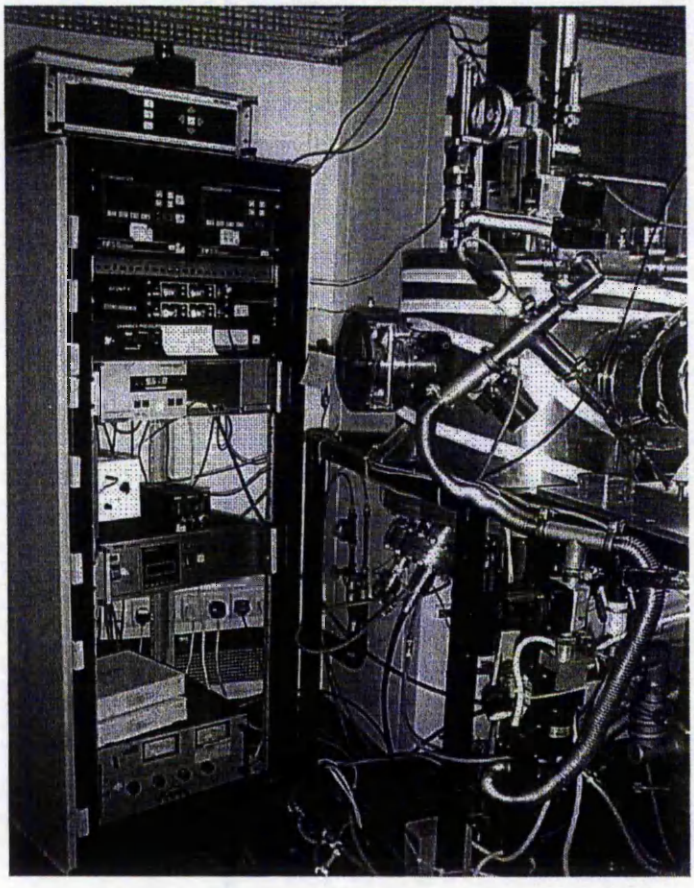


Figure 2-8: Sputtering system used for deposition of phosphor and insulator thin-films of mmLETFEL test devices at TNTU

Apart from the fabrication of Y_2O_3 as the insulator of the TFEL devices, fabrication of PECVD Si_3N_4 for use as an alternative insulator material has also been investigated for comparison purposes. As such, the following discusses the fabrication of all three materials in three separate sections.

2.4.3.1 Phosphor: Zinc Sulphide doped with Manganese (ZnS:Mn)

8000Å of r.f. magnetron sputtered ZnS:Mn thin films were deposited at a rate of 2600Å/hour, at a frequency of 13.56MHz, with the substrate temperature maintained at 200°C. A 0.43 %w of Mn in ZnS phosphor, was cold pressed into a 75 mm diameter powder target to be sputtered for 3 hrs at 100W. The growth parameters were set to $1x10^{-7}$ Torr base pressure, $3x10^{-3}$ Torr process pressure and 5sccm of Ar gas flow.

2.4.3.2 Insulator: Yttrium Oxide (Y_2O_3)

3000Å of r-f magnetron sputtered Y_2O_3 thin films were deposited at a rate of 857Å/hour with the substrate temperature maintained at 200°C. A 75 mm diameter x 4 mm thick solid yttrium oxide target from Cerac Ltd, was sputtered for 3.5 hrs at 120W. The Ar gas flow, base and process pressure, and deposition temperature were the same as that utilised for the ZnS:Mn deposition.

2.4.3.3 Insulator: Silicon Nitride (Si_3N_4)

This 3,000Å insulator material was deposited by PECVD using the Plasma Technology DP800 system at Central Microstructures Facility (CMF), RAL, Oxford. The chamber was pumped down to a base pressure of 10mTorr and the substrate maintained at a constant temperature of 300°C. Gases used were 120sccm:19sccm of NH_3:SiH_4 and the process pressure set at 320mTorr. An a.c. power of 13W was applied and a deposition rate of 67Å/min was achieved.

2.4.4 Fabrication of Top Electrodes

Previously, the top electrodes of LETFEL devices have been of Aluminium sputtered to a thickness of about 8,000Å. However, SEM observation showed undesirable Al "spikes" appear and penetrate into the bondpad region. Thermal expansion and reflow of the Al during heating, where high temperature is common, could have caused this phenomena. It follows that these "spikes" would also penetrate into the insulator material, thus reducing the current-limiting characteristics typical of a TFEL device. This affects the performance of the mmLETFEL device, and produces unreliable devices that would break down at much lower than expected voltages, since these "spikes" effectively behave as short-circuits at some points. **Figure 2-9** illustrates the observed Al "spikes".

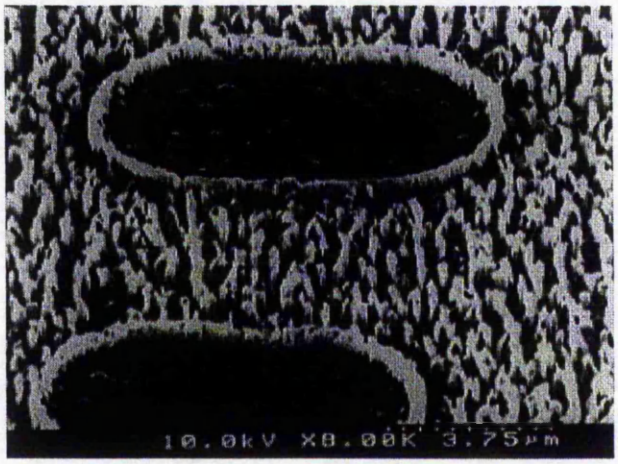


Figure 2-9: Illustrating the protruding "spikes" occurring at the Al layer

To overcome this problem, a refined electrode fabrication was developed, resulting in two levels of metallisation. Firstly, a tri-layer of TiW/Al/TiW, followed by a thickening of Al at the bondpad region. The TiW helps to eliminate the problem associated with the formation of the "spikes" as it shielded the reflow of Al from penetrating into either interface, i.e the insulator material or the bondpad region.

The thickening of the Al at the bondpad region however is needed to facilitate an easier wire-bonding process of devices to chip carriers. Furthermore, commonly used wire-bonding thread is of either Al or Au, and the wire-bonding procedure depends on the force and power generated by the 'ultrasonic' bonding. Al is a softer material compared to TiW, and achieving an optimum setting for the wire-bonding procedure is difficult since too much

energy applied would break the Al wire, and too little energy would be insufficient for adhesion to make good quality bonds.

The system used for the deposition of these two electrode materials was the Plasmalab System 400 at RAL. These three films can be deposited consecutively without breaking the vacuum conditions, just by switching between two metal targets. The chamber was evacuated down to a base pressure of 10^{-6}Torr, and a 10sccm of Ar gas flow was injected. A d.c. power was applied and the process pressure maintained at 5mTorr.

The system used for RIE of these materials was the Plasmalab System 90 at RAL. The chamber was pumped down to a base pressures of 10^{-4}Torr and the required gases were admitted in. A power supply of a frequency range at ~13MHz was applied under a process pressure of 70mTorr.

The process conditions specific to the deposition and etching of these two materials are given individually below.

2.4.4.1 Top Electrode: Aluminium (Al)

Deposition

The growth parameters were determined for a deposition rate of 500Å/min, at an applied power of 5kW. A deposition time of 5 mins yielded an Al with a thickness of 2,500Å.

Etching

Gas used was 40sccm of $SiCl_4$ gas flow and at an applied power of 160W. An etch rate of 200Å/min for about 13 mins etch time yielded an Al layer of 2,500Å thickness.

2.4.4.2 Top Electrode: Titanium/Tungsten (TiW)

Deposition

The growth parameters were determined for a deposition rate of 200Å/min, at an applied power of 5kW. A deposition time of 7min 30sec yielded a TiW with a thickness of 1,500Å.

Etching

Gases used were 40sccm:10sccm of CF_4:O_2 gas flow and at an applied power of 120W. An etch rate of 600Å/min for about 2min 30sec yielded a TiW layer of 1,500Å thickness.

2.4.5 mmLETFEL Top Electrode Etch

As mmLETFEL device fabrication deals with relatively small geometry and pixel size, masking and patterning at the aperture region is crucial. Although photoresists are commonly used for masking of thin films due to their selective solubility with UV light exposure, however in this instance where high temperature is required, they can be damaged. As a substitution, a dielectric or metal mask is used as a sacrificial mask. After the deposition of this sacrificial mask, the dielectric or metal film has to be masked with photoresist initially, followed by patterning of the thin films using etching.

Deposition of the sacrificial mask

PECVD SiO_2 is used as the sacrificial mask, and a 2 μm thickness is deposited at a rate of 181Å/min using the Plasma Technology DP800 System at RAL. Gases used were 7sccm:200sccm of SiH_4:N_2O with a process pressure of 300mTorr at an applied power of 12W, and process temperature of 300°C.

Photoresist coating of the sacrificial mask

A conventional positive photoresist *Dynalith OFPR 800 cps 23* was spun for 60 sec at 5000 rpm onto the PECVD SiO_2 layer. It was then subjected to a soft bake for 2 mins at 95°C. The photoresist coating was exposed at 350 mJ/cm^2 for 40 sec using a Canon pla-500F mask aligner at TNTU. The mask CP06 was used for the patterning, and upon transfer of the pattern it was developed in an AZ726MIF developer at 21°C for 90 mins. It was then subjected to a hard-bake at 130°C for 1 hour. This yielded a 1μm photoresist layer (measured using the Tencor P-2 Long Scan profiler), which was sufficient for subsequent etching of the sacrificial layer and TAT electrode.

Figure 2-10 through to **Figure 2-13** show the systems used (as described above) for photoresist coating using the spinner, thin-film patterning via u-v exposure using the mask aligner, development of the patterned resist, and thin-film thickness scanning, at TNTU.

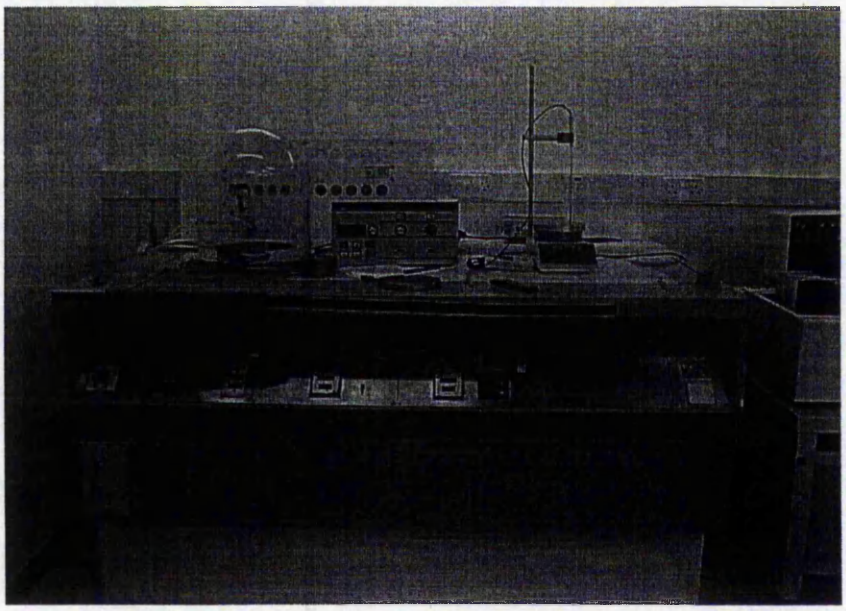


Figure 2-10: Photoresist spinner used for resist coating of thin-films at TNTU

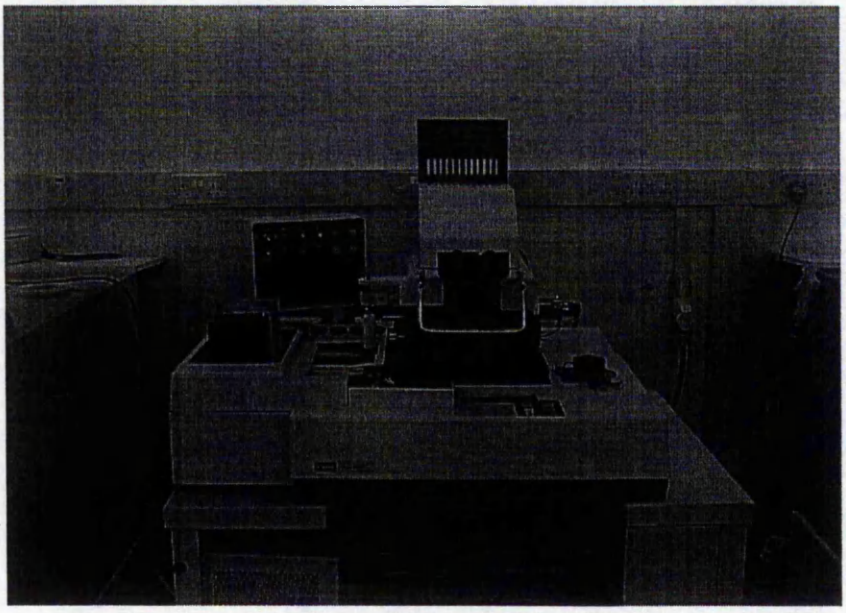


Figure 2-11: Mask aligner used for thin-film patterning via u-v exposure at TNTU

Figure 2-12: Platform used for development of photoresist after u-v exposure at TNTU

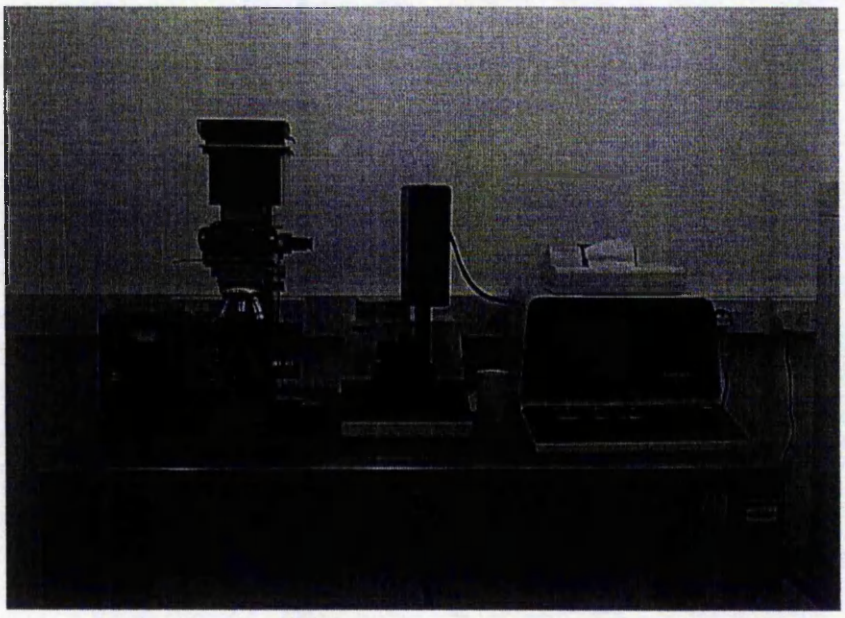


Figure 2-13: Scan profiler used for determining thickness of thin-films at TNTU

Etching of the sacrificial mask

The sacrificial mask, PECVD SiO_2 was RIE using 20sccm:2sccm of CHF_3:O_2 with the process pressure maintained at 100 mTorr. A power of 500W was applied at room temperature. The SiO_2 and photoresist etch rates were 560Å/min and 100Å/min respectively. A total process time of 45 mins was determined.

Etching of the TAT electrode

The process conditions for this particular step have been detailed in the previous section. The etching of the TAT electrode was done right after the etching of the SiO_2, without breaking the vacuum in the chamber.

Resist Removal

A 35sccm O_2 flow was injected at a process pressure of 200mTorr. Using an applied power of 100W, the process was maintained at an etch rate of 100Å/min for 8 mins.

2.4.6 mmLETFEL Aperture Profile Definition

Following the etching of the TAT electrode, aperture profile of the mmLETFEL device can be determined via ion beam milling technique by varying the ion beam density, the ion energy, and the angle of incidence of the ion beam, onto the loaded sample. These values can be determined individually so that different etch-rates can be achieved for a corresponding material. Optimisation of this technique was a concurrent programme researched at RAL, Oxford, using the Veeco 10'' Microetch System at RAL, and therefore, the aperture profile of the mmLETFEL test devices in this instance has not been determined. The etching conditions pertaining to this process are detailed elsewhere.[98]

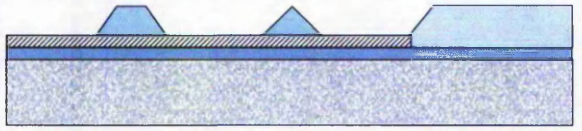
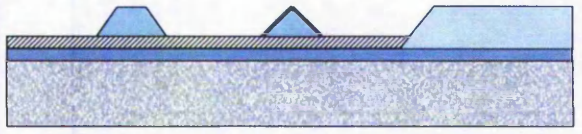
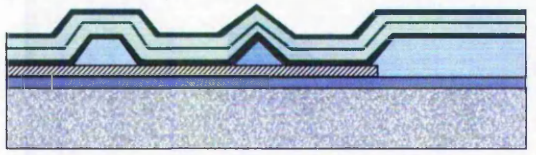
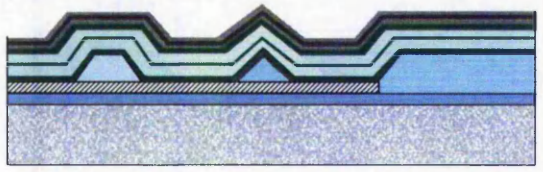
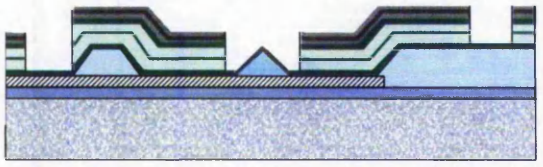
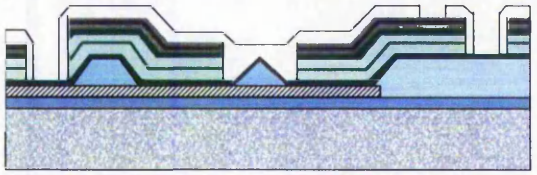
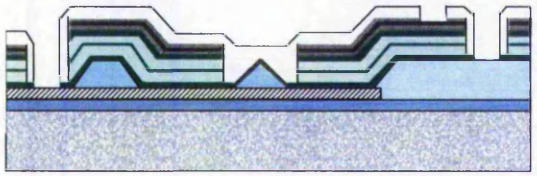
2.5 mmLETFEL Full Fabrication Route

This section illustrates a step-by-step fabrication route of the mmLETFEL test devices. **Table 2-2** lists these processes that the mmLETFEL test device fabrication has undergone, with the indication of the figure number each process relates to. The corresponding graphical illustration of these steps is shown in **Table 2-3** relating to **Figure 2-14.1** through to **Figure 2-14.13**. An overall illustration of the fully fabricated mmLETFEL device structure is shown in **Figure 2-15**. The description of the layers and denotations used in both **Table 2-3** and **Figure 2-15** is tabulated in **Table 2-4**. It is important to take note that several of the process steps detailed are concurrently being researched and the results being detailed elsewhere. These are indicated in italic font in Table 2-1, i.e. definition of the aperture via ion milling, etch of insulator at bondpad region, contrast layer fabrication, planarisation layer fabrication, and microlens fabrication. All mmLETFEL devices have been fabricated on a n-type, 2-6 Ωcm, (100±0.5)mm diameter and (525±50)μm thick Si substrate.

Process No.	Process Step/Name	Location	Technique/ Other Info.	Description	Figure No.
1a	Insulating material deposition	NMRC	Thermal Oxidation	5,000Å of T_{OX}	2-14.1
1b	Insulator definition	NMRC	Mask CP01		
1c	Insulator formed	NMRC	Plasma Etching		
2a	Base electrode material deposition	NMRC	(i) LPCVD (ii) d.c. magnetron sputtering	(i) 4,500Å of PolySi (ii) 3,000Å of TiW	2-14.2
2b	Base electrode definition	NMRC	Mask CP02		
2c	Base electrode formed	NMRC	Plasma Etching		
3a	Micro-mirror material deposition	NMRC	PECVD	15,000Å of SiO_2 45°-55° angle, 1.5μm height, 3μm width	2-14.3
3b	Micro-mirror definition	NMRC	Mask CP03		
3c	Micro-mirror formed	NMRC	Plasma Etching		
4a	*Micro-mirror metallisation deposition*	*NMRC*	*d.c. magnetron sputtering*	*500Å of TiW*	*2-14.4*
4b	*Metallised micro-mirror definition*	*NMRC*	*Mask CP05*		
4c	*Metallised Micro-mirror formed*	*NMRC*	*Plasma Etching*		

5	'barrier-layer' mmLETFEL material deposition	(i) TNTU (ii)Qudos	(i) r.f. magnetron sputtering (ii) PECVD	(i) 3kÅ/8kÅ/3kÅ Y_2O_3/ZnS:Mn/Y_2O_3 with a 'barrier-layer' of 100Å Y_2O_3 (ii) 3kÅ Si_3N_4 as insulator	2-14.5
6a	First level metallisation deposition	Qudos, RAL	d.c. magnetron sputtering	Tri-layer 1,500Å/2,500Å/1,500Å TiW/Al/TiW	2-14.6 and 2-14.7
6b	Sacrificial Mask deposition	Qudos, RAL	PECVD	2μm SiO_2	
6c	Sacrificial Mask/First level metallisation definition	TNTU	Mask CP06	Tri-layer 1,500Å/2,500Å/1,500Å TiW/Al/TiW 2μm SiO_2	
6d	First level metallisation formed	Qudos, RAL	RIE	Tri-layer 1,500Å/2,500Å/1,500Å TiW/Al/TiW	
7	*Aperture profile and contact definition*	*CMF, RAL*	*Ion Milling (Same Mask)*	*3μm aperture width*	*2-14.7*
8a	Passivation layer deposition	Qudos, RAL	PECVD	3,000Å Si_3N_4	2-14.8
8b	Passivation layer definition	TNTU	Mask CP07		
8c	Passivation layer formed	Qudos, RAL	RIE		
9	*Y_2O_3 etch at bondpad region*	*n/a*	*Mask CP08*	*n/a*	*2-14.9*
10a	Second level metallisation	Qudos, RAL	d.c. magnetron sputtering	5,500Å of Al	2-14.10
10b	Second level metallisation definition	Qudos, RAL	Mask CP09		
10c	Second level metallisation formed	Qudos, RAL	RIE		
11	*Contrast layer fabrication*	*TNTU*	*Mask CP10*	*Brewer Science DARC100 black polyamide material, ~1μm -1.5μm*	*2-14.11*
12	*Planarisation layer fabrication*	*CMF, RAL*	*Mask CP11*	*Photosensitive JSR PC302 planarisation material, ~1μm -5μm*	*2-14.12*
13	*Microlens fabrication*	*CMF, RAL*	*Mask CP12*	*JSR MFR340F lens material*	*2-14.13*

Table 2-2: List of the step-by-step processing route of a mmLETFEL device

Process No.	Figure No.	Graphical Illustration
1	2-14.1	
2	2-14.2	
3	2-14.3	
4	*2-14.4*	
5	2-14.5	
6	2-14.6	
7	2-14.7	
8	2-14.8	
9	2-14.9	

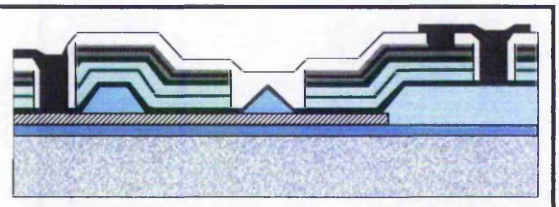
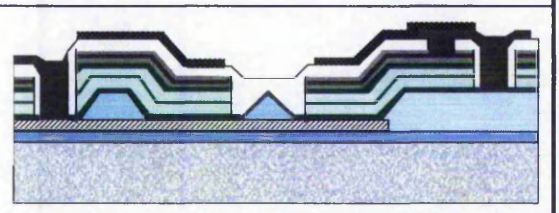
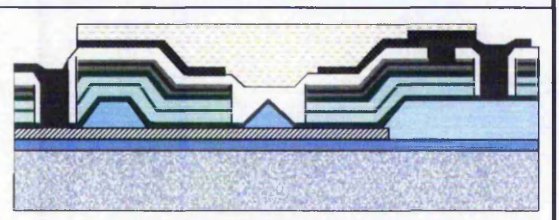
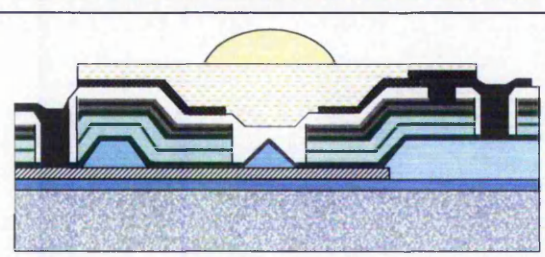
10	2-14.10	
11	*2-14.11*	
12	*2-14.12*	
13	*2-14.13*	

Table 2-3: Graphical illustration of the full processing sequence of a mmLETFEL device (Figure 2-14.1 to Figure 2-14.13)

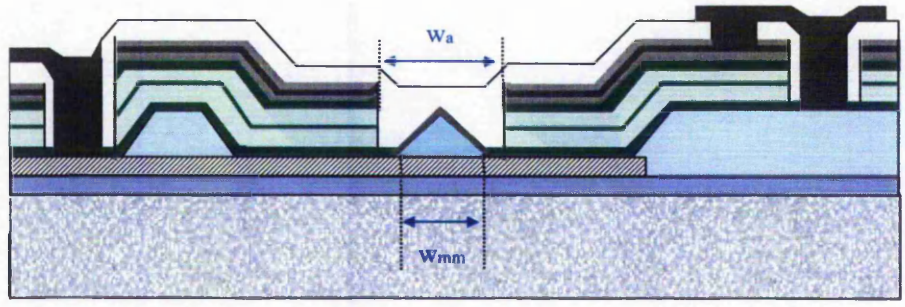


Figure 2-15: Fabricated mmLETFEL device structure investigated for this particular research programme (excluding those processes concurrently under investigation shown in italics in Table 2-1, Table 2-2 and Table 2-3)

	Description
w_a	Width of emitting aperture
w_{mm}	Width of micro-mirror

Layer	Description
	N-type Silicon
	Insulating Layer Material (Thermal Oxide, TOX)
	Base Electrode Layer Material (PolySilicon or Titanium/Tungsten)
	Micro-Mirror Layer Material (PECVD Silicon Dioxide, SiO_2)
	Metallisation Layer Material (Titanium/Tungsten, TIW)
	mmLETFEL Insulator Layer Material (Yytrium Oxide, Y_2O_3)
	mmLETFEL Phosphor Layer Material (Zinc Sulphide doped Manganese, ZnS:Mn)
	Metallisation Layer Material (Aluminium, Al)
	Passivation Layer Material (Silicon Nitride, Si_3N_4)
	Contrast Layer Material (Black Polyamide)
	Acrylic Planarisation Layer Material
	Acrylic Microlens Layer Material

Table 2-4: Description of the layers and denotations used in Table 2-3 and Figure 2-15 of the fully fabricated mmLETFEL device structure

2.6 FABRICATED mmLETFEL TEST DEVICES

In this section, **Figure 2-16** through to **Figure 2-18** show SEM pictures taken of actual mmLETFEL test devices being fabricated for various investigations. **Figure 2-16** shows the conventional non-etched mmLETFEL device and **Figure 2-17** the etched mmLETFEL device utilising the ion milling technique. Finally, **Figure 2-18** depicts the profile of the mmLETFEL test device being used in this particular research, i.e. in this case, with the base electrode fabricated.

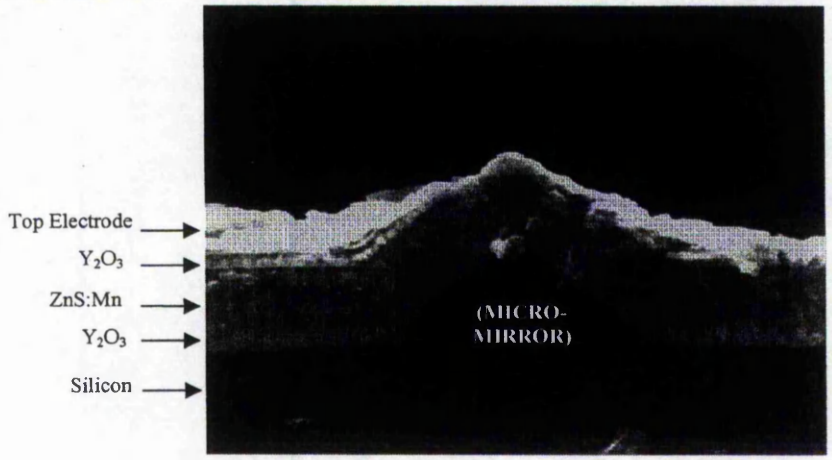


Figure 2-16: A conventional mmLETFEL device with non-etched aperture profile

Figure 2-17: A mmLETFEL device with etched aperture profile, utilising the ion milling technique (courtesy from S.O. Barros)

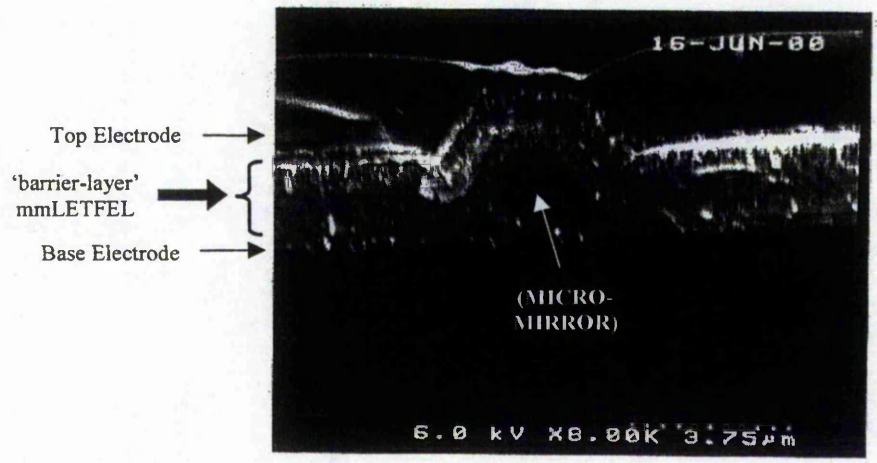


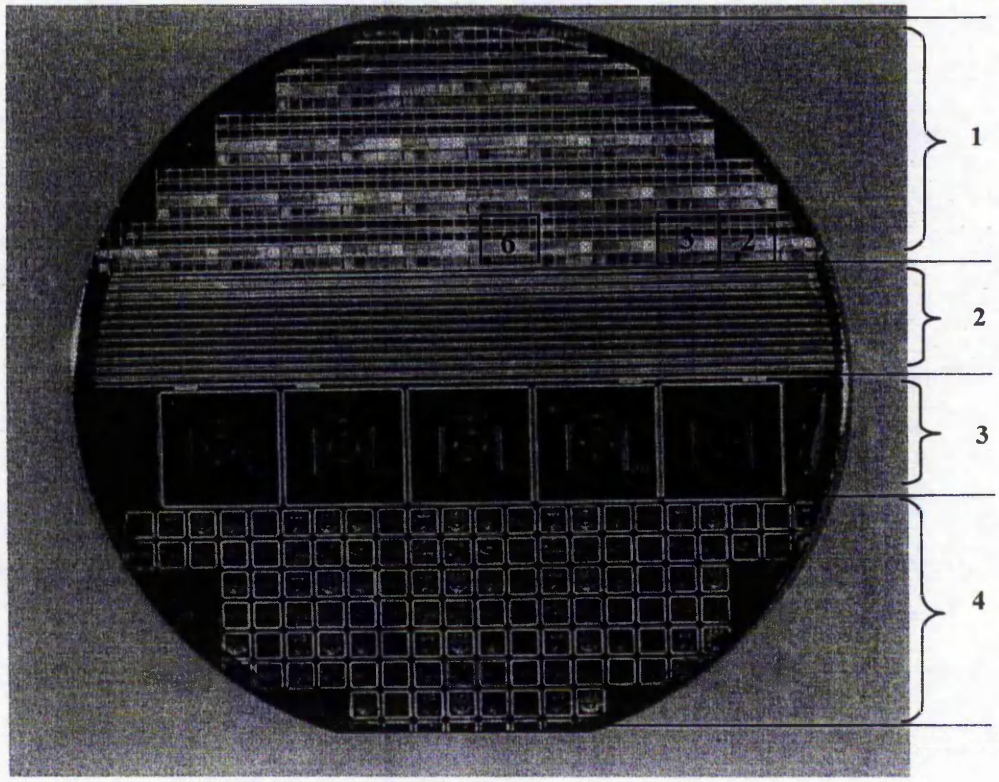
Figure 2-18: mmLETFEL test device primarily utilised in this investigation – containing fabricated base electrode and 'barrier-layer' mmLETFEL structure

2.7 CONCLUSION

To conclude, the full fabrication route of an mmLETFEL device being investigated under various programmes has been explained and detailed above, in particular special attention has been paid to the processing sequences pertaining to this investigation. This include most importantly the fabrication of the base electrodes, PolySi and TiW, and secondly the deposition of PECVD Si_3N_4 as an alternative insulator material.

Test wafers with mmLETFEL devices grown utilising the mask set explained above have been successful. The mmLETFEL test devices being fabricated for this investigation have been characterised, and the technique as well as the results, of both the electrical and the optical characterisation, are explained and detailed in the next chapter.

Please refer to the following chapter for a list of test wafers which have been fabricated and characterised. The following **Figure 2-19** shows the types of devices found on a typical test wafer, while **Figure 2-20** illustrates a typical printer test device and the corresponding die while under test probe.

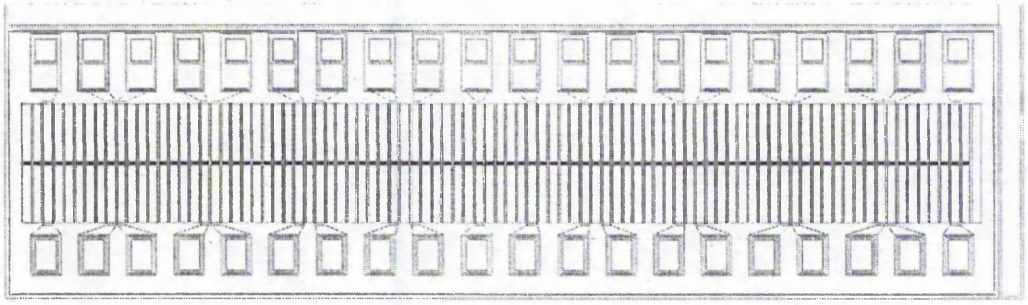


No.	mmLETFEL Devices	Die Dimensions
1	Test Devices	1.8mm x 1.6mm
2	Printer Devices	4.1mm x 1.2mm
3	Large-Area Displays	16mm x 16mm
4	Small-Area Displays	4mm x 4mm

Figure 2-19: A test wafer illustrating the mask set used for the fabrication of mmLETFEL devices in this investigatio

N. B.

1. There are 20 test devices fabricated in a repetitive fashion within section no. 1 of a test wafer as indicated above, and the area encompassing these 20 test devices is called a test cell. Boxed no. 2, 3 and 6 (for test cells no 2, 3 and 6 respectively) have been shown above.
2. All these devices are illustrated further in Appendix A1 through to Appendix A3.



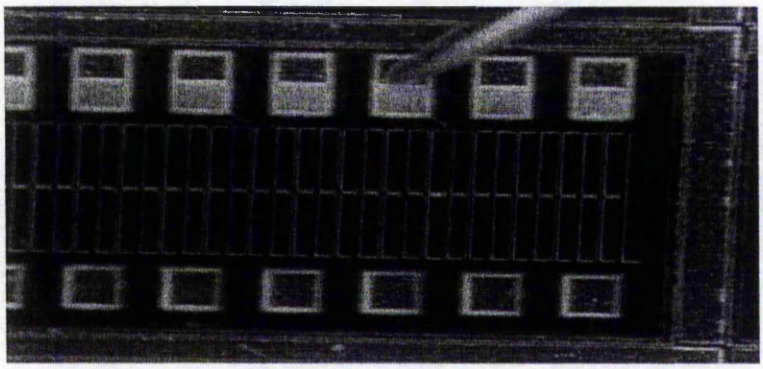


Figure 2-20: Illustration of a mmLETFEL printer test device and the corresponding test die while under probe

Contents

3 Characterisation of mmLETFEL Test Devices

3 CHARACTERISATION OF mmLETFEL TEST DEVICES

3.1 INTRODUCTION

In this chapter, the electrical and optical characterisations of the fabricated mmLETFEL test devices are detailed and the measurement results obtained are explained and discussed. An outline of the test wafers fabricated for these characterisations and the mmLETFEL test device structures (die dimensions and corresponding illustrations), are also given.

Figure 3-1 and **Figure 3-2** show two wafer prober stations used for characterisation purposes of mmLETFEL test wafers. For either electrical or optical characterisations, the drive voltage was fed via an amplifier and supplied from the Tektronix AFG5101 Programmable Arbitrary/Function Generator (for the main prober station), and from the Thurlby Thandar Instruments TG1010 Programmable 10MHz Function Generator (for the secondary prober station).

Instantaneous voltages at desired circuit nodes during any characterisations or tests in either prober stations were observed using the Tektronix TDS210 2-channel Digital Oscilloscope. For the main probe station, observations and measurements for any characterisations were recorded manually, while the secondary prober station had been equipped with a software tool for automated computation and record of measurement results. Various programs had been written for this purpose, and will be explained briefly in each of the characterisation techniques detailed in the relevant sections later in the chapter.

Depending on the type of characterisation being performed, appropriate adjustments were made to the wafer prober station accordingly. The corresponding equipment used in any instance will also be detailed in the relevant sections.

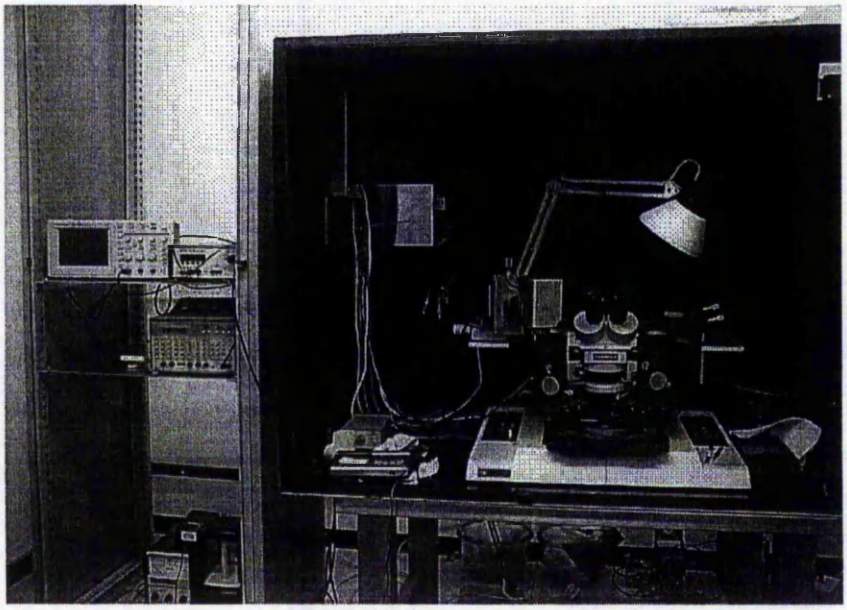


Figure 3-1: The main wafer prober station used for characterisation of mmLETFEL test devices

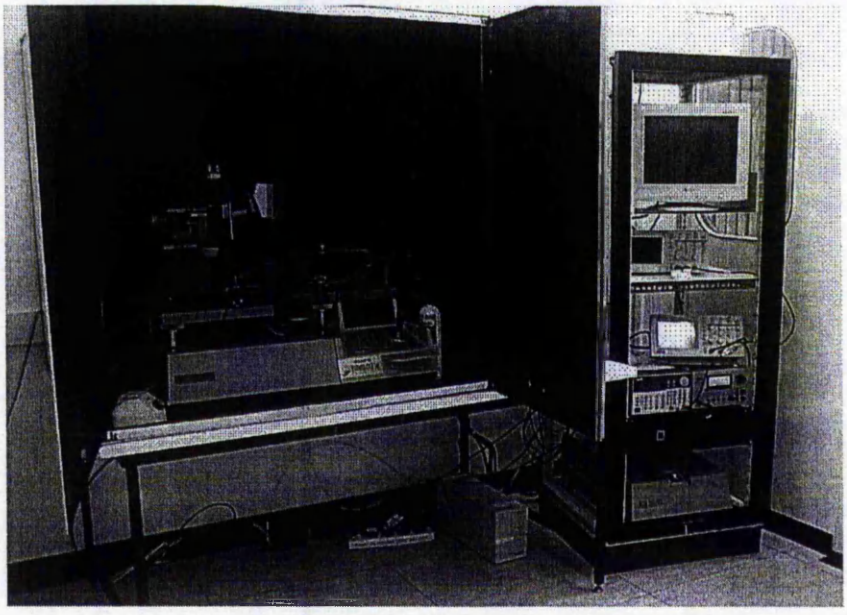


Figure 3-2: The secondary wafer prober station used for characterisation of mmLETFEL test devices

3.2 mmLETFEL Test Device Structures

Many test wafers had been grown for characterisation purposes, and **Table 3-1** lists all of these test wafers that had been fabricated, and their corresponding descriptions. Brief comments on the outcome of these fabricated test devices are also included. For these listed wafers which had been grown with micro-mirror structures on Si wafer, they utilise the 100Å Y_2O_3 'barrier-layer' sandwiched between two stacks of 4000Å ZnS:Mn phosphor layers, 3000Å of insulator layers, and 1.5kÅ/2.5kÅ/1.5kÅ of TAT top electrode. As these were fully-fabricated mmLETFEL devices, there was also a Si_3N_4 passivation layer with a thickness of 3000Å. All other fabrication steps will remain the same unless otherwise stated; the fabrication details of which have already been explained in the previous chapter.

Test Wafer Nos.	Metallised Micro-Mirror	Base Electrode	Insulator	Top Electrode	Anneal Temp.	Comments
NTU127	None	None	Y_2O_3	Al	700°C	OK
NTU172	None	None	Y_2O_3	Al	700°C	OK
NTU356	None	None	Y_2O_3	Al	700°C	OK
NTU428	None	TiW	Y_2O_3	TAT	500°C	Unstable devices (early breakdown observed)
NTU429	None	PolySi	Y_2O_3	TAT	500°C	
NTU430	None	PolySi	PECVD Si_3N_4	TAT	500°C	OK
NTU431	None	TiW	PECVD Si_3N_4	TAT	500°C	OK
NTU449	TiW	None	r.f. sputtered Si_3N_4	TAT	500°C	OK
NTU450	TiW	None	PECVD Si_3N_4	TAT	500°C	OK
NTU592	None	None	Y_2O_3	TAT	500°C	No or weak photo-luminescence (PL) observed due to phosphor contamination (NTU595, NTU599 and NTU600 wafers were crazed)
NTU593	None	PolySi	Y_2O_3	TAT	500°C	
NTU594	None	TiW	Y_2O_3	TAT	500°C	
NTU595	None	TiW	PECVD Si_3N_4	TAT	500°C	
NTU596	None	PolySi	PECVD Si_3N_4	TAT	500°C	
NTU597	None	None	PECVD Si_3N_4	TAT	500°C	
NTU598	TiW	None	PECVD Si_3N_4	TAT	500°C	
NTU599	None	None	PECVD Si_3N_4	TAT	700°C	
NTU600	TiW	None	PECVD Si_3N_4	TAT	700°C	
CR46	None	PolySi	Y_2O_3	TAT	500°C	No PL observed due to chamber contamination
CR47	None	TiW	Y_2O_3	TAT	500°C	
CR123	None	TiW	Y_2O_3	TAT	500°C	OK
CR128	None	PolySi	Y_2O_3	TAT	500°C	OK

Table 3-1: List of the test wafers fabricated and their corresponding descriptions

It is important to note that the problems associated with some of the non-functional test wafers were mainly due to fabrication problems that emerged which affected the overall mmLETFEL device reliability and performance. These problems include irregularity in the calibration of the PECVD Si_3N_4 deposition process (during the second-year of the research programme), alignment errors involved during the masking of the mmLETFEL device for aperture and electrode definition (during the second-year of the research programme), contamination of the ZnS:Mn phosphor powder (before the laboratory relocation during the final-year of the research programme), and contamination of the deposition chamber (after the laboratory relocation). Therefore, there was only a limited number of working test wafers available for the electro-optical characterisations.

For an illustration of the characterised mmLETFEL test devices, the following **Table 3-2** through to **Table 3-5** list the respective annotations with the graphical representation of these test devices and their corresponding die structure dimensions (all lengths and widths are quoted in μm).

mmLETFEL Test Devices	Description			Illustration (Die Dimensions: 1.7mm x 1.5mm)
	Sidewall Widths	Resolution (p.p.i.)	Devices per die	
L65	2	200	11	
L66	4			
L67	6			
L68	10			
L69	2	300	17	
L70	4			
L71	6			
L72	10			
L73	2	600	35	
L74	4			
L75	6			
L76	10			
L77	2	1200	70	
L78	4			
L79	6			
L80	10			

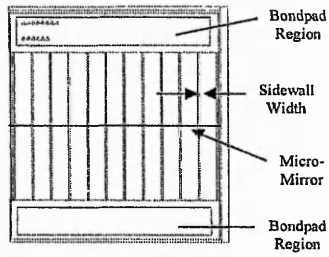


Table 3-2: List of characterised mmLETFEL test device structures, their dimensions and graphical illustrations (for L65-L80)

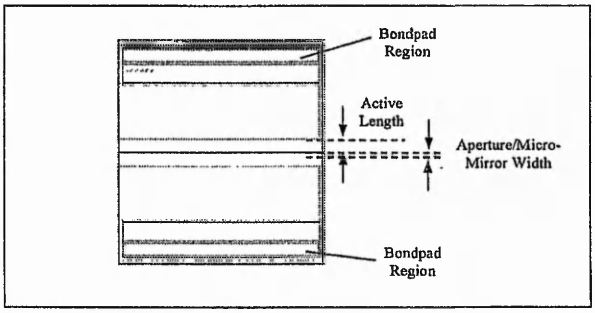
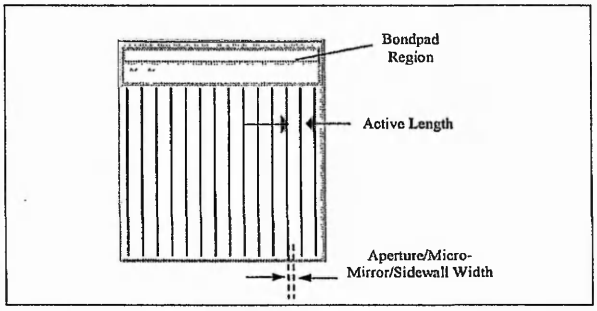
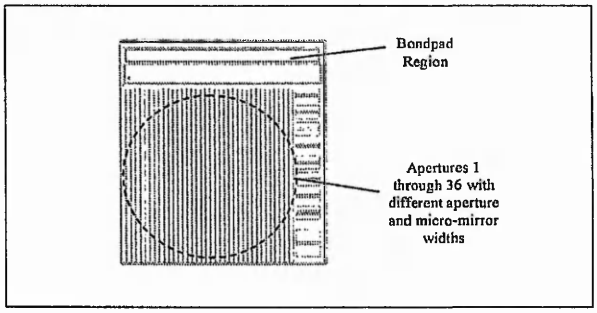
mmLETFEL Test Devices	Description		Illustration (Die Dimensions: 1.8mm x 1.6mm)
	Active Lengths	Aperture Widths	
TDEV01	10	3	
TDEV02	20	3	
TDEV03	30	3	
TDEV04	40	3	
TDEV05	50	3	
TDEV06	100	3	
TDEV07	200	3	
TDEV08	300	3	
TDEV11	5	3	
TDEV12	10	3	
TDEV13	15	3	
TDEV14	20	3	
TDEV15	25	3	
TDEV16	30	3	
TDEV17	40	3	
TDEV18	50	3	
TDEV19	100	3	
TDEV20 (see table below for dimensions on apertures nos. 1 to 36)	30	Variable	

Table 3-3: List of characterised mmLETFEL test device structures, their dimensions and graphical illustrations (for TDEV01-08, TDEV11-20)

mmLETFEL TDEV20	Description		mmLETFEL TDEV20	Description	
	Micro-Mirror Width	Aperture Width		Micro-Mirror Width	Aperture Width
1	3	3	19	4	3
2	3	3	20	4	3
3	3	3	21	4	3
4	3	3.5	22	4	3.5
5	3	3.5	23	4	3.5
6	3	3.5	24	4	3.5
7	3	4	25	4	4
8	3	4	26	4	4
9	3	4	27	4	4
10	3.5	3	28	4.5	3
11	3.5	3	29	4.5	3
12	3.5	3	30	4.5	3
13	3.5	3.5	31	4.5	3.5
14	3.5	3.5	32	4.5	3.5
15	3.5	3.5	33	4.5	3.5
16	3.5	4	34	4.5	4
17	3.5	4	35	4.5	4
18	3.5	4	36	4.5	4

Table 3-4: Description of mmLETFEL test device TDEV20 (for apertures 1 to 36)

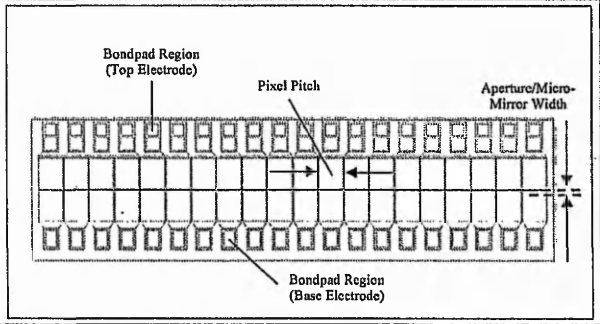
mmLETFEL Printer Test Devices	Description		Illustration (Die Dimensions: 4.1mm x 1.2mm)
	Devices per die	Pitch	
130 dpi	20	193.5	
300 dpi	45	85.0	
600 dpi	90	42.5	
For all these printer test devices, active length is at 250μm on either side feeding into a 3μm width reflecting micro-structure, with the aperture size at 3μm.			

Table 3-5: Description of mmLETFEL printer test device structures, their dimensions and graphical illustrations (for 130, 300 and 600dpi)

3.3 mmLETFEL Measurement and Characterisation Techniques

Electro-optical characteristics of the fabricated mmLETFEL test devices were primarily analysed by results obtained from the charge-voltage (Q-V),[99, 100, 101] and luminance-voltage (L-V),[60] measurements. The capacitance-voltage (C-V) technique,[102] on the other hand, was used to determine the dielectric constant of the crucial materials in the few mmLETFEL test device structures fabricated for these characterisation purposes. The device performances, such as transferred charge, power dissipation, and luminance, were also evaluated and expressed in terms of the layer thickness, the dielectric constant, the threshold field and the luminous efficiency.

In all cases when comparing the electrical and optical characteristics for each mmLETFEL test device configuration, it is essential that the specific drive conditions, i.e. the drive waveform, the drive voltage, and the drive frequency, are cited clearly. This is desirable because the EL excitation and thus the luminance observed of any TFEL devices (and here, mmLETFEL test devices), is largely dependent on these parameters.

The characterisations performed on mmLETFEL test devices have been primarily concerned with comparison of the same test device number among several test cells (see **Figure 2-19**) on a particular test wafer. This allows for determination of the margin of experimental error in measurements. The results obtained are then compared to that from another test wafer where only one variable has been changed each time.

Table 3-6 summarises the optical and electrical characterisations conducted on only the operational mmLETFEL test devices of the corresponding test wafers as listed in **Table 3-1**, accompanied by the specified drive conditions. S, Q, and T, correspond to sinusoidal, square, and triangular, waveforms, respectively; and the unit for the drive frequency is quoted as kHz. Characterisation techniques are denoted as L-V for luminance versus drive voltage measurements; Q-V for charge versus drive voltage measurements; and Image Profile for the digital image capture and technique of evaluating the relative luminous intensity of various apertures. Annotations used for the names of the test devices are the same as those listed in **Table 3-2** through to **Table 3-5**.

Test Wafer Nos.	Characterisation			
	Type	Drive Frequency	Drive Waveform	Test Devices
NTU127	L-V	5	Q	L65-L80
NTU172	L-V	1, 5	S/Q/T	TDEV01- 07,09,10 TDEV12-19
		10	Q	TDEV01-08 TDEV12-19
	I-V	1, 2, 5, 10, 15, 20	Q	130dpi
NTU356	L-V	1, 2, 5, 10	S/Q	TDEV11-19
	Image Profile	5	S	TDEV20
		5	S	130dpi, 300dpi, 600dpi
	Q-V	5	S	TDEV11-19
NTU428	L-V	1, 2, 5, 10	S/Q	TDEV11
	Q-V	5	S	TDEV11,12
NTU429	Q-V	5	S	TDEV11
NTU430	L-V	1, 2, 5, 10	S/Q	TDEV11-19
	Q-V	5	S	TDEV11,12
NTU431	L-V	1, 2, 5, 10	S/Q	TDEV11-19
	Q-V	5	S	TDEV11,12
NTU449	L-V	1, 2, 5 10	S/Q	TDEV11-19
	Q-V	5	S	TDEV11,12
NTU450	L-V	1, 2, 5, 10	S/Q	TDEV11-19
	Q-V	5	S	TDEV11,12
CR46	Q-V	5	S	TDEV11,12
CR47	Q-V	5	S	TDEV11,12
CR123	L-V	5	S	TDEV11-19
	I-V	5	S	TDEV11-19
	Q-V	5	S	TDEV11-19
CR128	L-V	5	S	TDEV11-19
	I-V	5	S	TDEV11-19
	Q-V	5	S	TDEV11-19

Table 3-6: List of the test wafers fabricated and the types of characterisations conducted (where S, Q, and T, correspond to sinusoidal, square, and triangular, waveforms, respectively; and drive frequency is cited in kHz)

3.3.1 Optical Characterisation

For the L-V characterisation, the test wafer was held in place by a metallic plate in a typical wafer prober station (as shown in **Figure 3-1** and **Figure 3-2**), which was connected to a vacuum pump to ensure good adhesion to the Si substrate. The luminance values were measured using the Minolta LS-110 Luminance Meter that was mounted at a distance of 20cm in a vertical position from the test wafer. The luminance meter has an internal lens system of a 1/3° angle acceptance cone focused on the surface-emitting region.

A program was computed using the National Instruments LabVIEW Version 5.0, a graphical programming for instrumentation tool software, to capture the values of the luminance values obtained into the computer. The parameters and values of the drive waveform, drive voltage, drive frequency, and luminance, were also measured and recorded. An L-V curve is obtained by plotting the luminance value versus the corresponding drive voltage as it increases to a peak value. **Figure 3-3** shows a simple block diagram of the optical measurement system.

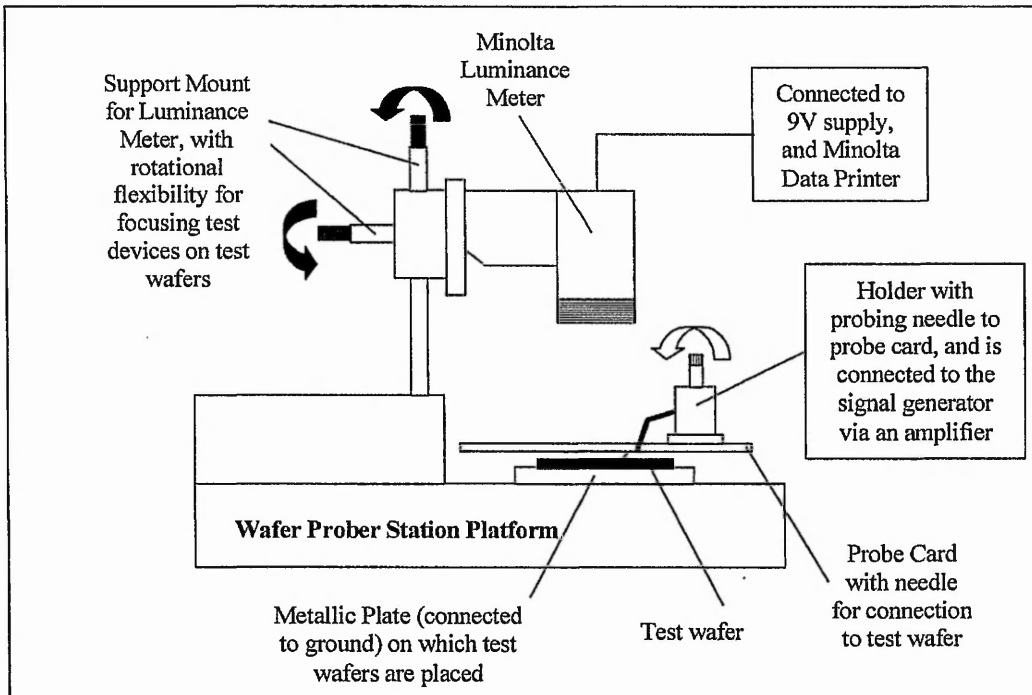


Figure 3-3: Block diagram of the configuration used for optical characterisation

The luminance value that is recorded by the luminance meter is measured by the acceptance cone that is focused on the test device where the emitting region is present. If the emitting region is larger than this circle of focus, it can be concluded that the luminance value measured and recorded correspond exactly to the intensity of the light which is being emitted in this instance.

However, if the emitting region is smaller than this circle of focus, the actual value for the emitting region in such cases will have to be calculated. In other words, a multiplying factor has to be determined for all the test devices where the emitting regions are smaller than the circle of focus, in order to calculate their true luminance values.

The circle of focus has a diameter of 1.1mm, thus giving the area of the circle to be, $A_c = 9.503 \times 10^{-7} m^2$. The measured luminance value, $L_{measured}$, is corrected by multiplying this luminance value with a factor, K, to obtain the actual luminance value, $L_{corrected}$, that corresponds to the actual intensity that is emitted from the emitting region of a given test device. Where the factor, K, is merely the ratio of the area of the circle of focus to that of the emitting region within that circle.

By knowing and calculating the total area of the emitting region for each specific test device to be characterised within the area of the circle of the focus, the multiplying factor can then be determined, as shown in **Equation 3-1** and **Equation 3-2**.

$$L_{corrected} = L_{measured} \times K \qquad \textbf{Equation 3-1}$$

Thus, giving the multiplying factor as,

$$K = \frac{A_c}{A_{emit}} = \frac{9.503 \times 10^{-7}}{A_{emit}} \qquad \textbf{Equation 3-2}$$

where A_{emit} is the area of the emitting region for each measured test device.

Table 3-7 lists the calculated factor, *K*, for each of the mmLETFEL test devices used for characterisation.

mmLETFEL Test Devices	Factor, K
TDEV01 - TDEV08	287.97
TDEV11	2.67
TDEV12	4.34
TDEV13	6.13
TDEV14	7.68
TDEV15	9.33
TDEV16	11.00
TDEV17	14.37
TDEV18	17.78
TDEV19	34.84
130dpi	1863.33
300dpi	5279.44
600dpi	17598.15
L65 - L80	215.98

Table 3-7: Calculated multiplying factor, K, used for correction of luminance values measured of mmLETFEL test devices

To evaluate the luminance values obtained for mmLETFEL TDEV20 especially (as illustrated in **Table 3-3**), the Pulnix TM6AS was mounted in place of the luminance meter for this purpose. A visual video image capture of a test device being driven was recorded using another computed LabVIEW program. The pixels of the captured image were then computed at grey-scale levels using the Scale & Profile software. Thus, the luminous intensity from one specific aperture to another can then be compared between the relative grey-level values obtained. In this case, the luminous intensities of the 36 apertures designed in TDEV20 are being compared, involving varying sizes in both micro-mirror and emitting aperture widths.

3.3.2 Electrical Characterisation

By employing a sensor device – either a resistor or a capacitor with known values, and connecting it in series with the mmLETFEL test device, the current-voltage (I-V) and charge-voltage (Q-V) characteristics of the devices can be found. Here, two separate LabVIEW programs were accessed for each characterisation respectively. The measurements were recorded, and the curves plotted and used for analysis and comparison. From these measurements, the capacitance-voltage (C-V) characteristics can also be analysed to aid in the determination of mmLETFEL electrical properties.

Figure 3-4 below shows a simple block diagram of the circuit configuration used. The function generator feeds the amplifier that drives the mmLETFEL test device via a series device, usually a resistor (100Ω) for current limitation, and a sense device. An a.c. signal was applied, and the drive voltage, $v_1(t)$, and the voltage drop across the mmLETFEL test device, $v_L(t) = [v_2(t) - v_3(t)]$, were measured.

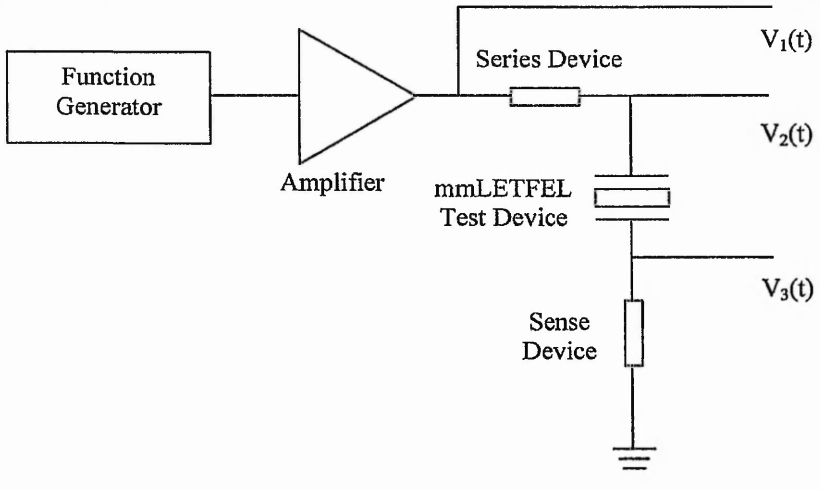


Figure 3-4: Block diagram of the circuit configuration used for electrical characterisation

A Q-V curve is obtained by plotting the instantaneous charge, $q(t)$, against the voltage across the mmLETFEL test device, $v_L(t)$. The $q(t)$ is best obtained from a circuit configuration that uses a sense capacitor, C_s, as compared to one that uses a sense resistor, R_c, because the sense capacitor accounts for the integration constant responsible for giving the appropriate Q-V offsets that can be found along the y-axis of the Q-V curve. In this case, the instantaneous charge can be calculated directly by,

$$q(t) = C_s \times v_3(t) \qquad \textbf{Equation 3-3}$$

From **Equation 3-3**, the current expression can then be calculated from,

$$i(t) = \frac{dq(t)}{dt} = C_s \times \frac{dv_3}{dt} \qquad \textbf{Equation 3-4}$$

or, alternatively, if a series resistor (R_s) was also utilised, the current expression becomes,

$$i(t) = \frac{v_2(t) - v_1(t)}{R_s} \qquad \textbf{Equation 3-5}$$

However, for a circuit configuration that uses a sense resistor (R_c) instead (whether or not a series resistor was also used), the current expression would then be calculated from,

$$i(t) = \frac{v_3(t)}{R_c} \qquad \textbf{Equation 3-6}$$

Thus, the I-V curve can also be obtained by plotting the calculated instantaneous current, $i(t)$, versus the voltage drop across the mmLETFEL test device, $v_L(t)$.

When analysing the C-V characteristics of the mmLETFEL test device, the C-V curve is obtained by plotting both the capacitance, and voltage drop, across the mmLETFEL test device. The dynamic capacitance across the mmLETFEL test device is given by,

$$C[v_L(t)] = \frac{dq(t)}{dv_L(t)} \qquad \textbf{Equation 3-7}$$

where it is the first derivative of the charge with respect to the voltage drop across the mmLETFEL test device respectively.

Alternatively, it is also equivalent to the total current divided by the time derivative of the voltage drop across the mmLETFEL test device respectively. Using **Equation 3-4**, the dynamic capacitance can also be found as,

$$C[v_L(t)] = \frac{i(t)}{\frac{d[v_L(t)]}{dt}}$$ **Equation 3-8**

The following **Table 3-8** summarises the circuit configuration methods mentioned thus far, and related current, charge and capacitance expressions.

No	Circuit Configurations		Current Expressions	Charge Expressions	Capacitance Expressions
	Series Device	Sense Device			
1	None	Capacitor	$i(t) = \frac{dq(t)}{dt} = C_s \times \frac{dv_3}{dt}$	$q(t) = C_s \times v_3(t)$	$C[v_L(t)] = \frac{dq(t)}{dv_L(t)}$
2	Resistor	Capacitor	$i(t) = \frac{v_2(t) - v_1(t)}{R_s}$		$C[v_L(t)] = \frac{i(t)}{\frac{d[v_L(t)]}{dt}}$
3	None	Resistor	$i(t) = \frac{v_3(t)}{R_c}$	$q(t) = \frac{1}{R_c}\int_0^T v_3(t)dt$	
4	Resistor	Resistor			

Table 3-8: Summary of circuit configuration used and related electrical expressions

For the electrical characterisation in this investigation, the Q-V characterisation has been performed using the circuit configuration no. 2 (R_s=*100Ω* and C_c=*9.84x10^{-8}F*), and the I-V characterisation has been performed using circuit configuration no. 4 (R_s=*100Ω* and R_c=*1kΩ*).

3.4 mmLETFEL TEST DEVICE PARAMETERS

Prior to device characterisation, parameters such as the dielectric constant of the respective insulator materials, and sheet resistance of the respective base electrode layer materials, used in the various device configurations have to be determined.

The dielectric constants of the insulator materials Y_2O_3, PECVD and sputtered Si_3N_4 were measured and recorded here at TNTU, Nottingham. The measurement was performed using the C-V technique via the use of a HP4192A LF Impedance Analyser, where the average accumulation capacitance of a thin film was measured with respect to the d.c. bias voltage applied. A Si wafer with a single thin-film material that was to be tested was grown for this purpose. Evaporation of Al material onto the grown thin-film with the use of an electrode mask with test diodes of known area, as well as onto the back of the Si wafer for better conductivity, completes the circuit.

Figure 3-5 and **Figure 3-6** show the system used for Al evaporation, and the wafer prober station used primarily for determination of the dielectric constant of thin-films grown via the C-V technique, respectively.

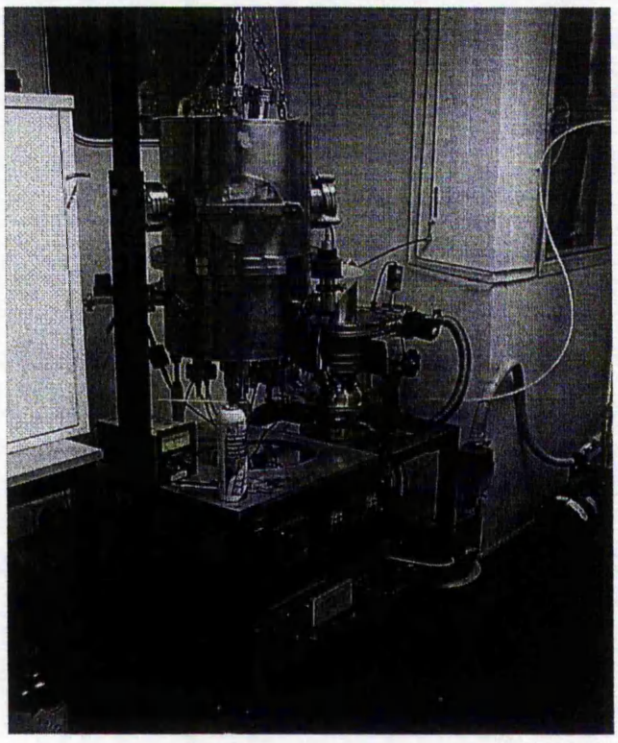


Figure 3-5: System used for evaporation of Al material at TNTU

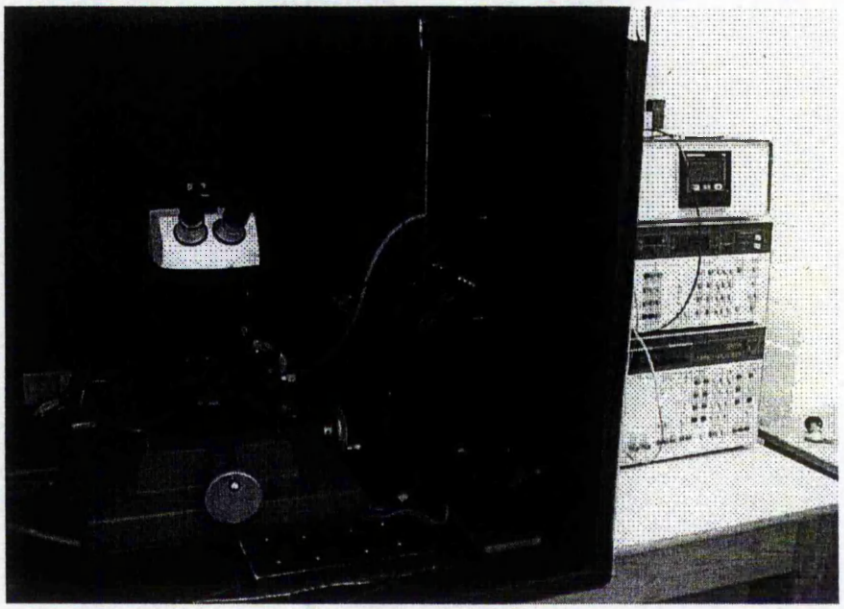


Figure 3-6: Wafer prober station used primarily for C-V characterisation of thin-films

The dielectric constant of a given material, ε_r, can thus be calculated.

$$C = \frac{\varepsilon_o \varepsilon_r A}{d} \qquad \textbf{Equation 3-9}$$

$$\varepsilon_r = \left(2.7135 \times 10^9\right) \times C \cdot d \qquad \textbf{Equation 3-10}$$

where C is the average accumulation capacitance measured, d is the average measured thickness of the test diodes, A is the known area of the test diodes at 3.08×10^{-6} m^2, and ε_o is the permittivity of vacuum at 8.854×10^{-12} F/m.

Measurement of the sheet resistance of the base electrode materials, TiW and PolySi, were performed at NMRC, Cork. These measurements and those of the dielectric constants of the insulator materials mentioned previously are tabulated in the following.

Materials	Dielectric Constant	Materials	Sheet Resistance (Ω/sq)
ZnS:Mn	8.3 ± 0.1	TiW	2.46
Y_2O_3	11.9 ± 0.1	PolySi	15.72
PECVD Si_3N_4	6.8 ± 0.2		

Table 3-9: Device parameters determined for insulator and base electrode materials

3.5 mmLETFEL Electro-Optical Characteristics

Understanding of the mmLETFEL device characteristics and performance can best be analysed from the electro-optical characteristics obtained from measurements made using the L-V and Q-V techniques.[103]

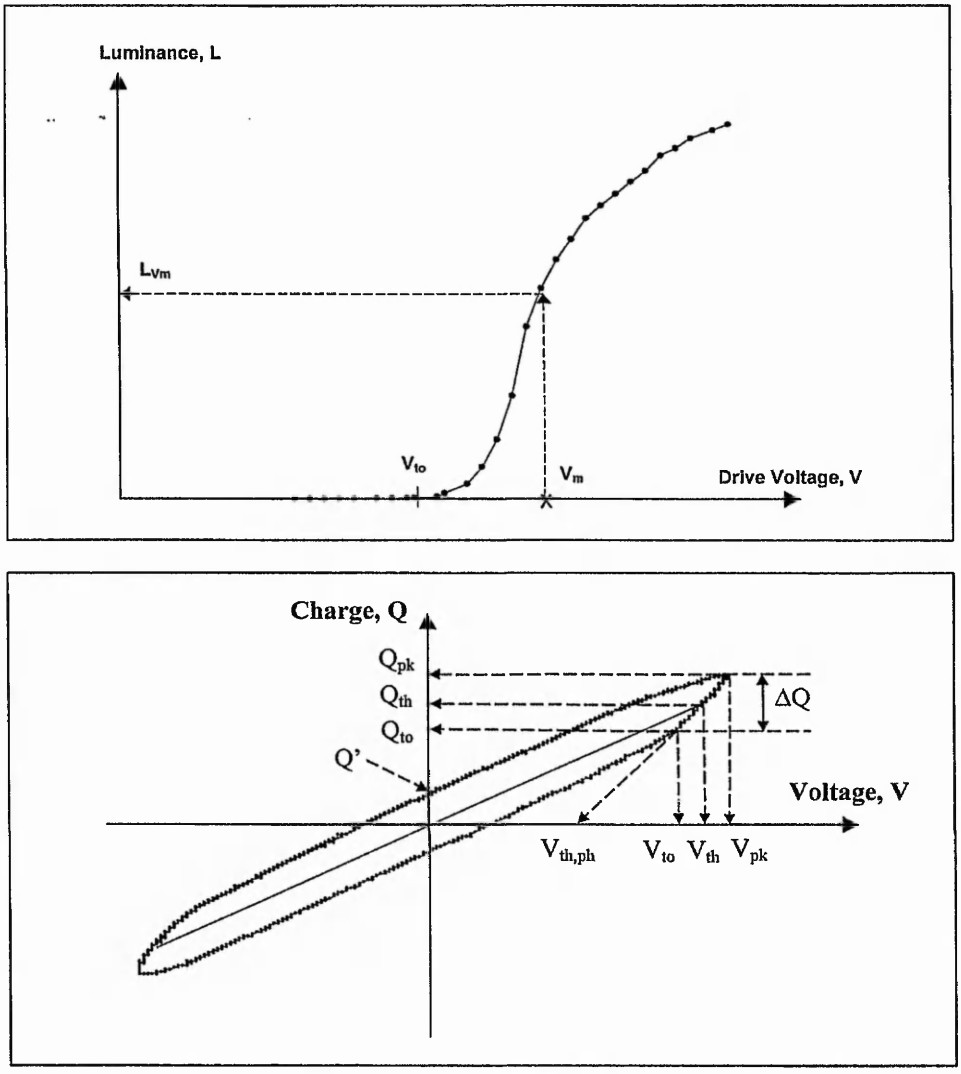


Figure 3-7: Typical L-V and Q-V characteristics obtained for a mmLETFEL test device

The above figures depict the typical L-V and Q-V curves of a mmLETFEL device, and the important parameters that can be approximated from these plots are also indicated, where explanation of these parameters and what evaluations can be achieved for the mmLETFEL device follows. From the L-V curve, V_{th} is the threshold voltage of the device; V_{m1}, V_{m2} and

V_{m3} are three various points of the drive voltages relative to V_{th}, with their corresponding luminance values at L_{Vm1}, L_{Vm2} and L_{Vm3}. From the Q-V curve, V_{th} has the same definition as in the L-V curve, V_{to} is the drive voltage corresponding to the device turn-on, V_{pk} is the peak drive voltage; and the corresponding charge values at Q_{th}, Q_{to}, and Q_{pk}. Q' is the remaining charge after the drive voltage returns to zero, and ΔQ is the transferred charge density of the device. $V_{th,ph}$ corresponds to the threshold voltage for the phosphor layer.

When the driving voltage applied to a mmLETFEL test device is below the device threshold voltage, the Q-V curve is represented by a straight line passing through the origin. Since the mmLETFEL structure is considered as a series of capacitors, thus the total capacitance of the device before the threshold is reached can be calculated from the slope of this particular line.

$$Q = C_{off} \cdot V \qquad \textbf{Equation 3-11}$$

where C_{off} is the total capacitance before the device is turned on.

Once the driving voltage reaches and increases above the device threshold voltage, this Q-V line starts to spread out into a parallelogram as shown in **Figure 3-7**. The outspread of the curve is equal from both sides of the straight line $Q = C_{off} \cdot V$, and this line through the origin can now also be given as,

$$Q_{th} = C_{off} \cdot V_{th} \qquad \textbf{Equation 3-12}$$

where V_{th} is the threshold voltage of the mmLETFEL test device with Q_{th} as the corresponding threshold charge density. The slopes on either side of this line that crosses the y-axis are parallel and therefore they can be given as C_{off} too.

The slopes on the remaining sides of the parallelogram however can be indicated as C_{on} as this represents the total capacitance after the device is turned on. The slope is then given by,

$$Q - Q_{th} = C_{on}(V - V_{th}) \qquad \textbf{Equation 3-13}$$

Now, C_{off} represents the total capacitance comprising of the phosphor and insulator capacitances before the device is turned on, and C_{on} represents the total capacitance comprising only of the insulator capacitances after device turn-on. Thus the respective equations are as follows,

$$C_{off} = \frac{C_{i1} \cdot C_{i2} \cdot C_p}{C_{i1} \cdot C_{i2} + C_{i1} \cdot C_p + C_{i2} \cdot C_p} \qquad \textbf{Equation 3-14}$$

$$C_{on} = \frac{C_{i1} \cdot C_{i2}}{C_{i1} + C_{i2}} \qquad \textbf{Equation 3-15}$$

Solving the above equations for the phosphor capacitance, C_p, and the insulator capacitance, C_{i1} and C_{i2} (assuming that both insulator layers have the same thickness and thus equivalent capacitance), to give,

$$C_p = \frac{1}{\frac{1}{C_{off}} - \frac{1}{C_{on}}} \qquad \textbf{Equation 3-16}$$

$$C_{i1} = C_{i2} = 2 \times C_{on} \qquad \textbf{Equation 3-17}$$

From **Equation 3-13** and the above relationships, the slope for C_{on} can also be expressed as,

$$Q = C_{on} \cdot \left(V - V_{th,ph}\right) \qquad \textbf{Equation 3-18}$$

with $\left[V_{th,ph} = \frac{C_{on}}{C_{on} + C_p} \cdot V_{th} \right]$ where $V_{th,ph}$ is the threshold voltage for the phosphor layer, and can be obtained by extrapolating the slope of C_{on} towards the x-axis as shown in the Q-V curve of **Figure 3-7**.

In order to evaluate the device performance, the power dissipation and luminous efficiency of the mmLETFEL test device have to be determined. From **Figure 3-7**, the area encompassed by the Q-V curve gives the energy density of the mmLETFEL test device per cycle of the driving voltage, E_{in}, which is also known as the input power density per cycle.

$$E_{in} = 2 \times V_{th,ph} \times \Delta Q \qquad \textbf{Equation 3-19}$$

or $$E_{in} = 4 \times V_{th} \times Q' \qquad \textbf{Equation 3-20}$$

where Q' is the remaining charge density in the mmLETFEL test device after the drive voltage goes to zero, and ΔQ is the transferred charge.

Therefore, the input power density delivered to the mmLETFEL test device, hence the power dissipation of the mmLETFEL test device, is merely the product of the input energy density and the drive frequency.

$$P_{in} = f \times E_{in} \qquad \textbf{Equation 3-21}$$

Having determined the power consumption, the luminous efficiency (for a Lambertian emitter) is then given by the following equation,

$$\eta_{eff} = \pi \times \frac{L}{P_{in}} \qquad \textbf{Equation 3-22}$$

where L is the luminance in Cdm^{-2}, and P_{in} is the power consumption in Wm^{-2}.

Luminous efficiency increases just above the threshold voltage of the mmLETFEL test device, and has a maximum in the voltage region where the luminance is at its steep rise. Therefore, to evaluate the luminous efficiency, η_{eff}, it is desirable to obtain corresponding luminous efficiency at various voltages above the threshold voltage within this particular voltage region, which is usually a few tens of volts above the threshold voltage, depending on the sheer rise of the curve. However in this case, the luminous efficiencies of mmLETFEL test devices thus far have been evaluated at (V_{th}+50)V and at the peak drive voltage, V_{pk}=250V.

For example, at a voltage of $(V_{th}+V_m)$, where V_m=50V, the luminous efficiency becomes,

$$\eta_{eff(V_m)} = \pi \times \frac{L_{Vm}}{P_{in}} \qquad \textbf{Equation 3-23}$$

where L_{Vm1} is the corresponding luminance value at that drive voltage of $(V_{th}+V_{m1})$.

Based on the points discussed above, evaluations of the various mmLETFEL test device structures and configurations will be conducted. However, prior to these investigations, mmLETFEL test devices fabricated on Si will be evaluated for their dependence on varying drive conditions. This provides an indication that mmLETFEL test devices exhibit similar optical and electrical characteristics to that of a conventional ACTFEL device. This demonstration also forms the basis for the analysis of all the other mmLETFEL test device structures and configurations being subjected to the same drive conditions.

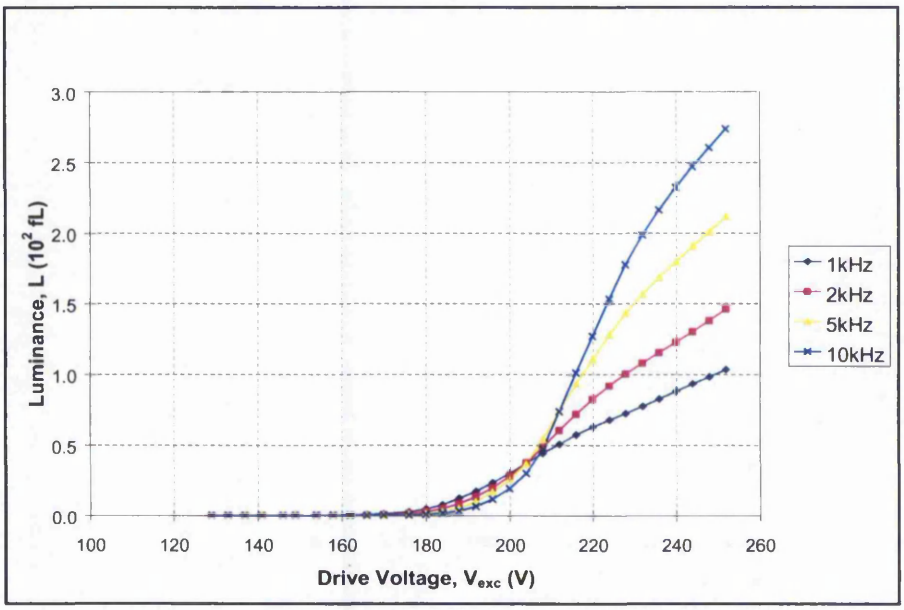
3.5.1. mmLETFEL test devices under different drive conditions

The following plots show the dependence of mmLETFEL test device luminance on the drive conditions such as drive waveform and drive frequency. **Plot 3-1** shows a mmLETFEL test device driven at 1, 2, 5 and 10kHz by a sinusoidal waveform, while **Plot 3-2** shows the same mmLETFEL test device being driven at the same frequencies but by a square wave instead. Both these plots are supplied from the same test device number (TDEV11) of wafer NTU356, from 2 different test cells. Similarly, other test devices, i.e. from TDEV12 to TDEV19, have also shown the same characteristics, measured from these same two test cells. Thus the L-V curves obtained can be representative of the behaviour of mmLETFEL devices under the same drive conditions.

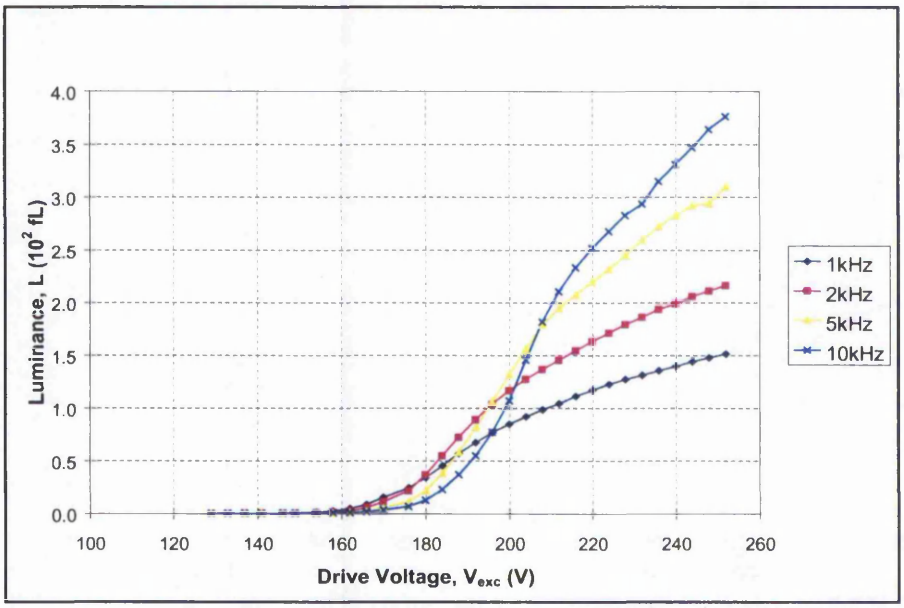
From these plots, it was evident that EL emission observed for mmLETFEL test device structures was strongly affected by the drive conditions applied. Increasing the frequency increased the luminance accordingly. The increase in the frequency effectively decreased the time for the EL emission decay and thus a larger output luminance was observed when the next opposite polarity pulse or wave arrived.

At the same time, the square drive waveform was observed to produce higher values in luminance as compared to when driven by the sinusoidal waveform. The sharp leading and falling edges that is characteristic of a pulse waveform effectively increased the rate of electron flow in the device once the device threshold voltage was reached. The additional in-phase current that flowed through the phosphor layer caused increased EL emission producing a larger output in luminance.

Both these observations were consistent with the physical mechanism of a conventional ACTFEL in that they demonstrated the typical electrical and polarisation characteristics expected.



Plot 3-1: mmLETFEL test device (TDEV11) driven by a sinusoidal waveform at 1, 2, 5, and 10kHz



Plot 3-2: mmLETFEL test device (TDEV11) driven by a square waveform at 1, 2, 5 and 10kHz

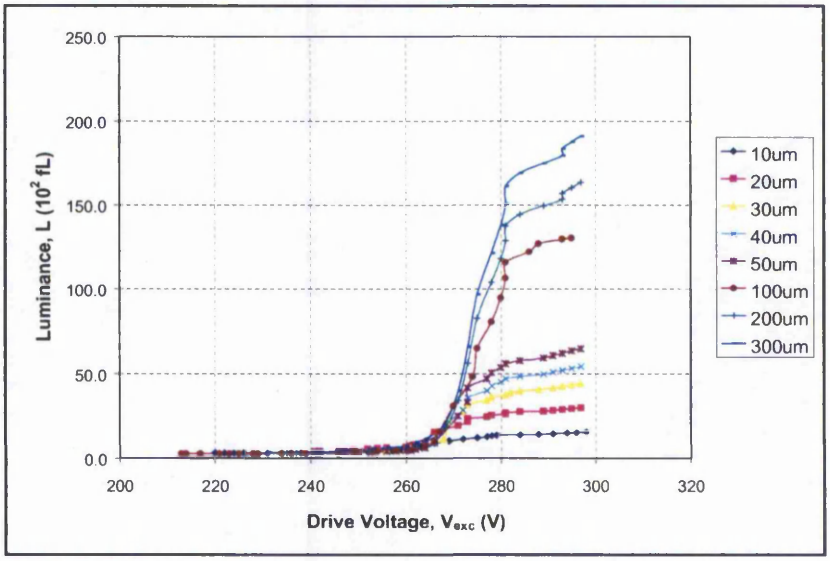
The following sub-section illustrates the comparison of characteristics of mmLETFEL test devices with different features e.g. test devices TDEV01-08 and TDEV11-19 by the L-V method, and TDEV20 by the Image Scan & Profile method.

3.5.2. mmLETFEL test devices with varying features

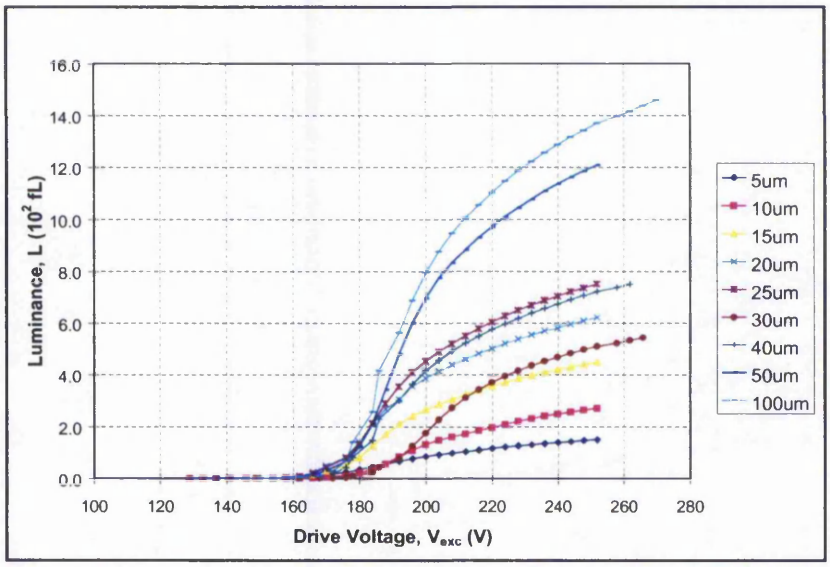
3.5.2.1 Active Material Lengths and Sidewall Widths

As lateral emission is the main EL emission contributor in the mmLETFEL technology due to the inherent waveguiding property of the device, it is obvious that the length of the mmLETFEL device is an important factor. As such, to fully utilise this useful emission occurring within the phosphor layer, an optimum length of the active material length has to be determined. However, although a larger output in EL emission is expected with increasing active material length, this phenomena is also limited by the attenuation of the propagating light within the mmLETFEL waveguide. Theoretical modelling of this attenuation factor versus the propagating length is being detailed in a concurrent investigation where the outcoupling mechanism of these mmLETFEL devices is also being detailed simultaneously.[63]

The following plots have been characterised from mmLETFEL test devices TDEV01-08 (NTU172) and TDEV11-19 (NTU356) deposited on Si (from 2 separate test cells on each wafer), driven by a square waveform at 5kHz. The characteristics shown have been consistent, in that an increase in active material length results in an increase in the overall luminance obtained, up to 300μm length of active material.

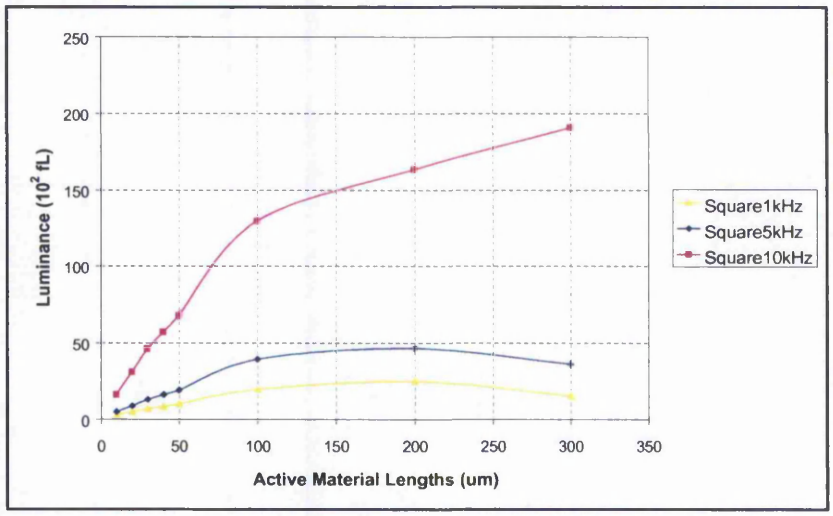


Plot 3-3: Comparative L-V characteristics of mmLETFEL test devices TDEV01-TDEV08



Plot 3-4: Comparative L-V characteristics of mmLETFEL test devices TDEV11-TDEV19

From **Plot 3-3** and **Plot 3-4**, it was demonstrated that as the active material length increased, there was a significant increase in the luminance observed. This is further illustrated by plotting the obtained luminance versus active material lengths at the peak drive voltage of +300V and at various drive frequencies. As the active material length increases, the luminance increases accordingly.



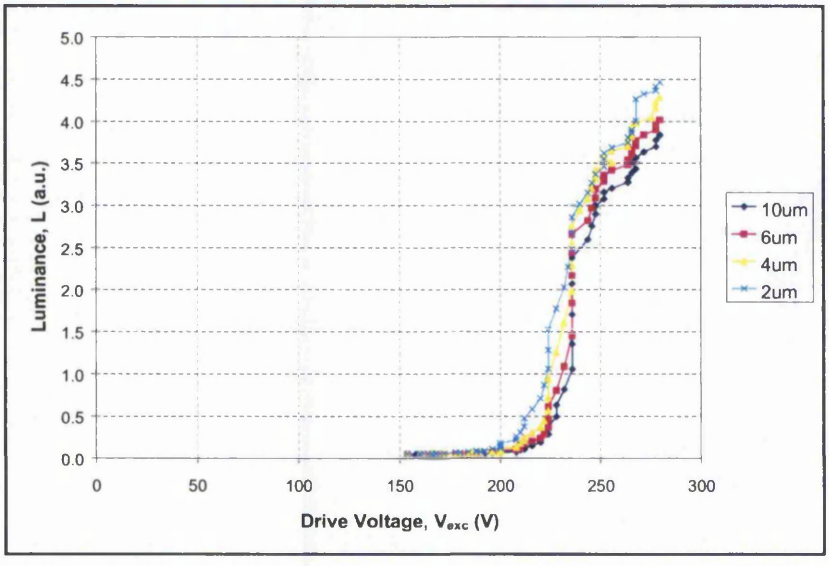
Plot 3-5: Luminance versus Active Material Lengths of mmLETFEL test devices

This indicates that the output efficiency is approaching its saturation point at active material lengths approaching 300μm. However, a new mask set consisting of test devices with increased lengths needs to be fabricated and investigated for the optimum active material length to be used.

For test devices L65 through to L80 (wafer NTU127) in **Plot 3-6** however, characterisation on devices with differing features of sidewall widths showed that as the sidewall width increases, the corresponding luminance also decreases. This could be that the effective active material volume decreases relatively. The difference in saturated luminance for test devices of 2μm as compared to 10μm was only of the order 1-1.5 a.u., indicating that there was no significant loss in the outcoupling of light when the sidewall was increased.

As such, sidewall width as small as 2μm can be utilised without affecting considerably the performance of the device in terms of overall luminance. However due to the fact that 2μm is considerably close to the process tolerance, and since there is no significant difference to the luminance between these devices, a sidewall width of 4μm is proposed instead.

Plot 3-6 shows a plot of these test devices (L73 to L76) measured from 3 separate test cells at 600d.p.i. It has been observed that this plot is representative of other test devices at other resolutions, i.e. 200d.p.i. (L65 to L68), 300d.p.i. (L69 to L72), and 1200d.p.i (L77 to L80).



Plot 3-6: Comparative L-V characteristics of mmLETFEL test devices L73-L76 (representation for differing sidewall widths at various resolutions)

3.5.2.2 *Aperture and Micro-Mirror Widths*

Figure 3-8 illustrates a mmLETFEL test device TDEV20 illuminating while under test on a wafer prober station. **Plot 3-7** shows the profile of the apertures across the mmLETFEL device by comparing the average relative intensities obtained for each of these apertures. There are 36 apertures in TDEV20, and every 3 apertures are of the same features, the details as tabulated in **Table 3-4**. The image capture of the test device TDEV20 (from 6 separate test cells) while driven at a specific drive condition (V_{exc}=±250V at 5kHz), is then evaluated using Scan and Profile method. By scanning several lines across one image, the relative intensities in grey scale levels are recorded and averaged. The mean average of the values obtained from the other images captured from these 6 different test cells is then calculated, and the result plotted as shown in **Plot 3-7**.

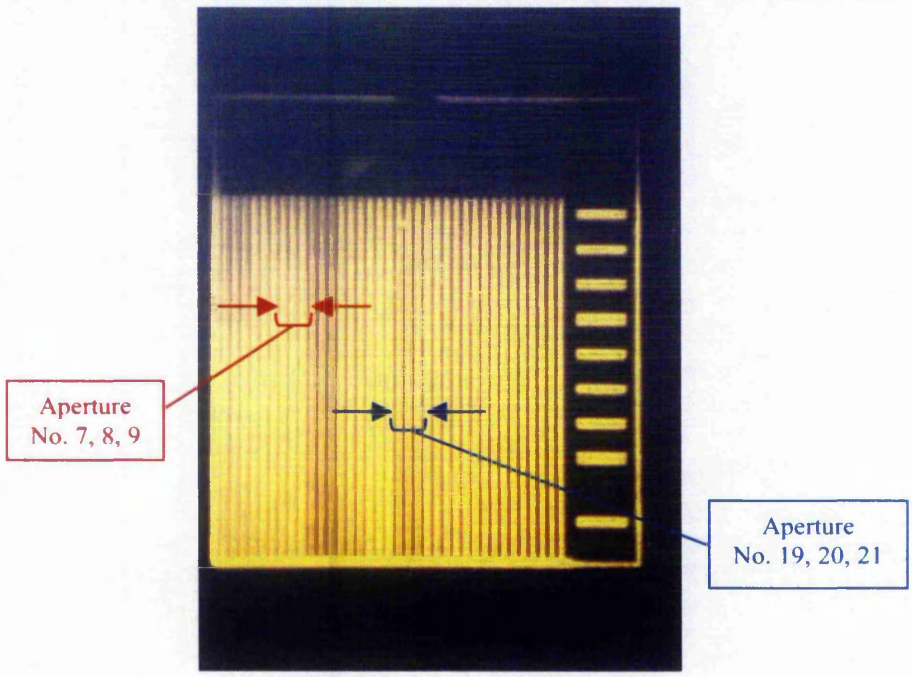
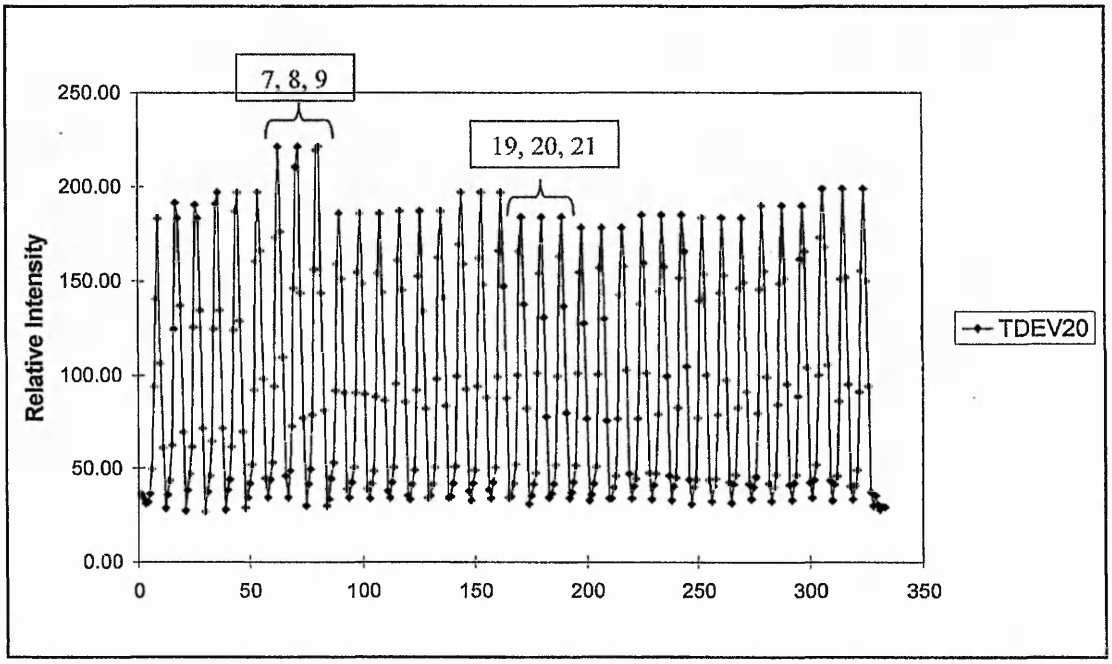


Figure 3-8: Image capture of mmLETFEL test device TDEV20 while under electrical probe

From the evaluation of this test device profile obtained, it can be concluded that greater luminance was produced at apertures where the emitting aperture width was larger than that of the micro-mirror width. This is due to the scattering and bending losses believed to occur at the emitting aperture where the light outcoupling is crucial. [63] If the aperture width was

the same or smaller than that of the micro-mirror, the propagating light would be reflected back internally into the device, and less would be emitted to the outside media. From the profile shown, it can be deduced that test devices with an aperture width of 4μm and a micro-mirror width of 3μm produce the largest output of EL emission, i.e. apertures nos. 7, 8, and 9.



Plot 3-7: Image profile of mmLETFEL test device TDEV20

These experimental observations made so far aid in the design of the mmLETFEL printer test device. The dimension determined thus far are for the active material length at 300μm; the sidewall width at 4μm; the aperture and micro-mirror widths at 4μm and 3μm respectively; and these can be incorporated into the device design. The relevant features mentioned are as shown in **Figure 3-9** of a typical mmLETFEL printer test device at 130dpi resolution.

At present, fabricated mmLETFEL printer test devices have an active material length of 250μm on either side feeding into the reflecting micro-structures, a micro-mirror and aperture widths of 3μm each, and a sidewall width of 10μm. Depending on the resolution of the devices, the number of dies and pixel pitch dimensions differ, as already illustrated in **Table 3-5**.

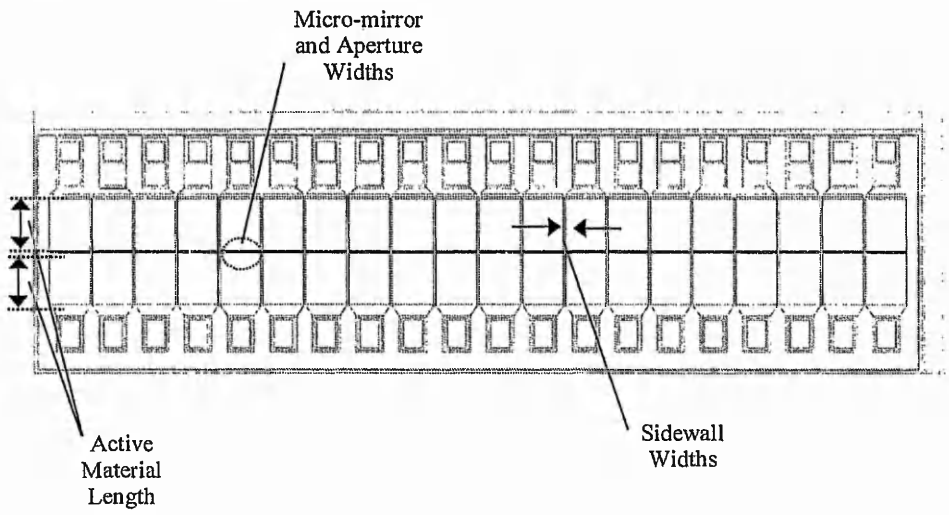


Figure 3-9: Illustration of the mmLETFEL printer test device and the relevant features

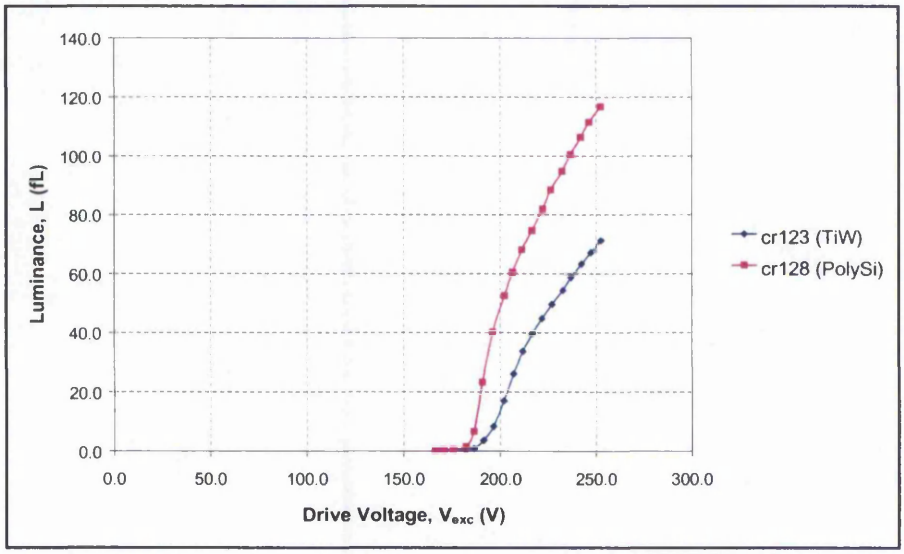
Having analysed the dependence of mmLETFEL test devices on the drive conditions and varying features applied, and hence determined the optimum features to be implemented, comparisons of the luminance and electrical properties are now made of mmLETFEL test devices fabricated with different base electrode and insulator materials. The device performance of each of these device configurations is evaluated under each sub-heading:

1. base electrodes of PolySi and TiW
2. insulators of Y_2O_3 and PECVD Si_3N_4

The drive conditions utilised for both the L-V and Q-V characterisation techniques were specified for a sinusoidal waveform at a frequency of 5kHz.

3.5.3 mmLETFEL test devices with different base electrodes

The comparison was made between the intensities obtained from mmLETFEL test devices fabricated on different base electrodes but with the same insulator material, i.e. Y_2O_3. In this case, the luminance values were measured of mmLETFEL test devices from the most recent wafers of CR123 and CR128. The L-V curve is shown in **Plot 3-8** for TDEV11 averaged from 15 and 13 separate test cells respectively for CR123 and CR128.



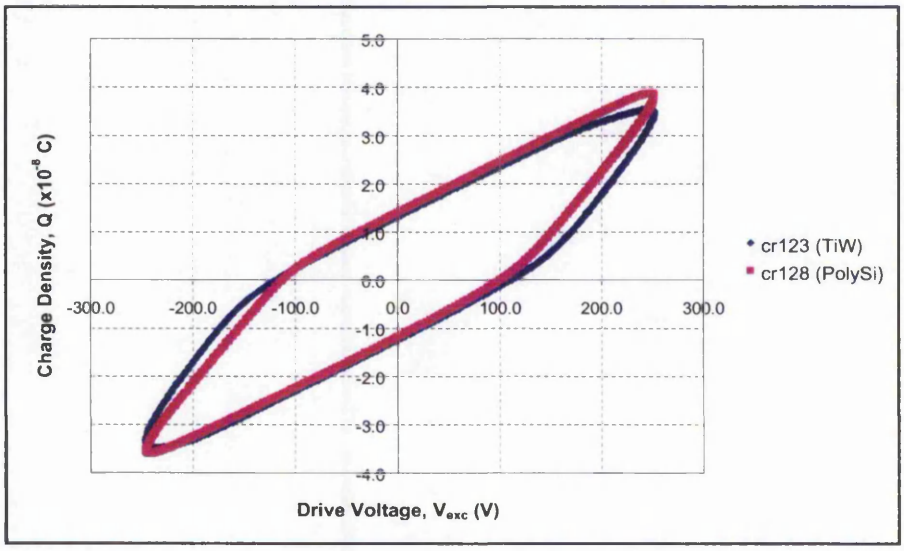
Plot 3-8: Comparative L-V characteristics of mmLETFEL TDEV11 grown with PolySi and TiW materials as base electrodes (Y2O3 as insulators)

The on-set threshold voltage observed for the mmLETFEL test devices grown on PolySi base electrode (CR128) was at V_{th}=182.3V, while the ones grown on TiW base electrode (CR123) was recorded at V_{th}=186.4V. The luminance obtained at 50V above the on-set threshold voltage and at the peak drive voltage, i.e. 250V, for each test wafer are tabulated in **Table 3-10**. The recorded sheet resistance for both the materials is also tabulated.

Base Electrode Material	Sheet Resistance (Ω/sq)	Threshold Voltage V_{th} (V)	Luminance at (V_{th}+50) V (fL)	Luminance at V_{pk}=250V (fL)
PolySi	15.72	182.3 ± 2.0	90.0 ± 9.0	118.4 ± 12.0
TiW	2.46	186.4 ± 2.0	55.3 ± 11.0	72.2 ± 14.0

Table 3-10: Luminance values of mmLETFEL TDEV11 grown with PolySi and TiW materials as base electrodes (Y2O3 as insulators)

Q-V characteristics of the same mmLETFEL test devices that were fabricated on PolySi and TiW base electrodes, i.e. mmLETFEL TDEV11 on CR123 and CR128 with insulator material of Y_2O_3 are shown in **Plot 3-9**.



Plot 3-9: Comparative Q-V characteristics of mmLETFEL TDEV11 grown with PolySi and TiW materials as base electrodes (Y2O3 as insulators)

The parameters as discussed and explained in the equations appended in the introduction to Section 3.5 relating to mmLETFEL electro-optical characteristics, such as the threshold voltage and its corresponding threshold charge density, the phosphor threshold voltage, and other parameters, were determined from the Q-V curve in **Plot 3-9**. The evaluation of mmLETFEL test devices performance from the aspects of transferred charge, power consumption and luminous efficiency were then calculated from these obtained parameters using **Equation 3-21** and **Equation 3-23**, and tabulated in the following **Table 3-11**.

Base Electrode Material	Transferred Charge ΔQ (10^{-8} F)	Power Dissipation P_{in} (mW/cm^2)	Luminous Efficiency at (V_{th}+50)V $\eta_{eff\,(50V)}$ (lm/W)	Luminous Efficiency at V_{pk}=250V $\eta_{eff\,(Vpk)}$ (lm/W)
PolySi	3.09	36	2.66	3.49
TiW	2.50	33	1.83	2.39

Table 3-11: Parameters calculated from Q-V characterisation of mmLETFEL TDEV11 grown with PolySi and TiW materials as base electrodes (Y2O3 as insulators)

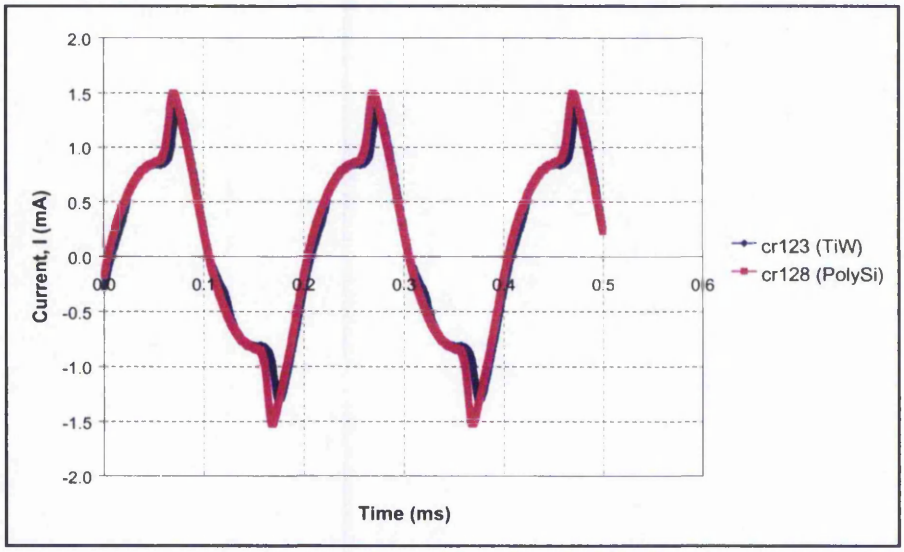
From both **Table 3-10** and **Table 3-11**, it was evident that mmLETFEL test devices fabricated on PolySi as the base electrode (CR128) exhibited greater luminance at a given drive voltage and frequency, which was found to be approximately 1½ times higher compared to that grown on TiW base electrode (CR123).

The increase in luminance affects the luminous efficiency since luminance is directly proportional to the luminous efficiency but is inversely proportional to the power consumption of the device as expressed in **Equation 3-23**. Consequently, the luminous efficiency obtained for mmLETFEL test devices grown on PolySi base electrodes (CR128) also exhibited close to a 1½-fold increase, since the power dissipation for both wafers were found to be similar.

This observed difference in luminance for these two wafers can be due to process-related factors, i.e. alignment of the mask-set during photolithography. Since both the micro-mirror and aperture widths at present have both been designed at 3μm, the alignment of the top electrode to the apertures prior to the etching process has to be as accurate as possible such that there is no significant effect to the light output efficiency at these emitting apertures.

Additional to the larger output of EL emission obtained, the corresponding threshold voltage obtained for mmLETFEL test devices grown on PolySi base electrodes (CR128) was found to be lower. However, this can be considered less significant since thickness of materials deposited may differ slightly from one wafer to another. At the same time the Q-V characteristics obtained for both wafers were also very similar. Thus it can be concluded that the deposition of these two base electrodes does not affect significantly the device performance for either test devices.

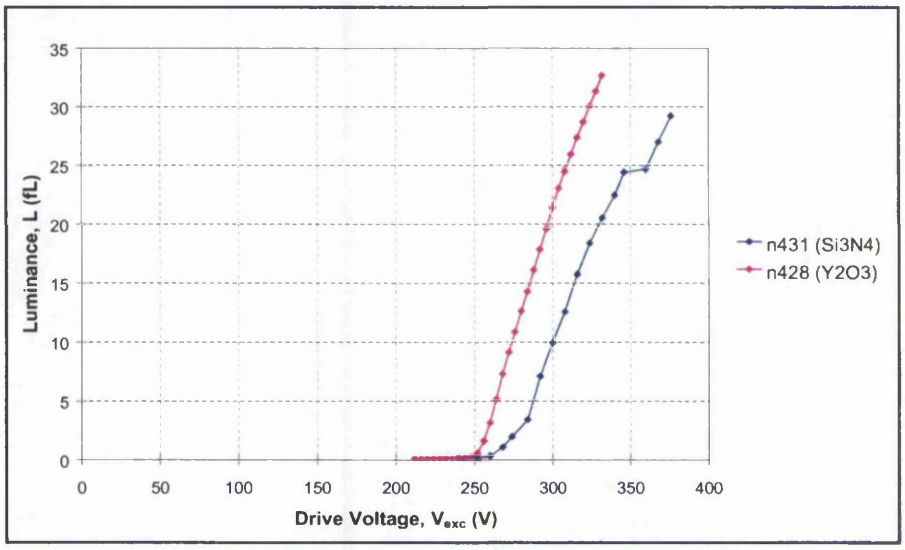
The I-V characteristics of **Plot 3-10** shows the current flow in the mmLETFEL test devices tested at the same drive condition. Consistent with the Q-V and L-V characteristics, the on-set of the current flow has started slightly earlier for mmLETFEL test devices grown on PolySi base electrodes (CR128) due to the earlier threshold voltage occurring at the start of the breakdown of the phosphor layer, i.e. $V_{th,ph}$. Since the rate of current flow is proportional to the rate of charge in time, thus at a given drive voltage, the comparatively higher charge density sustained in wafer CR128 after threshold (as shown in **Plot 3-9**) causes a comparatively higher current flow in these mmLETFEL test devices.



Plot 3-10: Comparative I-V characteristics of mmLETFEL TDEV11 grown with PolySi and TiW materials as base electrodes (Y2O3 as insulators)

3.5.4 mmLETFEL test devices with different insulators

A comparison between the different insulators fabricated on the same base electrode material was also analysed. In this case however, luminance values were obtained from mmLETFEL test devices fabricated on earlier wafers of NTU428 and NTU431 as the phosphor deposited for these wafers was the same. The L-V plot is shown in **Plot 3-11** for TDEV11 measured from test cell no 8 and test cell no 21 of the respective wafers.



Plot 3-11: Comparative L-V characteristics of mmLETFEL TDEV11 grown with Y2O3 and Si3N4 materials as insulators (TiW as base electrodes)

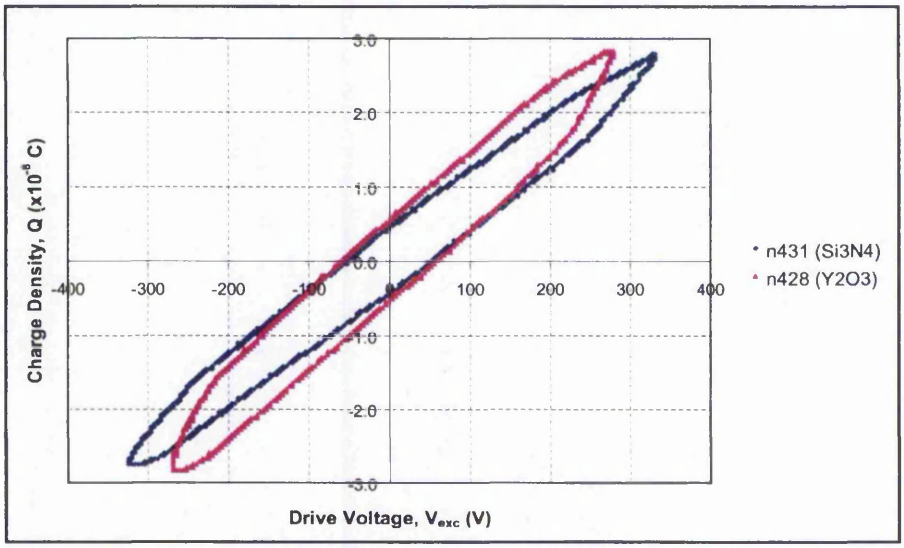
Although from the same batch using the same phosphor, wafer NTU429 did not work, thus comparison between wafers with different insulators, but on PolySi base electrode instead could not be analysed. Nevertheless, the important issue to be addressed here is the suitability of the insulator material. From the above plot, it is apparent that devices grown with Y_2O_3 as the insulators (NTU428) exhibit a much steeper L-V slope as compared to the same device feature but fabricated using PECVD Si_3N_4 insulator (NTU431) instead.

The on-set threshold voltage observed for mmLETFEL TDEV11 of wafer NTU428 was found to be at V_{th}=256V, while those grown on wafer NTU431 was observed at V_{th}=268V. The luminance values obtained at 50V above the on-set threshold voltage and at the peak drive voltage, i.e. 330V, for each test wafer are tabulated in **Table 3-12**. The measured dielectric constants of these two materials are also given.

Insulator Material	Dielectric Constant	Threshold Voltage V_{th} (V)	Luminance at (V_{th}+50) V (fL)	Luminance at V_{pk}=330V (fL)
Si_3N_4	6.8 ± 0.2	268.0 ± 2.0	15.8	24.4
Y_2O_3	11.9 ± 0.1	256.0 ± 2.0	23.0	32.7

Table 3-12: Luminance values of a mmLETFEL test device grown with Y2O3 and Si3N4 materials as insulators (TiW as base electrodes)

Q-V characteristics of the same mmLETFEL TDEV11 that were fabricated on TiW base electrodes but with different insulators, i.e. mmLETFEL test devices on wafers NTU428 and NTU431, is also shown in **Plot 3-12**.



Plot 3-12: Comparative Q-V characteristics of a mmLETFEL test device grown with Y2O3 and Si3N4 materials as insulators (TiW as base electrodes)

Similarly, the parameters such as the threshold voltage, the threshold charge density, the phosphor threshold voltage, etc. were found from the Q-V curve in **Plot 3-12**. The mmLETFEL test devices performance from the aspects of transferred charge, power consumption and luminous efficiency were then calculated from these obtained parameters and tabulated in the following **Table 3-13**.

Insulator Material	Transferred Charge ΔQ (10^{-8} F)	Power Dissipation P_{in} (mW/cm^2)	Luminous Efficiency at (V_{th}+50)V $\eta_{eff\,(50V)}$ (lm/W)	Luminous Efficiency at V_{pk}=330V $\eta_{eff\,(80V)}$ (lm/W)
Si_3N_4	1.46	13.6	1.01	1.57
Y_2O_3	1.10	13.4	1.50	2.13

Table 3-13: Parameters calculated from Q-V characterisation of a mmLETFEL test device grown with Y2O3 and Si3N4 materials as insulators (TiW as base electrodes)

From **Table 3-12**, the luminance obtained for mmLETFEL test devices grown with Y_2O_3 (NTU428) as the insulators exhibited greater luminance value at a given drive voltage, which was about 1½ times greater than those grown with Si_3N_4 as insulators (NTU431). Since the same material was used as the base electrode, any errors determined in the existing capacitance and/or resistance pertaining to this base electrode can be neglected. Thus one factor that prevailed was the use of different insulator materials for both wafers, thus indicating a difference in terms of device performance.

This can be due to a number of reasons such as the dielectric constant, and the reliability of the material in its ability to insulate the phosphor material from breaking down after device turn-on, as well as the nature of the interface between the phosphor and dielectric layers. The relationship between the dielectric constant and the dielectric breakdown strength in evaluating device performance in terms of the insulator materials used can be explained by the following equations.

Below threshold, the mmLETFEL device behaves as an ideal capacitor, and Maxwell's equations impose the following boundary conditions at the interface between the individual film layers to be,

$$\varepsilon_o \varepsilon_i E_i = \varepsilon_o \varepsilon_p E_p \qquad \textbf{Equation 3-24}$$

where ε_o, ε_i and ε_p are the relative dielectric constant of vacuum, the insulating layer, and the phosphor layer, respectively; and E_i and E_p, the electric field of the insulating layer and phosphor layer, respectively.

Since the peak applied voltage, V_{pk}, is the sum total of voltages across the insulating and phosphor layers, thus these voltages can be related in the following,

$$V_{pk} = E_i d_i + E_p d_p \qquad \textbf{Equation 3-25}$$

where d_i and d_p are the thicknesses of the insulating layer and phosphor layer, respectively.

Using **Equation 3-24** and **Equation 3-25**, the voltage which is applied across the phosphor layer, V_p, can then be calculated to be,

$$V_p = E_p d_p = \frac{\varepsilon_i d_p}{\varepsilon_i d_p + \varepsilon_p d_i} \times V_{pk} \qquad \textbf{Equation 3-26}$$

Thus, in order to maximise the voltage applied across the phosphor layer so as to maximise the EL output emission, the dielectric constant of the insulating layer, ε_i, has to be as large as possible, while its thickness, d_i, be as small as device reliability would allow. A large ε_i, or a small d_i, leads to a proportionally smaller voltage appearing across the insulating layer as expressed in **Equation 3-25**, hence resulting in a lower device operating voltage.

For this case, since both Y_2O_3 and Si_3N_4 have been grown with the same thickness, the difference lies in the dielectric constant of these materials. As tabulated in **Table 3-12** and **Table 3-13**, mmLETFEL test devices grown with Y_2O_3 insulators (NTU428) have a comparatively higher dielectric constant. Thus at a given drive voltage, the effective voltage applied across the Y_2O_3 insulator layer is lower compared to the Si_3N_4 insulator layer, resulting in a larger voltage applied across the phosphor layer for the mmLETFEL test devices of wafer NTU428 (with Y_2O_3 insulators).

Due to this higher resultant voltage appearing across the phosphor layer, these test devices utilising Y_2O_3 insulators (NTU428) experienced an earlier occurrence in the conduction of the phosphor layer. Hence a lower device threshold voltage is observed for these devices compared to those grown with Si_3N_4 insulators (NTU431). Consequently at a given applied

drive voltage to both types of test devices, the luminance obtained for these Y_2O_3 test devices (NTU428) is comparatively higher, thus a higher luminous efficiency is achieved. By manipulating **Equation 3-24**, the electric field for an insulating layer can be found as,

$$E_i = \frac{\varepsilon_p E_p}{\varepsilon_i} = \frac{8.3 \times 1.5 \times 10^{-8}}{\varepsilon_i} \qquad \textbf{Equation 3-27}$$

where ε_p=*8.3*, and E_p=*1.5x10*$^{-8}$ V/m; substituting typical values for ZnS:Mn phosphor used.

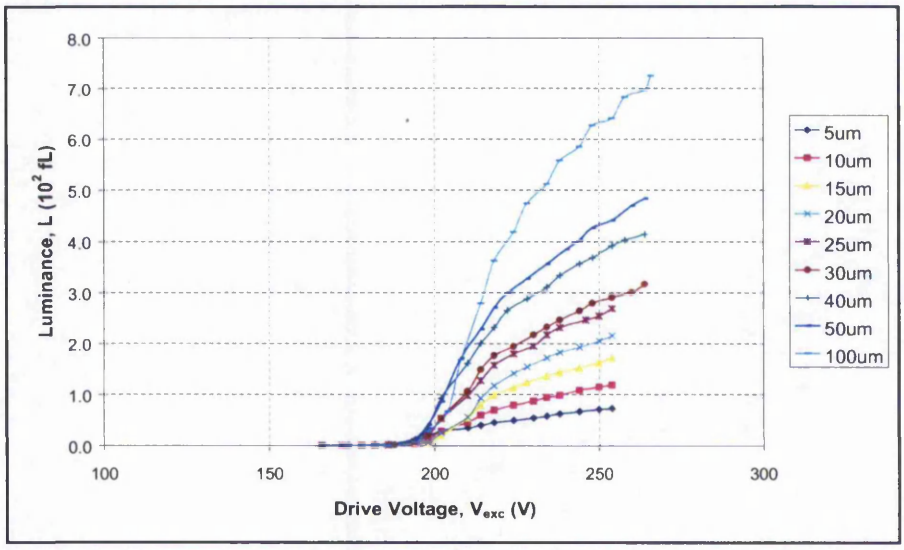
Here, it further demonstrated that a large ε_i has the advantage of producing more reliable devices due to the lower electric field that was needed to be sustained by the insulator during operation. Comparing just the insulator materials used in this investigation, it was clear that Y_2O_3 had greater advantages over PECVD Si_3N_4, in terms of dielectric constant and dielectric strength characteristics. In addition, the power consumption was found to be almost similar, i.e. 1.34W/cm^2 for devices with Y_2O_3 insulators and 1.36W/cm^2 for devices with Si_3N_4 insulators, thus affirming the superiority of Y_2O_3 over Si_3N_4 for use as insulator material in mmLETFEL devices.

3.5.5 Reproducibility of mmLETFEL test devices in terms of luminance

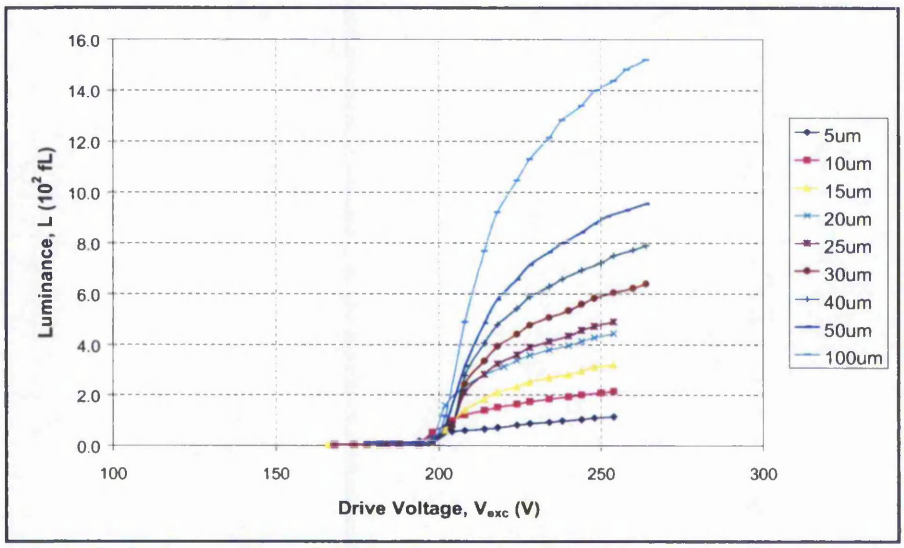
Reproducibility of mmLETFEL devices is a crucial factor since reproduction of devices exhibiting similar characteristics is greatly desired. In this case, wafers CR123 (with TiW base electrode) and CR128 (with PolySi base electrode) have been used for the purpose of this comparison since these wafers are the most recent. They have been grown within the time period of a week, using the same phosphor material, and the same deposition chamber.

Here, three methods have been proposed from which to observe the reproducibility of mmLETFEL devices in terms of measured luminance. All measurements have been taken from 15 test cells of wafer CR123, and 13 test cells of wafer CR128.

The first instance is to ascertain whether the mmLETFEL test devices from TDEV11 to TDEV19 still demonstrate similar increases in luminance values as already been shown in Plot 3-4 in Section 3.5.2.1. The following **Plot 3-13** and **Plot 3-14** show the L-V characteristics of mmLETFEL TDEV11 to TDEV19, demonstrating that the luminance value

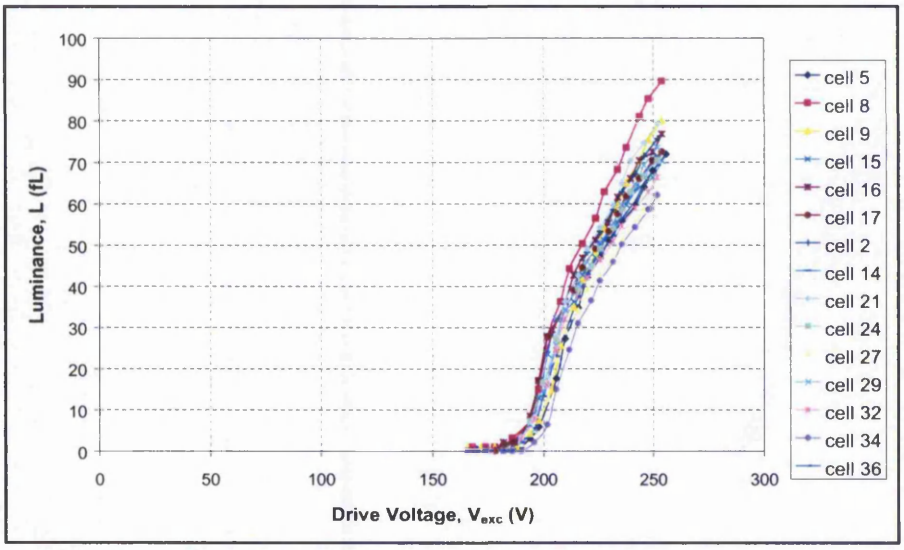


Plot 3-13: Comparative L-V characteristics of mmLETFEL test devices TDEV11-TDEV19 for wafer CR123 (Y2O3 as insulators and TiW as base electrodes)

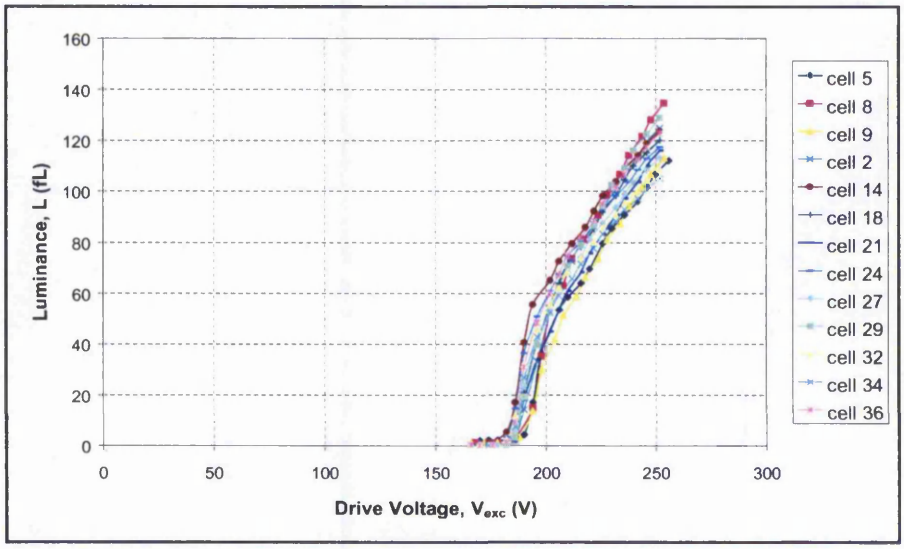


Plot 3-14: Comparative L-V characteristics of mmLETFEL test devices TDEV11-TDEV19 for wafer CR128 (Y2O3 as insulators and PolySi as base electrodes)

The second method is to observe the range of L-V curves for the same mmLETFEL test device, but measured at various positions across the entire wafer. Luminance measurements have been taken for mmLETFEL TDEV11 for both wafers CR123 and CR128 from the centre to the edges of the wafers.



Plot 3-15: Range of L-V curves for mmLETFEL TDEV11 across wafer CR123 (Y2O3 as insulators and TiW as base electrodes)



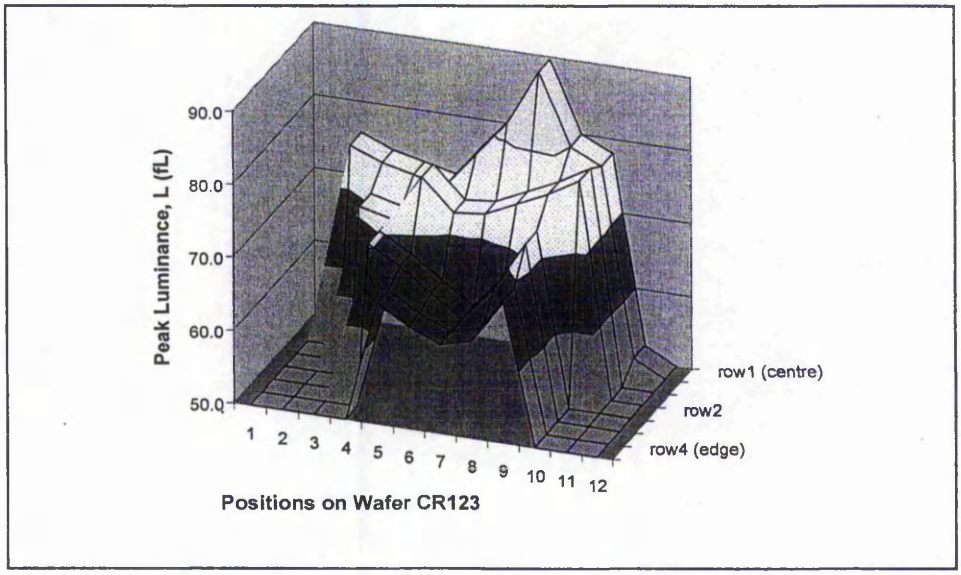
Plot 3-16: Range of L-V curves for mmLETFEL TDEV11 across wafer CR128 (Y2O3 as insulators and PolySi as base electrodes)

Plot 3-15 and **Plot 3-16** show the range of L-V curves obtained for TDEV11 demonstrating that the majority of the L-V curves between the two extremities of the lowest and highest peak luminances, i.e. at $V_{pk}=250V$, to fall within a range of ±14fL and ±12fL for wafers CR123 and CR128 respectively. However, at a drive voltage of $V_{exc}=(V_{th}+V_{ml})$ where $V_{ml}=50V$, the range of experimental error now falls to within ±11fL for CR123 and ±9fL for

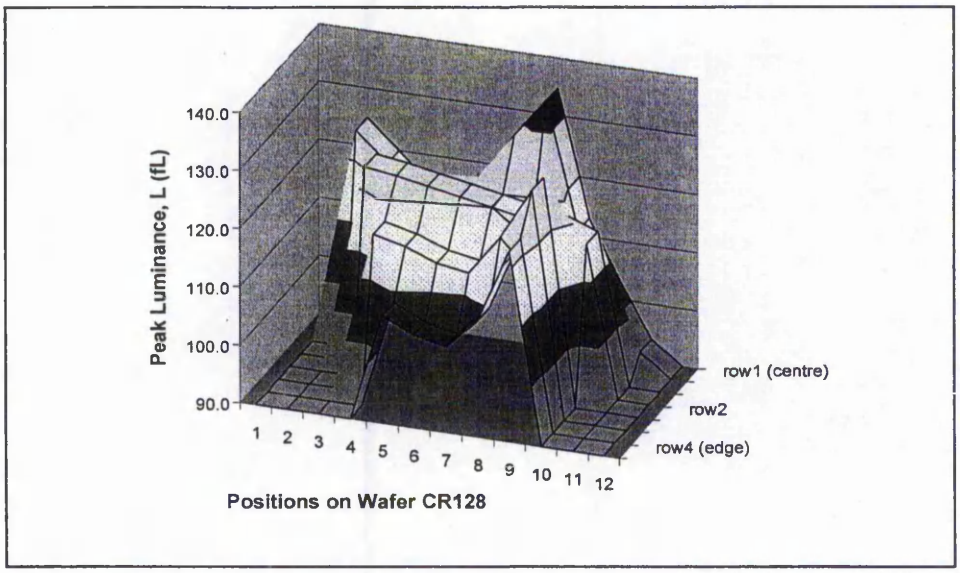
CR123 and CR128 respectively. However, at a drive voltage of $V_{exc}=(V_{th}+V_{ml})$ where $V_{ml}=50V$, the range of experimental error now falls to within ±11fL for CR123 and ±9fL for CR128. Since the mean deviation for these two curves falls within the same range, it can be deduced that the mean average can be measured from these curves and be used to represent the L-V characteristic of a typical mmLETFEL device (as previously shown in plots in Section 3.5.3 and Section 3.5.4).

However, to view it from a clearer perspective, the distribution of these L-V curves in terms of the peak luminances of these mmLETFEL test devices against their allocated positions across the entire wafer can be found and observed. In this manner, it can be shown where the highest and lowest peak luminance is expected, and how the reproducibility is mirrored in this case.

The uniformity of mmLETFEL test devices can be indicated by comparing the distribution of the peak luminance of mmLETFEL test devices against their positions located across one wafer (CR123) to the distribution found for the same test devices across another wafer (CR128). **Plot 3-17** and **Plot 3-18** below plot the peak luminance distribution across these wafers, where row 1 and row 4 indicates the centre and the edge of the wafer respectively. Similarly, along the x-axis, the centre position of the wafer is indicated by column no. 5, while the edges of the wafer are indicated by the nos. 1 and 12.



Plot 3-17: Distribution of peak luminance for mmLETFEL TDEV11 across wafer CR123 (Y2O3 as insulators and TiW as base electrodes)



Plot 3-18: Distribution of peak luminance for mmLETFEL TDEV11 across wafer CR128 (Y2O3 as insulators and PolySi as base electrodes)

Thus, both plots have shown that the distribution for both wafers in terms of the obtained peak luminance has a distributed peak at the centre of the wafers. The obtained peak luminance values then decreases as it approaches towards the edges of the wafers. In both cases, the highest peak luminance has been found for test cell no. 8.

From these 3 methods proposed and the results obtained, it can be concluded that the reproducibility of mmLETFEL devices thus far have been reliable. The L-V characteristics obtained have been expected of those of TDEV11 to TDEV19. At the same time, the tolerance range in which the L-V curves have been found for test cells across an entire wafer as compared to another has a difference of only ±2fL in the measured mean deviation at the peak drive voltage for both wafers. Confirmation of the reproducibility capability of the mmLETFEL technology was shown in the last instance where the peak luminance distribution across one wafer as compared to another was similar; in that the highest and lowest peak luminance values have been obtained for the same test cells for both wafers.

3.6 CONCLUSION

Luminance measurements are obtained of mmLETFEL test devices TDEV01-TDEV08, TDEV11-TDEV19, and L65-L80, fabricated on plain Si wafer, without the base electrodes deposited. The compared results aid in the modification of an improved design layout for the mmLETFEL printer test device. As such, the optimum device dimension have been determined for:

1. the sidewall width at 4μm
2. the aperture width at 4μm
3. the micro-mirror width at 3μm

As the active material length increases and approaches 300μm, the corresponding luminance has been found to increase accordingly. Thus, it is proposed that a new mask design incorporating test devices with greater active material lengths to be fabricated and characterised for determination of the optimum active material length to be used.

Following this, results are obtained for the characteristics of the four different mmLETFEL configurations, i.e. with Y_2O_3 and PECVD Si_3N_4 as insulators, and PolySi and TiW as base electrodes. The device characteristics are dependent on factors such as fabrication and processing techniques, thus these obtained values are only representative by way of comparison. Deposition of both PolySi and TiW as base electrodes has been successful and demonstrated their suitability for fabrication with the mmLETFEL test devices.

Measured results of mmLETFEL test devices fabricated with TiW and PolySi base electrodes have been comparable in that the threshold voltage, power consumption and transferred charge have been found to be similar. The slight increase in luminance and luminous efficiency for the former test devices, as well as the slightly lesser spread of the luminance range found (a difference of ±2fL between these two test wafers) suggests that PolySi would be the more suitable material.

The comparative characteristics of mmLETFEL test devices utilising the sputtered Y_2O_3 as insulators can be summarised as having the following advantages:

1. lower device threshold voltage
2. higher luminance
3. better device performance from the aspects of:
   (a) greater luminous efficiency
   (b) higher dielectric constant
   (c) lower operating voltage or electric field across the dielectric layer

Therefore, the recorded observations and evaluations for the optimum mmLETFEL structure to be fabricated for the integration exercise would be test devices utilising the Y_2O_3 material as insulators, and the PolySi material as base electrodes that has demonstrated its compatibility with the mmLETFEL technology.

In addition, it has been shown that the mmLETFEL test devices TDEV11 to TDEV19 grown on TiW and PolySi base electrodes have exhibited similar characteristics as expected to those grown on Si wafer without base electrodes. This indicates that the deposition of the base electrodes prior to the growth of mmLETEL test devices have no significant effect on the L-V characteristics expected for a mmLETFEL test device.

Further, the uniformity of L-V curves of test device TDEV11 across recent wafers, i.e. wafers CR123 and CR128, have demonstrated that the obtained peak luminance values at its peak drive voltage fall within the deviation range of ±14fL and ±12fL between the lowest and highest obtained peak luminance.

Lastly, the mmLETFEL technology has proven its reproducibility capability in the observation of the obtained peak luminance of mmLETFEL test devices being distributed across the entire wafer and comparing the aforementioned distribution to that of another wafer. The highest peak luminance value was found for the same test cell, i.e. test cell no. 8.

Contents

4 Characterisation and SPICE Modelling of High-Voltage MOSFETs

4 CHARACTERISATION AND SPICE MODELLING OF HIGH-VOLTAGE MOSFETS

4.1 INTRODUCTION

In order to assess the feasibility of integrating the mmLETFEL device with a high-voltage driver, an investigation into various aspects for such an integration exercise is required. Therefore, prior to the actual development of the OEIC, the following are taken into account for the feasibility investigation (the listed first two have been covered in Chapters 2 and 3):

1. Fabrication of mmLETFEL test devices using different base electrode materials and insulator materials
2. Characterisation of mmLETFEL test devices using different base electrode materials and insulator materials
3. Characterisation of fabricated test die of commercially available high-voltage drivers
4. Simulation and optimisation of the high-voltage driver SPICE model
5. Development of the individual mmLETFEL SPICE model and eventually the integrated OEIC SPICE model

In this chapter, an investigation into various commercial electronic high-voltage drivers from several manufacturers that is suitable for addressing mmLETFEL devices is conducted by performing SPICE modelling using their developed SPICE models and model parameters. The selection of a suitable driver is also explained, and this selection has been based on several factors. Device availability, technology accessibility, information exchange, and cost, are among the many factors taken into account.

Further, electrical characterisation and SPICE modelling of the selected commercial driver are detailed. A comparison between the experimental results and simulated characteristics is shown and analysed. Optimisation of the SPICE model is performed to achieve a refined model of the high-voltage driver for use in further simulation exercises involving the integrated mmLETFEL device pixel (which will be detailed in the next chapter).

4.2 HISTORY OF SPICE

SPICE is an abbreviation for "Simulation Program with Integrated Circuit Emphasis".[104, 105, 106, 107, 108] The SPICE program is essential to the design engineer as the circuit simulation obtained not only provides an understanding of the device physics, but is also used to predict the performance and extract model parameters of these devices. In this way cell improvement and circuit optimisation can be achieved prior to the device fabrication.

SPICE's capabilities include:

1. Non-linear D.C. analysis (D.C. operating point)
2. Linear small-signal analysis (frequency response)
3. Transient analysis (time response)
4. Small-signal D.C. transfer function analysis (from specified input to specified output)
5. D.C. small-signal sensitivity analysis (specified output variables with respect to every parameter)
6. Distortion analysis with A.C. analysis
7. Noise analysis with A.C. analysis
8. Fourier analysis (of an output variable)
9. Temperature analysis

SPICE was developed by the "Integrated Circuit Group" of Electronics Research Laboratory, and Dept of Electrical Engineering & Computer Science, at University of California, Berkeley in the late 60's. Although the original developer was Dr. Lawrence Nagel, Prof. D. O. Pederson was better known as the "father" of SPICE. SPICE2, also referred to as SPICE, is the industry standard written in the FORTRAN language, and was released to the public in 1972. SPICE3, a newer and redesigned implementation version of SPICE2, was converted to the C language for easier portability. PSPICE, an IBM-PC based program (by MicroSim Corporation), which is developed at the same University in the mid-70's, is derived from SPICE2 to fit into U.C. Berkeley CAD research program.

From here, other commercially supported versions of these two standards have emerged and all of which have options to extend simulation capabilities and interpret results. These include:

1. Original group of mainframe-based versions:
   a. HSPICE (by Meta-Software) - focuses on I.C. design with device model support.
   b. I-SPICE (by NCSS timesharing) - focuses on "interactive" circuit simulation and graphics output.
2. IBM-PC based programs (other than PSPICE):
   IS-SPICE (by Intusoft) - direct adaptations of SPICE2 or SPICE3, with additions including pre-processors or shell programs, to manage the input and provide interactive control, and post-processors for refining the output.
3. Advanced programs with "innards" which uses the same direct-method simulation algorithms as U.C. Berkeley SPICE:
   a. AccuSIM (by Mentor Graphics)
   b. PSPICE (by MicroSim Corporation)
   c. Spectre (by Cadence Design)
   d. ViewSpice (by ViewLogic Systems)

In this investigation, SmartSpice (a circuit simulator created within a software package, Virtual Wafer Fabrication (VWF) manufatured by Silvaco International), was used for modelling the mmLETFEL test devices and the high-voltage MOSFET devices. The circuit modelling performed can aid in the device and process modelling whose simulators are both incorporated within the software package itself. Thus, theoretical simulations of a device on all levels can be conducted and its characteristics analysed prior to device fabrication.

4.3 SPICE MODELS OF COMMERCIAL DRIVERS

Due to the requirement of switching 'ON' and 'OFF' the mmLETFEL device, the corresponding driver has to be able to withstand a high potential across its drain-source channel. In other words, a driver that can function as a high-voltage switch. Referring to **Figure 4-1**, where the mmLETFEL and high-voltage driver are shown in simplified block diagrams, the a.c. excitation voltage, V_{exc}, is dropped across both the n-channel high-voltage driver and mmLETFEL device, i.e. V_{diff} and V_{letfel}, respectively.

When a positive voltage is supplied to the gate of the high-voltage n-channel MOSFET, it behaves as a 'closed' switch, effectively grounds the base electrode of the mmLETFEL device, thus resulting in all of the excitation voltage to drop across the mmLETFEL device, i.e. $V_{letfel}=V_{exc(pk\text{-}pk)}$. The mmLETFEL device is said to switch 'ON' since the threshold voltage has been reached (on both polarities) causing EL emission to occur. This EL emission is the light source energy that is needed to discharge a photoconductively charged drum of a printer.

On the other hand, when 0V is applied to the gate of the MOSFET, the device behaves as an 'open' switch and effectively blocks the a.c. high voltage with a certain required modulation voltage. The MOSFET internal drain-source capacitance thus creates a capacitive network with the mmLETFEL total capacitance, resulting in the voltage drop across the mmLETFEL device to be $V_{letfel}=V_{exc(pk\text{-}pk)}-V_{diff}$. Depending on the high-voltage driver used, i.e. the drain-source voltage specified, V_{diff} may differ causing the resultant voltage V_{letfel} to differ accordingly. Ideally V_{diff} should only be the required voltage to be blocked such that the mmLETFEL cell changes from an 'ON' to an 'OFF' state, ensuring that the luminance, L_{diff}, obtained between these states are at zero emission and the corresponding value at the peak drive voltage respectively. In other words, the voltage drop across the mmLETFEL device should ideally be less than the peak-to-peak threshold voltage of the mmLETFEL device, i.e. $V_{exc(pk\text{-}pk)}-V_{diff}<V_{th(pk\text{-}pk)}$. This is because during turn-off, the light source energy should not be able to discharge a photoconductively charged drum of a printer. However, this is also dependent on the L-V characteristics of the mmLETFEL device obtained. Ideally the L-V curve should be as steep as possible, thus allowing for V_{diff} to fall between the two extremities of 0fL (before device threshold) and its saturation luminance value (after device threshold). **Figure 4-1** illustrates the 'ON' and 'OFF' state conditions

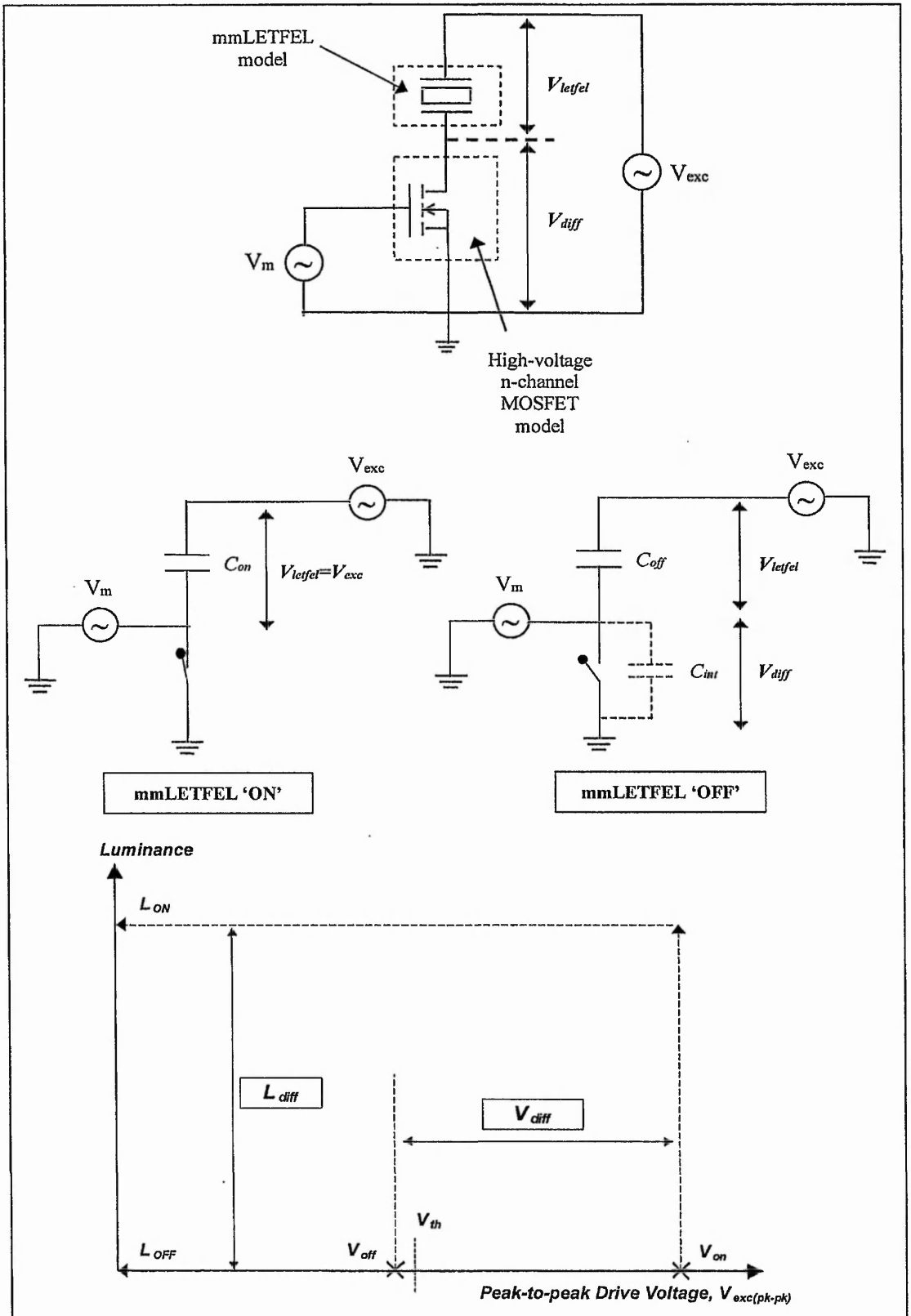


Figure 4-1: Illustration of the functionality of a high-voltage driver to switch the mmLETFEL device'ON' and 'OFF'

Several commercial fabrication houses that manufacture high-voltage MOSFET devices have been investigated. These include:

1. 50V process from HOLTEK, Taiwan [109] (Appendix C1)
2. 28V process from UMC, Taiwan [109] (Appendix C1)
3. 300V process from Supertex, USA [110] (Appendix C1)
4. 100V process from Alcatel Mietec, Belgium [111] (Appendix C3)

(Note that the voltage stated for each process refers to the maximum safe breakdown voltage of the devices).

Tables listing the SPICE model parameters obtained from these manufacturers are presented in Appendix C1 and Appendix C3, as specified above. Appendix C2 lists the model parameters corresponding to the SmartSpice n-channel MOSFET model Level=3 which selects the semi-empirical model, thus requiring some parameters to be obtained by optimisation. It is also the most reliable and most commonly used model.

As for the Alcatel Mietec driver, the model parameters, their descriptions, and default values are tabulated in Appendix C3. In this case, the SmartSpice n-channel MOSFET model Level=2 is used for the principal transistor which is suitable for modelling bulk charge effects on the drain current, i_{ds}. While the drain resistance is modelled using the SmartSpice MOSFET model Level=1. As such, the typical NDMOSHV model as suggested by Alcatel Mietec is a macro-model consisting of these two transistors in series.

During this particular investigation, many problems were encountered. Among the major obstacles faced was lack of expertise in the area of SPICE modelling of high-voltage MOSFET devices; break-down of communication with various fabrication houses regarding the provision of technology, test devices and SPICE model parameters; and the cost involved in the information and technology exchange in such cases.

The first SPICE model parameters obtained for a high-voltage MOSFET driver were from HOLTEK in Taiwan. However, the model parameters were represented in H-SPICE, and the interpretations of these parameters were significantly different to the general SPICE3 version. Although the driver chips were supplied, i.e. HT1606 and HT1607 - both of 50V process - there was insufficient documentation to enable further SPICE modelling, As such, the investigation into these devices was impaired and discontinued.

Next, communication with UMC in Taiwan was successful in obtaining the SPICE3 version of their n-channel 28V process MOSFET device model parameters. Documentation supporting this proposed nMOS device was also easily available. However, their assistance in providing the necessary test die was not gained. Therefore, this route was not further examined and the investigation had to be terminated.

This led to yet another embarkation for the search for other suitable high-voltage MOSFET drivers. Contact with Supertex in the U.S.A. opened up the possibility of accessing their 300V process MOSFET technology. The very high voltage involved was suitable to drive the mmLETFEL devices in that, by switching the driver on, it allows for the full swing of the excitation voltage, V_{exc}, to be applied across the mmLETFEL device, thus rendering the device to be switched fully 'ON'. And vice versa, by switching off the driver, only a minimal amount of voltage is applied across the mmLETFEL device, i.e. (V_{exc}-300V), thus rendering the device to be switched fully 'OFF'. This was ideal as it solved the issue of maintaining a steep rise of the L-V curve of a mmLETFEL device in order to achieve an optimum modulation voltage, and also the working region, in which to operate the device in.

However, documentation that can be obtained supporting this particular process was insufficient. At the same time, the cost of obtaining test dies from Supertex was too high, and this was the main deterrent in the continuation of this investigation. Since the purpose of this investigation is to prove the feasibility of integrating a mmLETFEL with its corresponding individual driver, it is anticipated that costs from Supertex may become more reasonable when the results of this work are presented.

Finally, EuroPractice [112] paved a way for contact with Alcatel Mietec in Belgium. Discussion with the experts proposed a 100V n-channel MOS device which would be able to act as a single switching element for an individual mmLETFEL pixel. SPICE model parameters, together with full documentation of this particular device (NDMOSHV model), were obtained. Simulations of the proposed NDMOSHV model were conducted, and communication via EuroPractice verified the simulated plots obtained.

Further, twenty test die were received from Alcatel Mietec via EuroPractice to enable electrical characterisation to commence, and comparison and analysis of the measured characteristics to the simulated NDMOSHV model. Although the test drivers had only one variation, i.e. only devices with drain width, w_d=40μm, were fabricated and available for use, optimisation of the NDMOSHV model was nevertheless pursued. The optimised NDMOSHV model based on the test drivers supplied was then utilised for subsequent simulations of the OEIC pixel.

The following sections detail the electrical characterisation and SPICE modelling of the Alcatel Mietec 100V NDMOSHV devices.

4.4 Electrical Characterisation of Alcatel NDMOSHV Test Devices

The test devices obtained from Alcatel Mietec, Belgium, via EuroPractice, were attached and wire-bonded[113] onto individual chip carriers for electrical measurements to commence. **Figure 4-2** and **Figure 4-3** respectively show the Alcatel driver die before and after wire-bonded onto chip carrier – the wire-bonded pad numbers of the die and its corresponding chip carrier pin numbers are also tabulated.

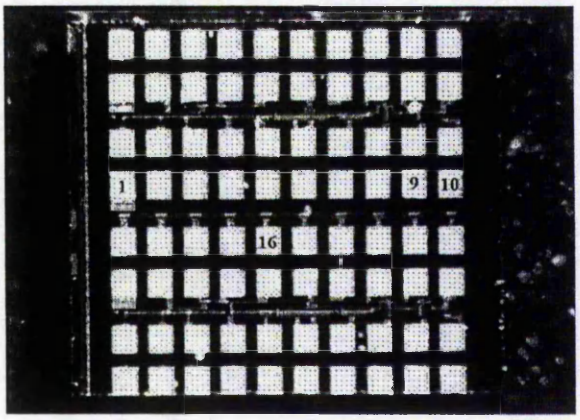
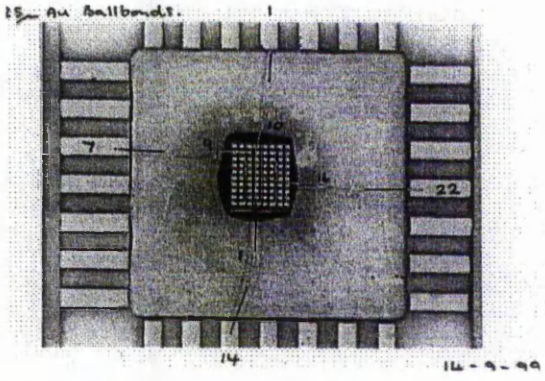


Figure 4-1: Illustration of the functionality of a high-voltage driver to switch the mmLETFEL device'ON' and 'OFF'



Description	Pad Configuration	Pin Configuration
Substrate	1	14
Source	9	7
Gate	10	1
Drain	16	22

Figure 4-3: Schematic of the wire-bonded Alcatel Mietec test die on a chip carrier

The electrical characterisation of the MOSFETs were conducted at Rutherford Appleton Laboratory, Oxford, using the TECAP system. [114] TECAP is an abbreviation for "Transistor Electrical Characterisation and Analysis Package", a system produced by Hewlett-Packard, model HP94445A, but which is now obsolete. It consists of an external source or monitor unit module HP4141B which can be programmed to source voltage and measure current; or to source current and measure voltage. The switching matrix configuration itself is from a module HP4085A, and the connections to the transistor are defined by the switching matrix controller module HP4084B. The recorded measurements, i.e. the extracted data from the electrical characterisation, are stored in LIF, which is a HP disc format. Conversion of this format to a DOS format was done using a conversion program called LIFUTIL. The data was then read and computed using Microsoft Excel for analysis. **Figure 4-4** illustrates a block diagram of the TECAP system.

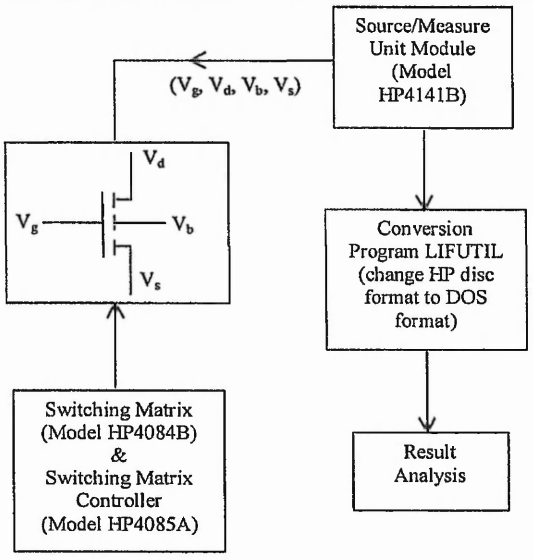


Figure 4-4: Block diagram illustrating the TECAP system used for electrical characterisation of Alcatel test die

Measurements were carried out on nine of the wire-bonded Alcatel test die for obtaining their output characteristics (I_{ds} versus V_{ds}) for $V_{gs}>V_{th}$, and their transfer characteristics (I_{ds} versus V_{gs}) for both low voltage, i.e. for drain voltage, V_{ds}=1V, and high voltage, i.e. for drain voltage, V_{ds}=80V. Comparison of these measured results to the simulated model is presented in the following section, where the SPICE modelling and simulation results are explained and detailed.

4.5 SPICE MODELLING OF ALCATEL NDMOSHV TEST DEVICES

The equivalent circuit of the NDMOSHV model and related SPICE model parameters were obtained from Alcatel Mietec via EuroPractice. The obtained NDMOSHV model is a macro-model consisting of a principal MOS transistor (dominant) modelling the real p-well channel, another MOS transistor (parasitic) modelling the NMOS formed under the gate in the NTUB region and a resistor representing the drift-region in the NTUB. **Figure 4-5** illustrates a schematic diagram of the typical NDMOSHV model used and optimised for SPICE modelling which was obtained via EuroPractice – where 'M' and 'MRM' are the component names for modelling the principal and parasitic MOSFET's respectively. 'I7' and 'I10' are the diode names, while 'I12' represents the drift region resistance and 'Rdummy' the parasitic resistance.

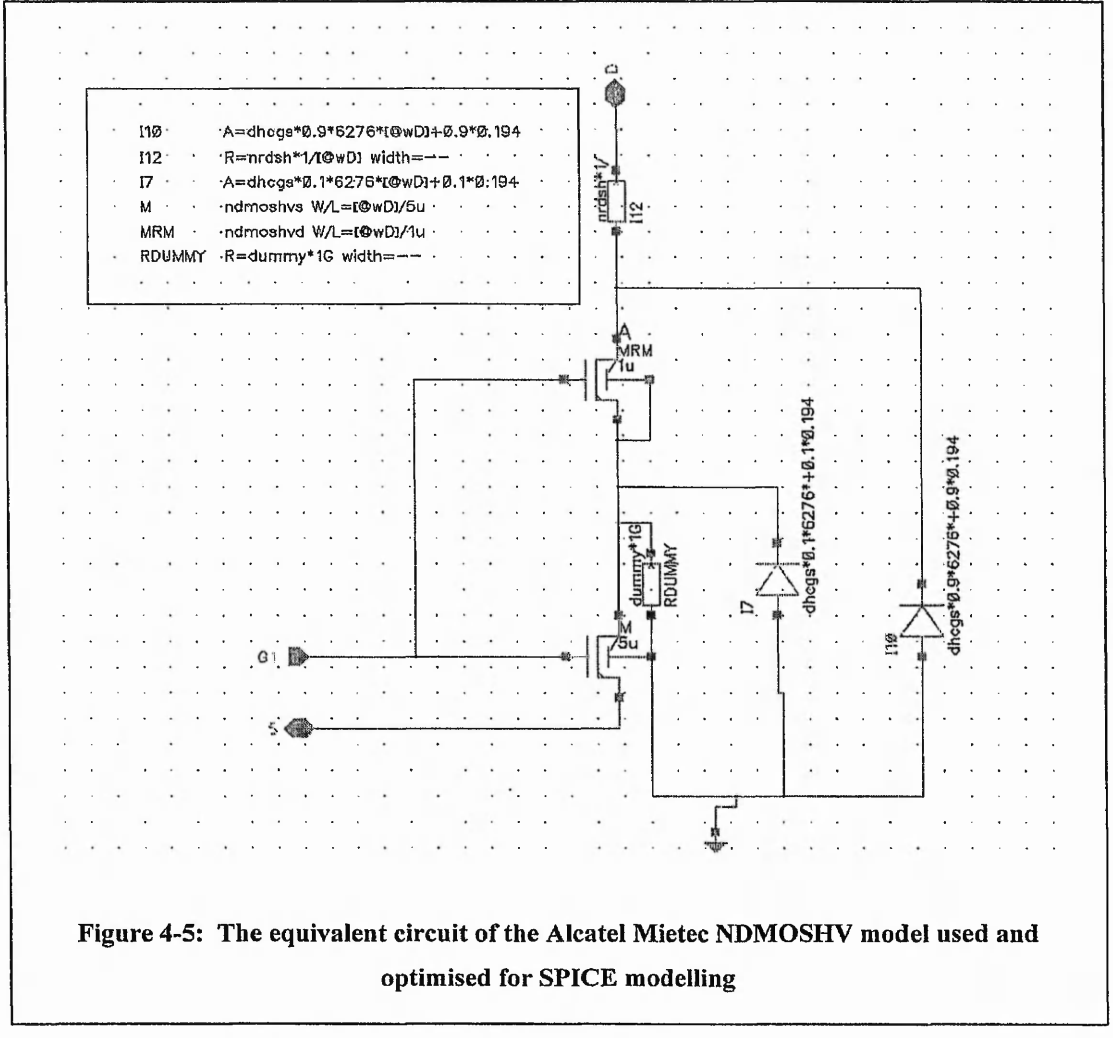
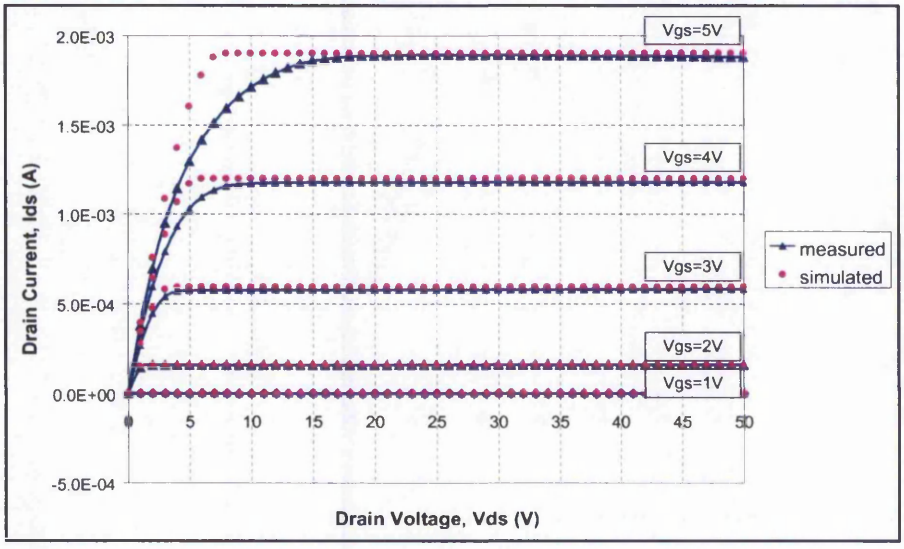


Figure 4-5: The equivalent circuit of the Alcatel Mietec NDMOSHV model used and optimised for SPICE modelling

The characterisation results of these test devices were compared to the simulated data obtained from the SPICE modelling.[115, 116] The initial acquired SPICE model parameters were modified (device geometry parameters) and scaled to fit the corresponding test devices dimensions. The measured values were averaged from the characterisation of nine separate NDMOSHV test devices as described in the previous section.

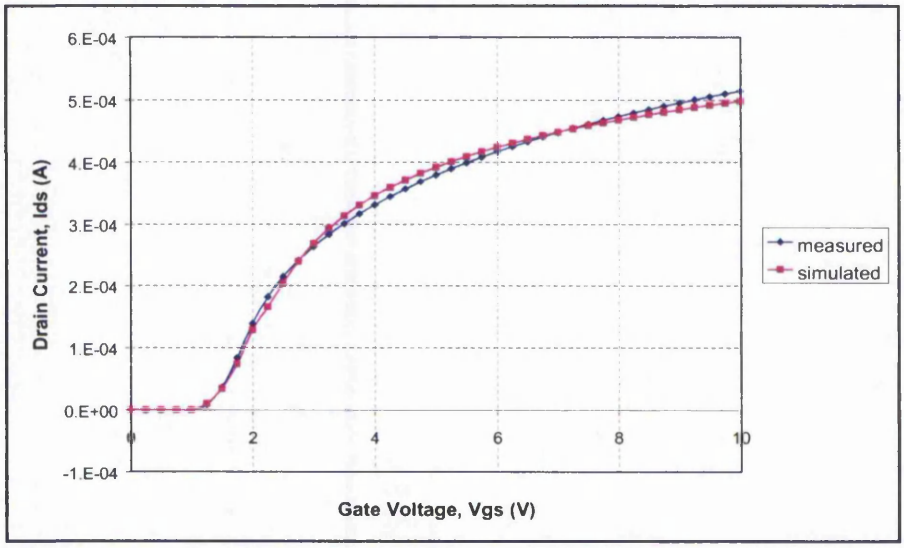
Plot 4-1 depicts the drain current versus drain voltage output characteristics (I_{ds}-V_{ds}) of the NDMOSHV test devices for both the measured and simulated values obtained. These were for incrementing gate voltages, V_{gs}, from 0V to 5V at 1V increment steps.



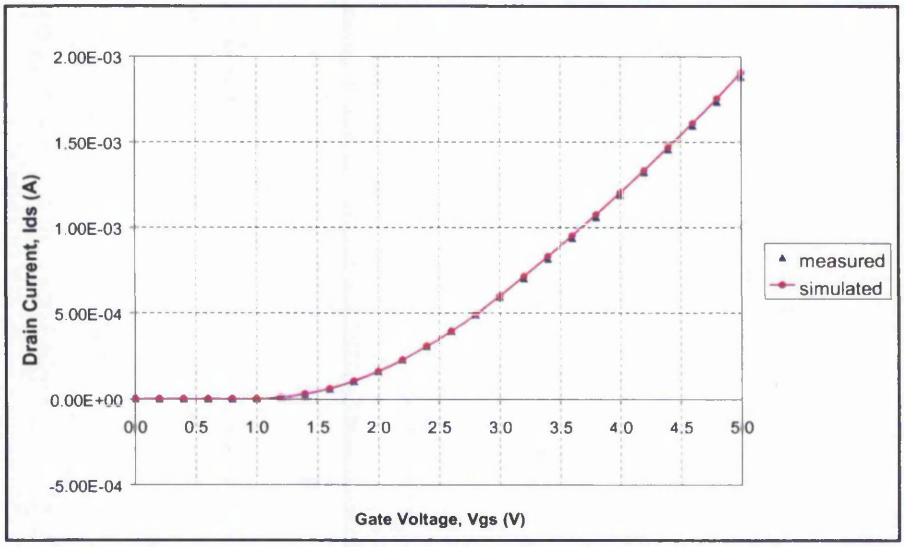
Plot 4-1: Average measured-simulated Ids-Vds characteristics of NDMOSHV test devices (Gate voltages of Vgs=0V-5V at 1V increment)

As observed, the saturation region has been very well modelled, however there is a discrepancy in the linear region. This is because of the SPICE model that has been developed by Alcatel for the NDMOSHV device causing difficulty in obtaining a good correlation between the measured and simulated data. Since this particular device has been developed and manufactured mainly for high-voltage switching applications, the saturation region becomes the more important factor in model optimisation. As intended for the mmLETFEL switching requirement, where the NDMOSHV device has to be operated at a large drain-source voltage as possible, thus the saturation region where $50V<V_{ds}<100V$ is the operating region at which the SPICE simulation should be modelled closely.

The drain current versus gate voltage transfer characteristics (I_{ds}-V_{gs}) were also measured and simulated at both low and high voltages. The obtained measured and simulated data are shown in the following **Plot 4-2** and **Plot 4-3**, firstly at V_{ds}=1V, and secondly at V_{ds}=80V, which are both well within the safe operating region defined by the Alcatel Mietec technology.



Plot 4-2: Average measured-simulated Ids-Vgs characteristics of NDMOSHV test devices (Drain voltage of Vds=1V)



Plot 4-3: Average measured-simulated Ids-Vgs characteristics of NDMOSHV test devices (Drain voltage of Vds=80V)

The accuracy between measured values and simulated values is defined as,

$$Error(\%) = \left| \frac{(Simulated - Measured)}{Measured} \times 100 \right| \qquad \textbf{Equation 4-1}$$

The errors for the NDMOSHV model as defined by Alcatel Mietec SPICE model characterisation and optimisation documentation[117]:

Id_Vg : In general <10%

Id_Vd : In general <10%

In this case, from these measured-simulated characteristics depicted in **Plot 4-1** through to **Plot 4-3**, the error tolerance has been determined to be within the maximum allowable error of 10% in the saturation region for the I_{ds}-V_{ds} characteristic. While the percentage error for the I_{ds}-V_{gs} characteristic was found to be well below 5%. These percentage errors are acceptable within the specified error constraints as described above. It can be deduced that the simulation results achieved for the corresponding NDMOSHV test devices are in agreement with the average measured data. Thus the refined NDMOSHV SPICE model is valid for use in subsequent simulation exercises.

The optimised SPICE model obtained for the Alcatel Mietec NDMOSHV model for the 100V process MOSFET is then used for simulations of an individual integrated mmLETFEL pixel, i.e. a mmLETFEL pixel in series with the Alcatel NDMOSHV model as the switching element as represented briefly in block diagrams in **Figure 4-1**. This simulation exercise is further detailed in the next chapter.

4.6 CONCLUSION

Various commercially available electronic drivers from various fabrication houses have been investigated, i.e. UMC and Holtek from Taiwan, Supertex from USA, and Alcatel Mietec via EuroPractice from Belgium. Problems encountered and associated with the obtained SPICE models, model parameters, and test die, have also been explained corresponding to each driver technology.

A selection of a commercial driver to be used for further analysis and feasibility investigation has been made, and the Alcatel Mietec technology has been chosen due to technology accessibility and cost. The equivalent circuit, the SPICE model parameters of the 100V Process high-voltage n-channel DMOS (NDMOSHV) device, and twenty test die, have all been successfully obtained via EuroPractice.

The obtained test die have been wire-bonded onto chip carriers for electrical characterisation using the TECAP system in RAL. SPICE modelling of the NDMOSHV model relating to the measurements obtained of these test die has been conducted. Based on the measured and simulated results, an optimised SPICE model has been produced.

The measured and simulated values have been compared, and the errors obtained have been found to be within the maximum allowable error margins as specified for the NDMOSHV model by Alcatel Mietec, i.e. <10% in the saturation region for the transistor output characteristics, and <5% for the transistor transfer characteristics.

Contents

5 SPICE Modeling of mmLETFEL Test Devices and the Integrated mmLETFEL Device

5 SPICE MODELING OF mmLETFEL TEST DEVICES AND THE INTEGRATED mmLETFEL DEVICE

5.1 INTRODUCTION

The full fabrication of mmLETFEL test devices on wafers with base electrodes of both TiW and PolySi materials were successful and have been detailed in Chapter 2. The experimental procedures, i.e. the electro-optical characterisation of test devices for the mmLETFEL test devices and electrical characterisation of the obtained driver test die from Alcatel Mietec, were performed and have been illustrated in Chapter 3 and Chapter 4 respectively. The SPICE model parameters obtained for the selected NDMOSHV technology were simulated to predict their operational characteristics and for model optimisation to fit the measured characteristics – these have also been included in Chapter 4.

To complete the investigation, circuit simulation of the integrated pixel consisting of a single mmLETFEL device and its corresponding driver, i.e. an OEIC cell, is performed to determine the switching capability of the selected driver. Prior to this however, the mmLETFEL equivalent circuit is developed. Theoretical simulation using SmartSpice of the mmLETFEL model is then performed based on electrical values obtained from calculations of its developed equivalent circuit. Comparison between the theoretical calculation and the electrical characterisation of mmLETFEL test devices is made to optimise the corresponding SPICE model that can be used later for subsequent simulations of an OEIC pixel.

The final step is to combine the formerly optimised NDMOSHV SPICE model from Alcatel Mietec detailed in Chapter 4, and the presently optimised mmLETFEL SPICE model detailed in the earlier part of this chapter, to form an OEIC equivalent circuit. Further simulations to the developed OEIC SPICE model are performed to predict its performance in the ability to switch the mmLETFEL test device between its 'OFF' and 'ON' states.

5.2 mmLETFEL SPICE MODEL

5.2.1 mmLETFEL Device Structure

Figure 5-1 shows two ACTFEL devices, consisting of a 'barrier-layer ZnS:Mn phosphor' sandwiched between two dielectric layers, feeding into one reflecting micro-mirror, to form a basic mmLETFEL device structure. This simple diagram depicts the basic mmLETFEL structure that is to be used for the derivation of its equivalent circuit and subsequently for the theoretical simulation exercises to be performed.

The inclusion of the base electrodes, i.e. TiW and PolySi, is represented as the micro-mirror underlying material grown onto the Si substrate. The top electrodes, i.e. the 'tri-layer TiW/Al/TiW', is represented as the last metallisation layer grown onto the mmLETFEL stack and then etched away from the emitting aperture.

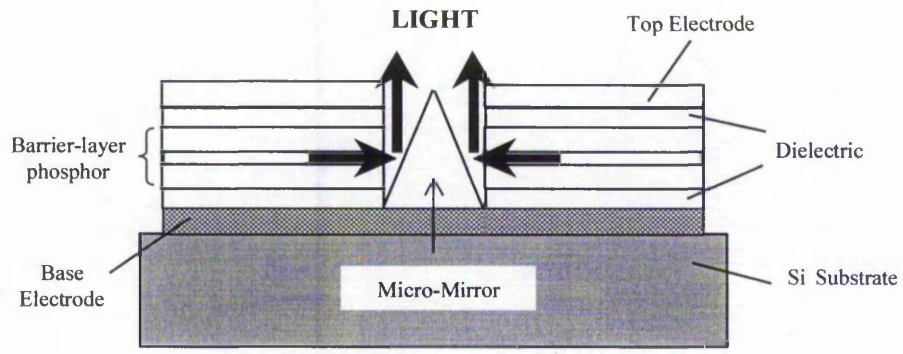


Figure 5-1: Schematic diagram depicting the mmLETFEL basic device structure to be used for derivation of its equivalent circuit and subsequent SPICE simulations

The following sub-section details the development of the equivalent circuit and the electrical parameters determined of which will be utilised for modelling and optimisation of mmLETFEL test devices. The electrical parameters obtained for the simulations in the first instance however are theoretical values calculated for the electrical quantities for the theoretical model. Following the electrical characterisation of mmLETFEL test devices, the SPICE model is then further refined to simulate a close fit to the obtained practical values.

5.2.2 mmLETFEL Equivalent Circuit

To aid in the modelling of the integrated mmLETFEL device, an equivalent circuit of the mmLETFEL device itself was developed. The active area where light is generated in the structure of an LETFEL device is basically the same as that of a conventional ACTFEL device. Thus the equivalent circuit of the ACTFEL which was proposed by Davidson *et al* [118] can be used to model the basic mmLETFEL device. **Figure 5-2** shows the circuit that is used to represent the mmLETFEL test device (including the base electrode resistance).

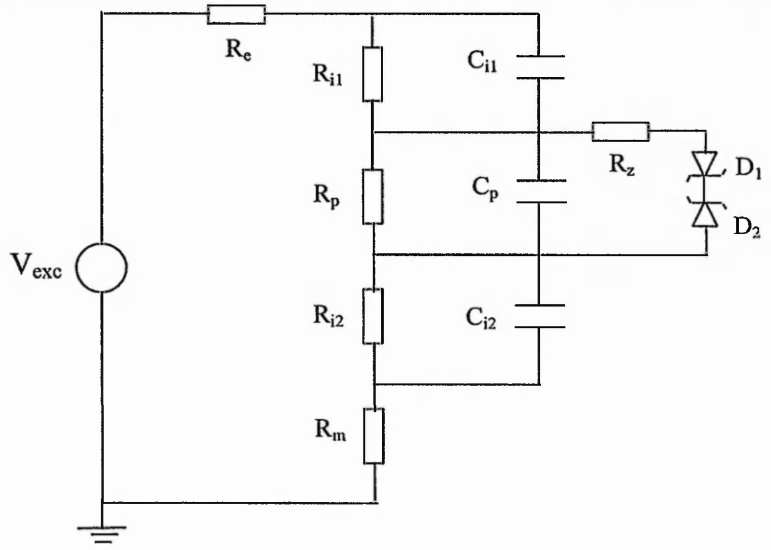


Figure 5-2: Equivalent circuit used for SPICE simulation of a mmLETFEL pixel

The equivalent circuit as shown above is used as a basic SPICE model for the mmLETFEL device. R_e is the resistance of the top electrode, and R_m is the base electrode resistance. R_p and C_p represent the resistance and capacitance of the 'barrier-layer' phosphor respectively; while the resistance and capacitance of the insulator layers, 1 and 2, are denoted by the subscript, *i*. R_z is the "hot electron" resistance associated with hot-electron emission from the phosphor-insulator interface states.[119] The two back-to-back zener diodes, D_1 and D_2, account for the conduction within the phosphor region, and the driving voltage is indicated by V_{exc}. The values for these components are calculated theoretically and simulated accordingly for SPICE correlation between these results and the measured characteristics.

5.2.3 mmLETFEL Device Electrical Parameters

Based on values of resistivity and relative dielectric constant of the materials used in mmLETFEL devices, as well as the defined active area, the values of capacitances and resistances of the respective layers can be calculated.[120]

The capacitance of a layer is calculated using,

$$C = \frac{\varepsilon_o . \varepsilon_r . A}{d} \qquad \textbf{Equation 5-1}$$

The resistance of a layer is calculated using,

$$R = \frac{\rho . l}{A} \qquad \textbf{Equation 5-2}$$

where ε_o is the permittivity of free space, with the value of 8.854×10^{-12} F/m; ε_r is the relative permittivity of a material; A is the active area of a mmLETFEL test device; d and l correspond to the thickness of a layer of material; ρ is the resistivity of a material.

Thus, for a given resolution at *d.p.i.*, the corresponding capacitance and resistance values are (where subscripts p and i denote the phosphor and insulating layers respectively),

$$C_{dpi/i} = \frac{\varepsilon_o . \varepsilon_{ri} . A_{dpi}}{d_i} \qquad \textbf{Equation 5-3}$$

and $$C_{dpi/p} = \frac{\varepsilon_o . \varepsilon_{rp} . A_{dpi}}{d_p} \qquad \textbf{Equation 5-4}$$

$$R_{dpi/i} = \frac{\rho_i . d_i}{A_{dpi}} \qquad \textbf{Equation 5-5}$$

and $$R_{dpi/p} = \frac{\rho_p . d_p}{A_{dpi}} \qquad \textbf{Equation 5-6}$$

where ε_{ri} and ε_{rp} are the dielectric constants of the insulator and phosphor layers; ρ_i and ρ_p are the resistivity values of the insulator and phosphor layers (in Ω-m); d_i and d_p are the thicknesses of the insulator and phosphor layers (in m); and A_{dpi} is the corresponding active area of the mmLETFEL pixel (in m^2) at a given resolution.

The resistance for the top electrode is calculated in the same way using **Equation 5-2**. For the base electrodes however, the sheet resistance was measured for each material, i.e. TiW and PolySi. Since sheet resistance is the ratio of bulk resistivity and thickness for a thin uniform layer, thus the resistance can then be calculated by,

$$R = \frac{\rho(x) \cdot l}{x \cdot w} = \frac{\rho(x)}{x} \cdot \frac{l}{w} = R_{sh}(\frac{l}{w}) \qquad \textbf{Equation 5-7}$$

where $\rho(x)$ is the resistivity as a function of distance x into the wafer; l is the length; w is the width; and R_{sh} is the sheet resistance in Ω/sq.

The back-to-back zener diodes represent the physical breakdown of the phosphor layer during excitation. Therefore, the breakdown voltage of these zener diodes represents the threshold voltage at which the phosphor layer breaks down. Thus, the breakdown voltage can be calculated by dividing the total charge at threshold by the phosphor capacitance,

$$BV_{diode} = \frac{Q_{th}}{C_p} \qquad \textbf{Equation 5-8}$$

where BV_{diode} is the breakdown voltage of the zener diodes; Q_{th} is the total charge at threshold voltage, V_{th}; and C_p is the capacitance of the phosphor layer.

Now, substituting from Equation 3-12 (in Chapter 3), **Equation 5-8** above can be written in terms of V_{th}, thus giving,

$$BV_{diode} = \frac{V_{th} \times C_{off}}{C_p} \qquad \textbf{Equation 5-9}$$

where V_{th} is the device threshold voltage; and C_{off} is the total capacitance before device turn-on, i.e. before the device threshold voltage is reached.

Substituting C_{off} in terms of phosphor and insulator capacitance (assuming that both the insulators are of the same thickness) as provided by Equation 3-14 (in Chapter 3), and by manipulating the above equation, **Equation 5-9** can then be rewritten as,

$$BV_{diode} = \frac{V_{th}}{(\frac{2C_p}{C_i}) + 1} \qquad \textbf{Equation 5-10}$$

The above equation for the breakdown voltage of the zener diodes in effect denotes the same value for the phosphor threshold voltage term, $V_{th,ph}$ as supplied in Equation 3-18 (in Chapter 3). Hence, the calculation performed above using theoretical parameters should match the experimentally determined $V_{th,ph}$ parameter observed for a Q-V characteristic curve. And these can be shown in a Q-V comparison plotted for both the experimental and simulated curves of the same device and same wafer.

The following tabulates the calculations derived from the above equations for the resistance and capacitance values of linear test devices at 130, 300 and 600 d.p.i. resolutions.

Resolution (dpi)	Active Area A_{dpi} $(\times 10^{-12} m^2)$	Resistance ($G\Omega$)		Capacitance (pF)	
		$R_{dpi/i}$	$R_{dpi/p}$	$C_{dpi/i}$	$C_{dpi/p}$
130	88515.7	$4.09 \times d_i$	$113 \times d_p$	$\frac{12.54}{d_i}$	$\frac{5.878}{d_p}$
300	39760.0	$9.10 \times d_i$	$252 \times d_p$	$\frac{5.633}{d_i}$	$\frac{2.64}{d_p}$
600	18637.5	$19.42 \times d_i$	$537 \times d_p$	$\frac{2.64}{d_i}$	$\frac{1.238}{d_p}$

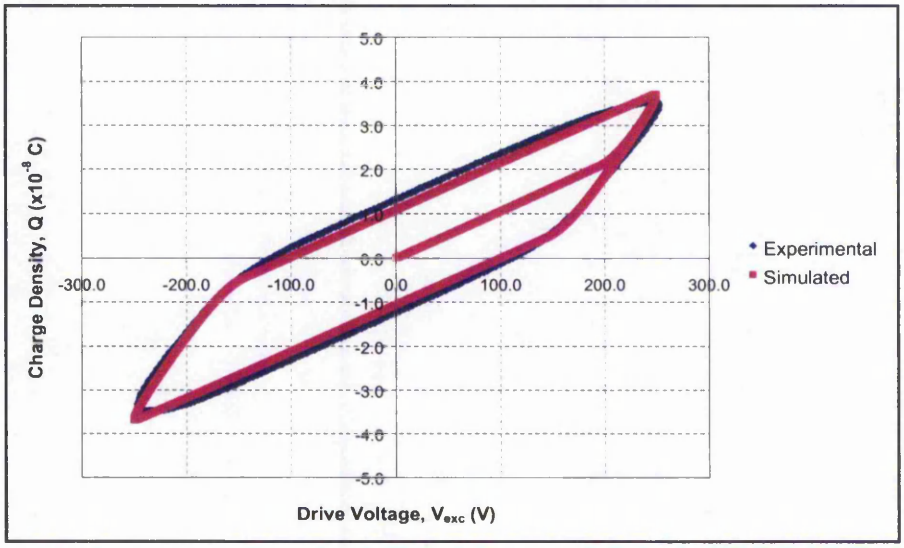
Table 5-1: Capacitance and resistance values calculated for both insulator and phosphor layers at various resolutions (where di and dp are the fabricated thickness respectively)

However, because the characterisation of mmLETFEL devices had been focused on test device TDEV11, the theoretical values for the calculated resistance and capacitance are based on this structure for SPICE simulation and correlation purposes. The following section thus details the simulation results.

5.2.4 mmLETFEL Simulations

In this case, the active area calculated for TDEV11 is at $A_{(TDEV11)} = 1.233\mu m^2$; the average dielectric constants measured for ZnS:Mn, Y_2O_3 and Si_3N_4, are $\varepsilon_p = 8.3$, $\varepsilon_{i\ (Y2O3)} = 12$, and $\varepsilon_{i\ (Si3N4)} = 7$, with thicknesses of $d_p = 8000Å$ (including the 100Å Y_2O_3 'barrier-layer'), $d_{i\ (Y2O3)} = d_{i\ (Si3N4)} = 3000Å$, respectively; and the average sheet resistance measured for TiW and PolySi, are $R_{s\ (TiW)} = 2.46\Omega$/sq and $R_{s\ (PolySi)} = 15.72\Omega$/sq, , with thicknesses of $l_{(TiW)} = 3000Å$ and $l_{(PolySi)} = 4500Å$, respectively.

Concentrating on the recent wafers as these utilise the same phosphor powder for mmLETFEL deposition, thus the comparison made minimises the number of involved variables, the following plot depicts the experimental and simulated results of wafer CR123.



Plot 5-1: Q-V characteristics of experimental-simulated results of mmLETFEL TDEV11 from wafer CR123 (Y2O3 as insulators and TiW as base electrode)

The capacitance values before and after turn-on, and the breakdown voltage, of zener diodes obtained theoretically using **Equation 5-1** and **Equation 5-10** previously, and those values obtained practically from the electrical characterisation as explained in Chapter 3 are tabulated in **Table 5-2**, for mmLETFEL test device TDEV11 of wafer CR123. In the same manner, simulations were also conducted for mmLETFEL TDEV11 of wafer CR128 to obtain the differences observed between the measured and simulated characteristics.

Wafer No	Parameters	Experimental Determination	Simulated Capacitance Values	Derived Values used for Simulation
CR123	C_{off}	1.09 x 10^{-10} F	1.06e^{-10} F	
	C_{on}	2.73 x 10^{-10} F	3.15 x 10^{-10} F	
	BV_{diode}	130 V		123.1 V
CR128	C_{off}	1.10 x 10^{-10} F	1.06 x 10^{-10} F	
	C_{on}	2.60 x 10^{-10} F	3.41 x 10^{-10} F	
	BV_{diode}	118 V		112.3 V

Table 5-2: Experimental-simulated results of capacitance and diode breakdown voltage for TDEV11 of wafer CR123

From the table above, it can be noted that the experimental and simulated values for the 'on' and 'off' capacitance, i.e. C_{on} and C_{off}, have been found to be within an error tolerance of approximately ±20% and ±4%, respectively. There are several reasons in which to explain the differences that are noted between these results.

One of the main reasons is the dielectric constants being different due to the variables involved during the fabrication process, e.g. thickness of materials grown are not accurate each time. This variation in the obtained thickness is usually the main factor in affecting the capacitance values obtained by measurements. Also, the possibility of moisture existing in the atmosphere and the difficulty in maintaining a totally 'clean' environment during the fabrication of the entire wafer can interfere with the outcome of the device's performance.

Especially for this particular investigation, the wafers fabricated for use in this research have undergone their entire processing route over 3 main locations; i.e. the fabrication of the base wafers including the micro-structures and base electrodes at NMRC (Cork, Ireland), the deposition of mmLETFEL device and photolithography process at TNTU, the deposition of the top electrodes, etching, and post-processing at RAL (Oxford).

The presence of stray capacitances within the circuitry, e.g. from external leads and external components used during the characterisation exercise, are also taken into account.

Another reason is the theoretical model used for the SPICE simulation did not account fully for possible capacitances existing at the phosphor/insulating interface states, as an understanding of the electric field occurring during breakdown would be necessary to determine a better and more accurate model.

Douglas and Wager,[121, 122] refined this model by adding a parallel resistor-capacitor combination, C_T and R_T, in series with the back-to-back zener diodes, D_1 and D_2, and series resistor, R_z. This was believed to enable representation of the states density and time response for the interface states. In addition, it is believed to be able to describe the waveform dependence of the turn-on voltage. This phenomenon is currently being looked into in conjunction with another current research programme[123] as the mmLETFEL structure develops.

In this case, although the SPICE model used for the simulation was the simplified model, it had been sufficient to demonstrate its suitability for further investigation. The correlation between the experimental and simulated results for the 'on' and 'off' capacitances and threshold voltages have been determined to within an approximate error tolerance of ±20% and ±4%, thus ensuring the overall performance of the device has not been distorted.

5.3 OEIC Model Circuit

From the previous section and from Chapter 4, the refined mmLETFEL SPICE model and the refined NDMOSHV SPICE model form the OEIC equivalent circuit for further simulations in determining the switching characteristics, i.e. the voltage range necessary to enable switching of the mmLETFEL pixel to its 'ON' and 'OFF' states. **Figure 5-3** shows the integrated mmLETFEL pixel – circuit diagrams used for the SPICE simulations of mmLETFEL devices are also appended in Appendix E (descriptions of the electrical parameters depicted in the diagram have been included in Chapter 4 and the earlier section of this chapter; and the model names used in SmartSpice simulations listed in Appendix D).

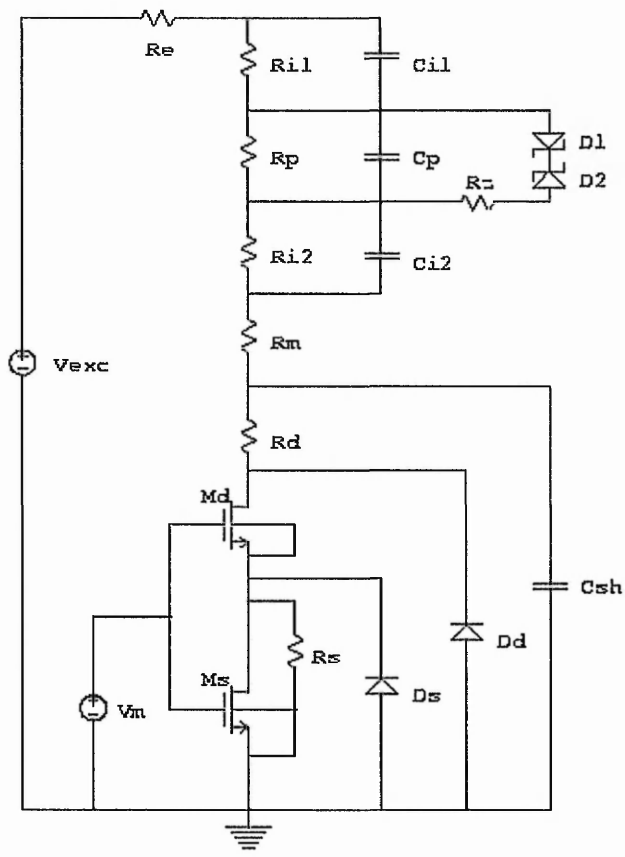


Figure 5-3: Equivalent circuit used for SPICE simulation of an integrated mmLETFEL pixel

A shunt capacitor, C_{sh}, has been added across the NDMOSHV model, connecting the drain of the MOSFET to ground. Thus the drain-source total capacitance can be modified to control the drain-source voltage that is dropped across the NDMOSHV. For simulation purposes, the values calculated for the mmLETFEL structure at various resolutions have been based on equations depicted in **Table 5-1**, and the drive conditions as utilised for the electro-optical charactertisation of mmLETFEL test devices explained in Chapter 3, i.e. at $V_{exc(pk)}$=±250V and a frequency of 5kHz.

In this case, numerous simulations of the NDMOSHV device in switching the mmLETFEL device 'ON' and 'OFF', using various values for the shunt capacitor, C_{sh}, have been performed. Since the maximum breakdown voltage of this device is 100V, simulations have been concerned with keeping the voltage drop across the NDMOSHV device to within 5% and 10% of this maximum drain-source voltage. Hence, values of C_{sh} have been determined for up to V_m≅90V (within 10%) and V_m≅95V (within 5%), and for mmLETFEL devices calculated at 130, 300 and 600 d.p.i. resolutions.

Resolution	V_{diff}=V_m≅90V (within 10%)		V_{diff}=V_m≅95V (within 5%)	
	V_m (V)	C_{sh} (x 10^{-12}F)	V_m (V)	C_{sh} (x 10^{-12}F)
130	89.6	37.5	94.4	34.5
300	89.9	16.7	94.7	15.4
600	89.7	7.8	94.4	7.2

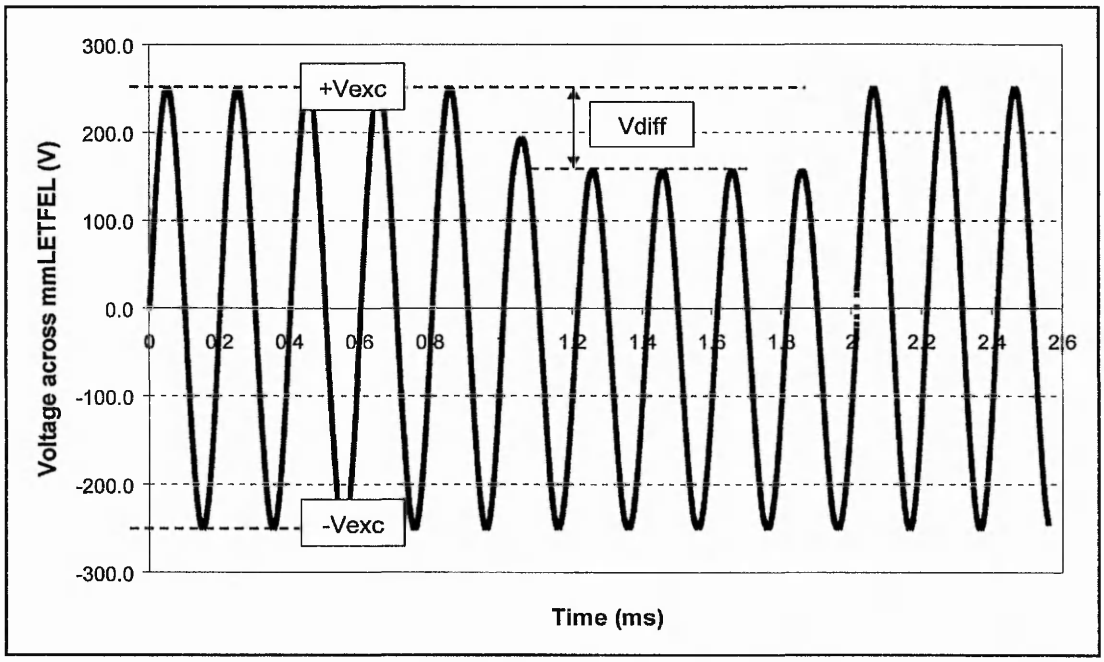
Table 5-3: Simulated values of shunt capacitance, *Csh*, found for switching mmLETFEL devices at various resolutions

Thus, for a 600 d.p.i. mmLETFEL device, a shunt capacitance value of 7.8pF is needed to cause a voltage range of 89.7V to be dropped across the NDMOSHV device, which is within the 10% margin of the maximum breakdown voltage.

The need of introducing the shunt capacitor in order to maintain the switching voltage range, the design and fabrication of this added capacitor prior to the deposition of the mmLETFEL device would require modification to the NDMOSHV device layout. This might mean having to extend the field oxide layer – that acts as an insulator around the MOSFET to isolate each individual transistor from adjacent devices – such that it connects the substrate to the base electrode of the mmLETFEL device. It is now a capacitor that sits parallel to the NDMOSHV device.

However, the eventual design layout for this purpose, including the use of suitable material and thickness obtained such that the capacitance value is within the two ranges as specified in **Table 5-3**, has to be discussed further with Alcatel regarding the technology constraints and possible fabrication factors influencing this outcome.

Plot 5-2 depicts the voltage drop across a mmLETFEL device (600 d.p.i. resolution) during the switching operation, while being driven by a sinusoidal waveform at $V_{exc(pk)}$=±250V with a frequency of 5kHz.



Plot 5-2: The voltage drop across a mmLETFEL test device (at 600 d.p.i.) vs time

It can be observed that the resultant voltage across the mmLETFEL is asymmetrical, with only the positive cycle being reduced by a value of V_{diff} during the mmLETFEL 'OFF' state, i.e. when the NDMOSHV device is switched 'OFF' by removal of the gate voltage. This is due to a p-n junction being formed between the drain and substrate during conduction. This has been represented by the diodes depicted in the circuit diagram of **Figure 5-3**, I7 (model name D_s) and I10 (model name D_d).

During the positive cycle of the excitation voltage, a current flow is observed through the mmLETFEL device and the NDMOSHV device. The ratio of the voltage drop for each of these devices respectively is determined by the capacitive network, as has been explained. However, during the negative cycle of the excitation voltage, the voltage is conducted via the diodes I7 and I10. Thus, a current flow in that direction effectively shorts the drain to the substrate. Hence, as observed, the negative cycle of the voltage V_{letfel} in **Plot 5-2** still maintains the full excitation voltage swing of –250V with respect to ground. However, the driving a.c voltage across the mmLETFEL device is reduced by V_{diff}.

Therefore, as illustrated in **Figure 4-1**, and now in **Plot 5-2**, in order to switch the mmLETFEL cell to its 'OFF' state, the effective voltage drop across the mmLETFEL device has to be below the peak-to-peak threshold level of the device. In other words, to shift the peak-to-peak voltage seen across the mmLETFEL cell to below the luminance threshold voltage on both polarities. Hence, $[V_{letfel(pk\text{-}pk)}=V_{exc(pk\text{-}pk)}-V_{diff}]<V_{th(pk\text{-}pk)}$. As such, the peak drive voltage at which to drive the devices is dependent upon both the threshold level of the corresponding mmLETFEL devices, as well as the switching range of the modulation voltage for which the individual driver is able to block.

Table 5-4 illustrates further the 'ON' and 'OFF' states conditions during the switching operation. When a positive voltage of V_{gs} is supplied to the gate of the NDMOSHV model, this turns on the NDMOSHV device and effectively grounds the drain connection, and all of the a.c. excitation voltage, $V_{exc(pk\text{-}pk)}$, is applied across the mmLETFEL cell. Once the $V_{exc(pk\text{-}pk)}$ exceeds the peak-to-peak threshold voltage level, $V_{th(pk\text{-}pk)}$ of a mmLETFEL device, light activation is realised and it is said that the device is now turned 'ON'.

States	Gate Voltage V_{gs} (V)	Voltage across the mmLETFEL $V_{letfel(pk\text{-}pk)}$ (V)
ON	$+V_{gs}$	$V_{exc(pk\text{-}pk)}$ $[>V_{th(pk\text{-}pk)}]$
OFF	$V_{gs}=0$	$V_{exc(pk\text{-}pk)} - V_{diff}$ $[<V_{th(pk\text{-}pk)}]$

Table 5-4: mmLETFEL 'ON' and 'OFF' states during the switching operation

On the other hand, during the period of V_{gs}=0V (when the gate of the NDMOSHV device is grounded, i.e. shorted to the source), the NDMOSHV device is now an 'open' switch. The NDMOSHV device is turned off, thus no channel exist, and so the drain-source capacitance dominates. The existing internal drain-source capacitance of the NDMOSHV device thus

forms a capacitive network with the mmLETFEL's total capacitance. Depending on the charge storage, this determines the voltage drop across both the mmLETFEL test device and the NDMOSHV device. The use of a shunt capacitor, as explained, effectively acts to increase the drain-source capacitance, hence controlling the voltage that is divided between the NDMOSHV device and the mmLETFEL device.

With a partial of the excitation voltage, V_{exc}, being dropped across the drain-source capacitance, the effective voltage across the mmLETFEL is now the difference of $V_{letfel}=V_{exc(pk\text{-}pk)}-V_{diff}$. When the peak-to-peak threshold voltage level of the mmLETFEL device, $V_{th(pk\text{-}pk)}$, is not reached, light activation is not realised, and it is said that the mmLETFEL cell is now turned 'OFF'.

Therefore, the desired voltage difference, V_{diff}, must be twice of the modulation voltage required to block the a.c. high voltage on one polarity. It should be large enough to cause the effective voltage drop applied across the mmLETFEL device, $V_{letfel(pk\text{-}pk)}$, to go below its peak-to-peak threshold voltage, $V_{th(pk\text{-}pk)}$. At the same time, this voltage must not exceed the allowable safe operating region of the specified NDMOSHV device supplied.

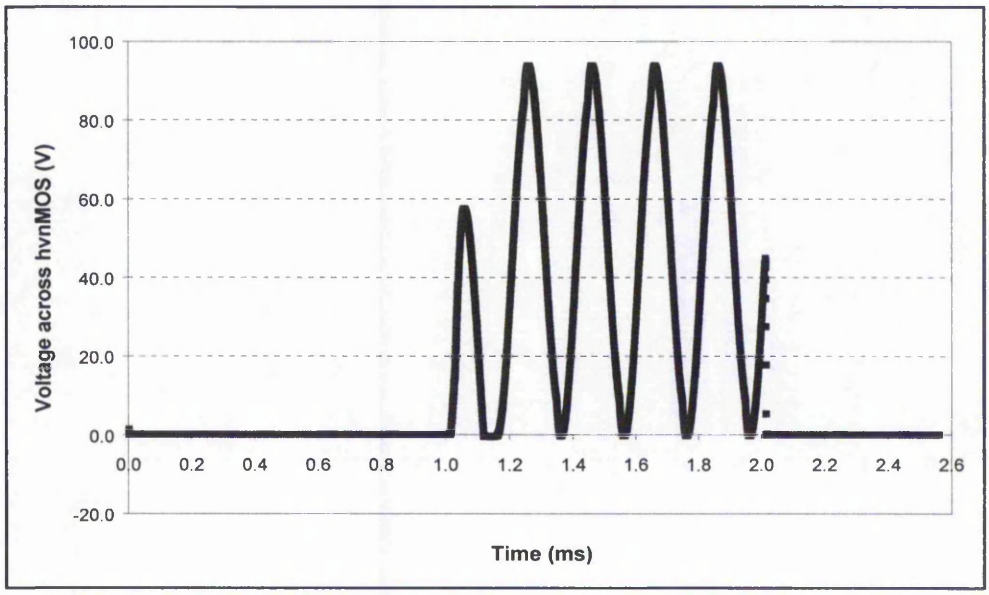
The limits that are set for the forbidden region in which these devices can never be operated in have been specified by Alcatel and already mentioned in Chapter 4. The border of this prohibition has been set at V_{gs}<8V and V_{ds}<100V, and V_{gs}<12V and V_{ds}<65V. Thus, switching on the NDMOSHV to address the mmLETFEL device at V_{gs}=5V can allow operations of up to a maximum of V_{ds}=100V.

However, continuous operation of the NDMOSHV device at high voltages can cause degradation of the DMOS characteristics and induce a large shift in the electrical parameters. Therefore the safe operating area imposed by this degradation phenomenon is set at V_{gs}<7V and V_{ds}<100V, and V_{gs}<12V and V_{ds}<50V.[124]

Shown in **Plot 5-3**, the simulated voltage drop across the NDMOSHV device was found at its peak of V_{ds}=89.7V, i.e. V_{diff}=89.7V. As previously shown in **Plot 3-8** of Chapter 3, the threshold voltages for mmLETFEL test devices of recent wafers CR123 (with Y_2O_3 insulators and TiW base electrode) and CR128 (with Y_2O_3 insulators and PolySi base electrode) were found to be at approximately V_{th}=186.4±2.0V (i.e. $V_{th(pk\text{-}pk)}$=372.8V) and V_{th}=182.3±2.0V (i.e. $V_{th(pk\text{-}pk)}$=364.6V) respectively.

Thus in order to render the peak-to-peak voltage drop across the mmLETFEL device to be below the peak-to-peak threshold level of the device, the excitation voltage has to be driven at a maximum of $\pm(V_{diff}/2)$ above the threshold level. In this case, $V_{diff} \leq 100V$ for the Alcatel Mietec 100V process DMOS drivers. Hence, $V_{letfel(pk\text{-}pk)}=V_{exc(pk\text{-}pk)}-V_{diff}=450-89.7=360.3V$, which is below the peak-to-peak threshold voltage found for these mmLETFEL devices.

The voltage drop across the drain-source contacts of the NDMOSHV device is shown in **Plot 5-3** below.



Plot 5-3: The voltage drop across the NDMOSHV device vs time

Therefore, by operating the drive voltage for the device at $V_{exc}=\pm 225V$, during the 'ON' state the voltage drop across the mmLETFEL device (600 d.p.i.) is at $V_{letfel(pk\text{-}pk)}=V_{exc(pk\text{-}pk)}=450V$.

While during the 'OFF' state, the voltage drop across the mmLETFEL device (600 d.p.i.) is at $V_{letfel(pk\text{-}pk)}=V_{exc(pk\text{-}pk)}-V_{diff}=360.3V$. As a result the luminance for these 'OFF' and 'ON' states is found at a range between zero and the corresponding luminance at its peak drive voltage of $V_{exc}=225V$. Hence, the mmLETFEL pixel can be switched fully 'ON' and 'OFF' with a switching voltage range of $V_{ds} \approx 100V$.

5.4 CONCLUSION

SPICE modelling of the mmLETFEL test device utilising the theoretically derived values of the capacitance values and threshold voltages have produced a close correlation with the experimental results. The turn-on and turn-off capacitances as well as the breakdown voltage of the zener diodes (representing the physical breakdown of the phosphor layer itself), have all shown a percentage error of well within <10%, thus indicating that the simplified model used thus far is suitable for further investigations.

Using the mmLETFEL model and the previously optimised Alcatel NDMOSHV SPICE model (Chapter 4), the integrated mmLETFEL device equivalent circuit has been constructed and simulated. The voltage range obtained for switching the mmLETFEL pixel at 600 d.p.i. resolution between its 'ON' and 'OFF' states has been found at V_{diff}=89.7V (within 10% of the maximum drain-source voltage V_{ds}), which is well within the safe operating region of the NDMOSHV device as specified by Alcatel Mietec. The value of the shunt capacitance in aiding the determination of this voltage switching range has been simulated at C_{sh}=7.8pF.

With a peak drive voltage at V_{exc}=±225V, this can result in a voltage drop across the mmLETFEL during its 'ON' and 'OFF' states to be at $V_{letfel(pk\text{-}pk)}$=$V_{exc(pk\text{-}pk)}$=450V, and $V_{letfelpk\text{-}pk)}$=360.3V, respectively. Hence, the luminance operating at its 'ON' and 'OFF' states would be at the corresponding luminance value at the peak drive voltage of V_{exc}=±225V, and 0fL at V_{letfel}=±180.15V, which is well below the threshold voltage of the mmLETFEL test devices found previously (Chapter 3).

Contents

6 Final Conclusions

6 FINAL CONCLUSIONS

6.1 SUMMARY OF THESIS

The main aim of this research was to investigate the feasibility and commercial viability of developing an integrated light source utilising the mmLETFEL technology, as an alternative low-cost yet high-intensity light source for electrophotographic printing applications. In short, the possibility of defining within the same pixel an integrated cell consisting of the mmLETFEL device and its corresponding electronic drive circuitry.

To summarise, this research included investigations into:

(a) the fabrication of mmLETFEL test devices utilising alternative insulator materials and base electrode materials;
(b) the characterisation of these fabricated mmLETFEL test devices, leading to determination of optimum features for maximum efficiency in terms of luminance, as well as the determination of the material configuration (suitable insulator and base electrode materials) of mmLETFEL device structure to be used for possible development of an integrated mmLETFEL device;
(c) examination of various commercially available high-voltage electronic drive technologies, leading to the electrical characterisation and SPICE modelling of test dies of the selected drive technology;
(d) SPICE modelling of an integrated mmLETFEL device – combining the developed mmLETFEL model and the optimised driver model – leading to the investigation of the selected driver technology in the switching range capability of an mmLETFEL pixel between its 'ON' and 'OFF' states;
(e) the definition of a possible processing route of an integrated mmLETFEL device structure for an OEIC development.

6.2 ACHIEVEMENTS

1. Discharge of a photoconductive material using LETFEL edge-emitter

Assessment of the lateral emission of a LETFEL test device in discharging a photoconductively charged organic drum was conducted at Imperial College, London, with the assistance of Dr. J. Veres. This particular edge-emitter device, i.e. eeLETFEL, used for this test has a recorded luminance obtained at 170kfL with a drive frequency of 5kHz. Assuming a 50% discharge, it managed to discharge a photoconductive drum at a speed of up to 13 p.p.m. Thus, in order to facilitate higher print speeds LETFEL devices with greater luminances are desirable, and especially for LETFEL on micro-mirror technology, good outcoupling efficiency at the emitting apertures is crucial in producing the required high-intensity light sources.

2. Fabrication and Characterisation of mmLETFEL Test Devices

Fabrication of mmLETFEL test devices deposited on underlying micro-mirrors and alternative base electrode materials, PolySi and Ti/W (both processes performed at NMRC, Cork) have been successful. The base electrode deposition process need to be compatible with the thermal annealing process in the mmLETFEL technology that is eminent and necessary for light emission activation. Also, due to the need of defining contacts to the base electrodes, etching of these bondpads was required, and thus an alternative insulator material, PECVD Si_3N_4 (performed at Qudos, RAL) has also been investigated, in addition to the conventional Y_2O_3 material, since Y_2O_3 is difficult to etch.

Four different configurations utilising these two base electrode and insulator materials were tested and measured for their electrical and optical characteristics. It has been found that the Y_2O_3 material exhibited lower threshold voltage and steeper L-V characteristics compared to the PECVD Si_3N_4 material, and showed reliable device performance in terms of dielectric strength due to its higher dielectric constant characteristics.

At the same time, mmLETFEL test devices on both TiW and PolySi base electrodes have demonstrated comparable characteristics, thus indicating that the prior deposition of base electrodes has no great significance effect on the overall device performance. However, PolySi has been the suggested material due to its slightly higher luminance and luminous

efficiency found. Therefore, the mmLETFEL device suitable for integration purposes has been proposed for the configuration using the Y_2O_3 as the insulator and the PolySi as the base electrode.

Electrical and optical characterisation of various mmLETFEL device structures has also been conducted and optimum features of mmLETFEL test devices were determined for further improvement to the existing linear test devices, subsequently introducing new dimensions that can be incorporated to modify the existing design of the prototype printer devices. These have been determined for active material lengths at 300μm on either side of the micro-mirror structure, side-wall widths at 4μm, aperture widths at 4μm, and micro-mirror widths at 3μm.

3. Dicing and Wire-bonding of mmLETFEL Test Devices

Dicing and wire-bonding of mmLETFEL test devices have been successfully performed at TNTU using the Sola Basic Tempress Model 602, and the K&S Wedge-Bonder Model 4123. Explanation of the operation of these two systems are detailed in Appendix B. Lists of suggested dicing and wire-bonding parameters are also included, allowing for these processes to commence for subsequent mmLETFEL devices.

4. Characterisation and SPICE Modelling of High-Voltage MOSFET's

Investigations into various commercially available high-voltage electronic drivers have been performed via SPICE modelling of available model parameters obtained from various fabrication houses, including Holtek (50V process) and UMC (28V process) from Taiwan, Supertex (300V process) from USA, and Alcatel Mietec (100V process) from Belgium.

Due to technology accessibility and cost, the Alcatel Mietec technology has been selected for further investigation. 20 test die, and the corresponding SPICE model parameter of the NDMOSHV technology have been supplied via EuroPractice.

Measured and simulated results were obtained from electrical characterisation of these test die using the TECAP system at RAL, and SPICE modelling of the equivalent SPICE model using SmartSpice (VWF), from Silvaco International. The comparison revealed a <10% error in the saturation region for the transistor output characteristics, and a <5% error for the

transistor transfer characteristics. These errors were found to be within the maximum allowable error margins as specified for the NDMOSHV model by Alcatel Mietec. Thus, the optimised SPICE model corresponding to the test die obtained has been produced.

5. SPICE Modelling of the mmLETFEL Device and the Integrated mmLETFEL

A simple equivalent circuit of the mmLETFEL test device has been developed and the corresponding SPICE model simulated for comparison with the measured characteristics. It has been found that the percentage error between the experimental-simulated correlation was well within 10% margin. The same model could be used for subsequent simulations, provided that the phosphor used for deposition was the same, and that the same processing sequence has been undertaken. Since different fabrication techniques can produce volatile results, any change to the processing step can influence the outcome of the SPICE simulated model, causing the error margin between this and its corresponding measured data to deviate. At present however, the developed simple model was sufficient for further simulations of an integrated mmLETFEL device with its corresponding drive circuitry.

Simulation of an integrated mmLETFEL pixel – the equivalent circuit of a mmLETFEL test device in series with the optimised SPICE model of the Alcatel Mietec NDMOSHV technology – have been successful. Results show the voltage range achieved between the 'OFF' and 'ON' state of the mmLETFEL test device being driven by a sine wave at 5kHz, was 89.7V, thus rendering the voltage drop across the mmLETFEL device during the 'OFF' state to be at $V_{exc(pk\text{-}pk)}$-V_{diff}=450V-89.7V=360.3V, and during the 'ON' state to be at $V_{exc(pk\text{-}pk)}$=450V. Hence, the corresponding luminance range obtained from L-V characteristics of a typical test device with Y_2O_3 insulator and PolySi base electrode, were 0fL (at $V_{letfel(pk\text{-}pk)}$=360.3V, i.e. $V_{letfel(pk)}$=180.15V) and 88.3fL (at $V_{letfel(pk\text{-}pk)}$=$V_{exc(pk\text{-}pk)}$=450V, i.e. $V_{exc(pk)}$=225V), for the 'OFF' and 'ON' states respectively.

Thus, it has been demonstrated that the Alcatel Mietec NDMOSHV model technology was feasible for use as the drive circuitry for the mmLETFEL technology.

6.3 LATEST DEVELOPMENTS OF mmLETFEL DEVICES

During the course of this research programme, several investigations have been undertaken simultaneous to this investigation. Among these investigations are:

1. Optimisation and characterisation of the fabrication process for the barrier-layer mmLETFEL test devices.[62]
2. Ion milling of the LETFEL emitting aperture structure; with and without the pre-fabricated underlying micro-mirrors.[63]
3. Laser annealing of the LETFEL structure; on thin films,[64] and the full device structure.[65]

Full fabrication of mmLETFEL test devices on pre-fabricated micro-mirrors on Si wafer from NMRC in Cork, Ireland, and incorporating the 'barrier-layer' phosphor has been successful, and the process conditions have already been detailed in Chapter 2. However, due to the cost of these base wafers obtained from Cork, investigations of pre-fabricating these micro-mirrors at Qudos, RAL, instead, has started. Thus far, results show that micro-mirrors fabricated with an angle of 45° are feasible. In addition, the cost has been greatly reduced from £80 per wafer (quotation from NMRC) to £47 (quotation from RAL). Due to the light confinement and wave-guiding nature of LETFEL devices, signifying that these micro-structures can be utilised as wave-guides instead of reflecting mirrors, more recent work includes fabricating vertical micro-structures (vmLETFEL) instead. Characterisation of these vmLETFEL devices has been proposed as future research investigating into the optical properties of such devices. This concept is briefly explained in the following.

Ion milling of mmLETFEL test devices, with the underlying micro-mirrors has been investigated.[125] It has been shown that a ~2x enhancement in the light intensity has been measured for the etched profile of the mmLETFEL test devices. At the same time, the angular profile obtained for these etched devices was observed to redistribute towards narrower angles of view, thus increasing the overall coupling efficiency of these etched test devices.

It has been reported that compared to conventional non-etched devices, an approximately 12% increase occurs of light output for head-mounted displays application where the acceptance angle investigated was for <30°, and an approximate 5% increase occurs of light output for electrophotographic printing applications where the acceptance angle investigated was for <6°. As such, this etching technique has been successful in defining the emitting aperture of mmLETFEL test devices.

In addition, two other outcoupling mechanisms have been examined.[126] Experimental results demonstrated that the surface-emitting edge-emitter utilising micro-mirror fabricated at angles of 45° did not exhibit a substantial improvement compared to conventional non-etched devices. On the other hand, theoretical optical modelling indicated that enhancement to the output properties would increase if the micro-structures were fabricated with an angle of 90° instead, resulting in an abrupt open-end surface edge-emitter.[64] These vertical micro-structures would enable wave-guiding of the light through to the outside rather than the initial intention of reflecting the light off the micro-mirrors. Specifically for electrophotographic printing applications, a coupling efficiency up to 30% is expected for these vertical edge-emitters, an increase of more than twice the etched profile. **Table 6-1** illustrates further the outcoupling mechanisms explained thus far.

The success of laser annealing on the first fully fabricated mmLETFEL devices has been reported recently.[127] Here, test devices with top electrodes consisting of Ti/W material have been fabricated on the same wafer facilitating direct comparison between both thermal and laser annealing. L-V characteristics of these test devices were then measured at a drive frequency of 5kHz. It is observed that as the fluence of the laser annealing pulse is increased, the luminance also increases. By using a single 20-ns pulse from a KrF laser, an incident fluence of 1.0 Jcm^{-2} produced test devices of almost equal luminance to test devices that have been thermally annealed at 500°C for 1 hour in vacuum. Thus, for fluences greater than 1.0 Jcm^{-2}, mmLETFEL test devices may be possible with luminances greater than conventional mmLETFEL test devices that have been thermal annealed.

The following table illustrates the various outcoupling mechanisms and the corresponding device structure, with the coupling efficiency obtained for each – where italicised, this shows the predicted outcome for the emitter structure that was proposed for further investigation.

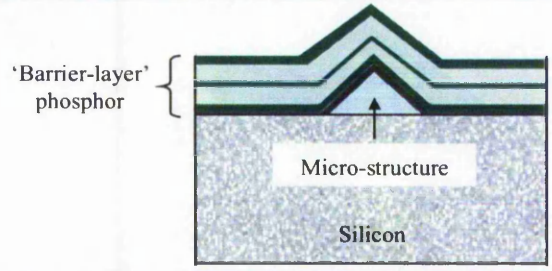
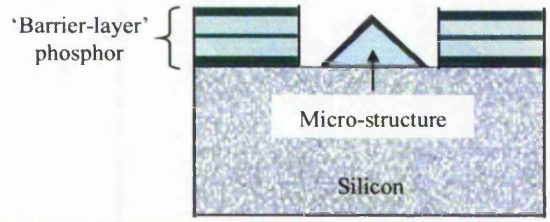
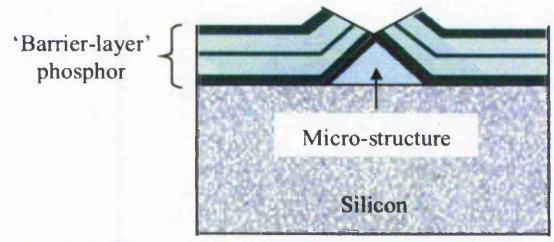
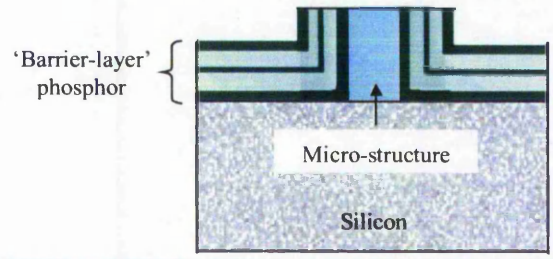
Outcoupling Mechanism	**Device Structure**	**Coupling Efficiency**
Conventional Non-Etched LETFEL Device		7%
Etched Aperture mmLETFEL Device (with 45° micro-structures)		12%
Open-ended mmLETFEL surface edge-emitter (with 45° micro-structures)		7%
Open-ended vmLETFEL surface edge-emitter (with 90° micro-structures)		*30%*

Table 6-1: Illustration of the various outcouplers and their corresponding coupling efficiencies.[64]

6.4 PROPOSED PROCESSING SEQUENCE FOR OEIC DEVELOPMENT

With new results obtained in this thesis, a processing sequence becomes feasible to include and incorporate these findings for an integrated mmLETFEL device with corresponding electronic driver. This includes incorporating laser annealing, thus avoiding the thermal annealing step that has been necessary previously, and also allowing for the possibility of utilising Al material as the base electrode instead of PolySi and/or TiW. At the same time vertical micro-mirrors may be incorporated as a standard device feature of the LETFEL device once these structures have been fabricated, tested and characterised in future.

The following table lists the possible processing sequence that is feasible for an integrated mmLETFEL test device for the development of an OEIC in the near future. The proposed fabrication steps that differ from previous mmLETFEL processing route have been highlighted accordingly in **Table 6-2.**

Process No.	Process Step/Name	Location	Technique/ Other Info.	Description
1a	Insulating material deposition	NMRC	Thermal Oxidation	5,000Å of T_{OX}
1b	Insulator definition	NMRC	Mask CP01	
1c	Insulator formed	NMRC	Plasma Etching	
2a	**Base electrode material deposition**	**TNTU**	**Sputtering**	**3,000Å of Al**
2b	**Base electrode definition**	**TNTU**	**Mask CP02**	
2c	**Base electrode formed**	**TNTU**	**Plasma Etching**	
3a	Micro-structures material deposition	Qudos, RAL	PECVD	15,000Å of SiO_2 45° angle, 1.5μm height, 3μm width
3b	Micro-structures definition	Qudos, RAL	Mask CP03	
3c	Micro-structures formed	Qudos, RAL	Plasma Etching	
4	'barrier-layer' mmLETFEL material deposition	TNTU	r.f. magnetron sputtering	3kÅ/8kÅ/3kÅ Y_2O_3/ZnS:Mn/Y_2O_3 with a 'barrier-layer' of 100Å Y_2O_3

6a	First level metallisation deposition	Qudos, RAL	d.c. magnetron sputtering	Tri-layer 1,500Å/2,500Å/1,500Å TiW/Al/TiW
6b	Sacrificial Mask deposition	Qudos, RAL	PECVD	2μm SiO_2
6c	Sacrificial Mask/First level metallisation definition	TNTU	Mask CP06	Tri-layer 1,500Å/2,500Å/1,500Å TiW/Al/TiW 2μm SiO_2
6d	First level metallisation formed	Qudos, RAL	RIE	Tri-layer 1,500Å/2,500Å/1,500Å TiW/Al/TiW
7	Aperture profile and contact definition	CMF, RAL	Ion Milling (Same Mask)	4μm aperture width
8a	Passivation layer deposition	Qudos, RAL	PECVD	3,000Å Si_3N_4
8b	Passivation layer definition	TNTU	Mask CP07	
8c	Passivation layer formed	Qudos, RAL	RIE	
9a	Second level metallisation	Qudos, RAL	d.c. magnetron sputtering	5,500Å of Al
9b	Second level metallisation definition	Qudos, RAL	Mask CP09	
9c	Second level metallisation formed	Qudos, RAL	RIE	

Table 6-2: Proposed processing sequence incorporating new features for an vmLETFEL device

Also, further discussion with Alcatel Mietec can be made to further establish the processing sequence of their NDMOSHV model technology for fabrication of test dies on Si wafer, and consequently incorporate the deposition of the mmLETFEL technology within the same die dimension. The design layout of the optimised drive circuitry based on the SPICE simulations can be made via collaboration with EuroPractice. The test wafers obtained can be used for mmLETFEL, and eventually vmLETFEL, test devices to be deposited onto the drain of the corresponding NDMOSHV driver.

6.5 FUTURE WORK

The eventual aim of this research is to build an integrated mmLETFEL linear bar array for use in electrophotographic printing application. Thus, for further assessment, a print-head array consisting of the mmLETFEL device with its corresponding driver circuitry is to be built and assembled within a typical "laser" printer following the feasibility investigation conducted thus far.

In order to aid in the progress of this ultimate objective, the following is a list of proposed future work for further research to be undertaken in realising the final phase of an OEIC development.

1. Design of the optimised drive circuitry layout through collaboration with Alcatel Mietec, thus facilitating the development of the integrated pixel – where the drive circuitry and the mmLETFEL pixel is defined and deposited within the same die dimension as the NDMOSHV device. This includes fabrication and characterisation of the fully integrated mmLETFEL pixel.

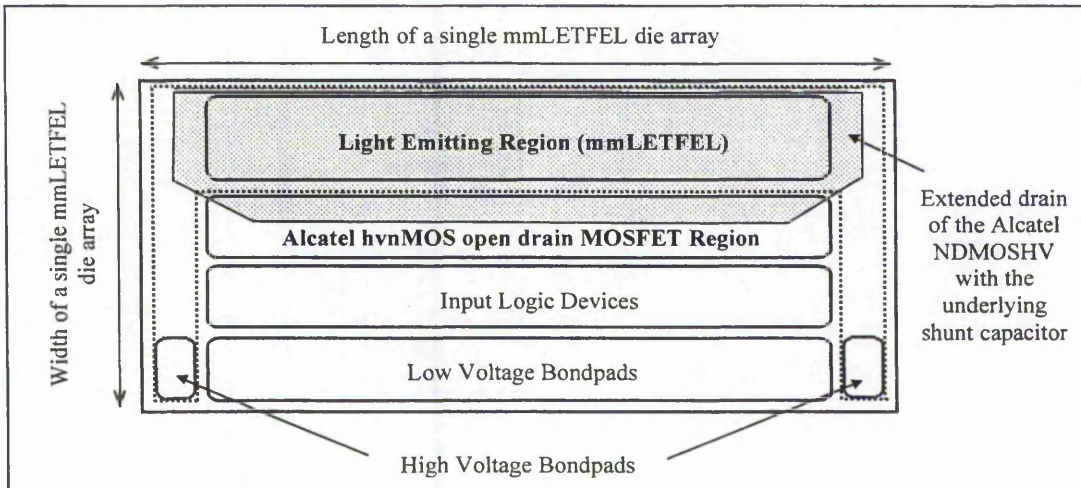


Figure 6-1: Plan view of an integrated mmLETFEL device with Alcatel NDMOSHV driver, and input logic devices

Figure 6-1 shows a sketch of the mmLETFEL die array that is possible to be designed and fabricated, but which requires further detailed discussion with Alcatel Mietec on the overall design, die size, chip layout, and possible constraints, and any other limitations of their technology, such as cost. Due to commercial sensitivity, these details have not been forthcoming, and future collaborations might help bring this to light, hence enabling the mmLETFEL integrated device technology to proceed and develop.

However, by using the general schematic layout diagram of a typical NDMOSHV device using the Alcatel Mietec I2T design rules,[128] a proposed physical layout of the integrated mmLETFEL can be realised, as shown in **Figure 6-2**.

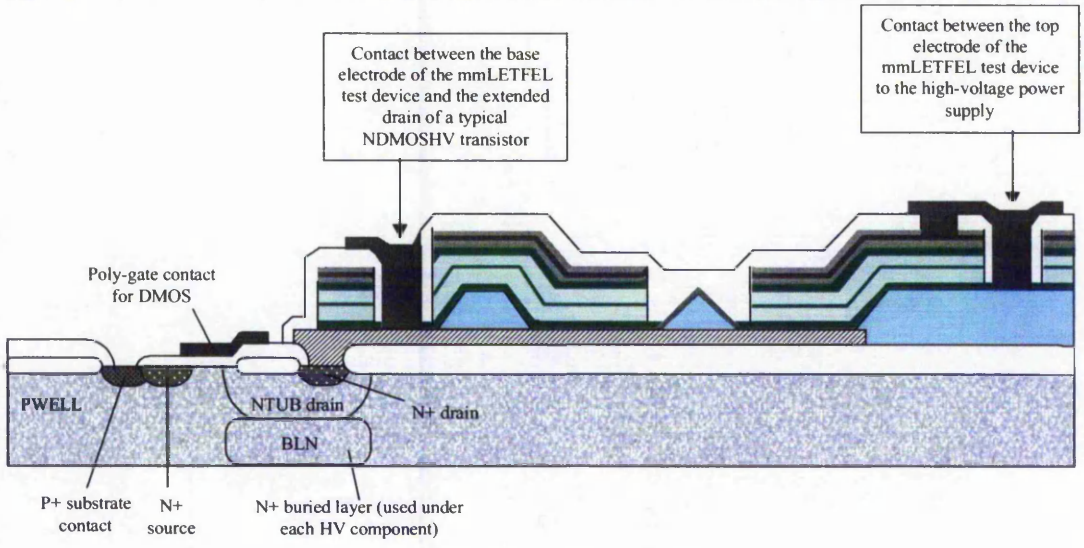


Figure 6-2: Proposed physical layout of the integrated mmLETFEL device

2. Investigation into the process sequence for a different LETFEL test device as proposed in the previous section; i.e. incorporating the vertical micro-structures for lateral wave-guiding of the internally generated light into the outside media, incorporating the Al as the base electrode material, and utilising laser annealing in replacement of the conventional thermal annealing. This includes fabrication and characterisation of the vmLETFEL test devices produced.

3. Further improvement to the existing model can be achieved by detailed characterisation of the interface states that are prevalent in the thin-film LETFEL stack. This leads to an enhanced model of the equivalent circuit, and better understanding of the mechanism of such devices. The improvement to the basic LETFEL SPICE model can be implemented for both mmLETFEL and vmLETFEL test devices as and when they are fabricated and characterised. This, in turn, helps in a more accurate determination of the electrical properties, in particular the power consumption, of the mmLETFEL circuit when simulated as an array of devices as intended for the electrophotographic printing application.

4. Lifetime and reliability studies on asymmetric drive of mmLETFEL test devices would be useful, facilitating an understanding of how this might influence the performance of the devices after a long period of continuous operation at this condition.

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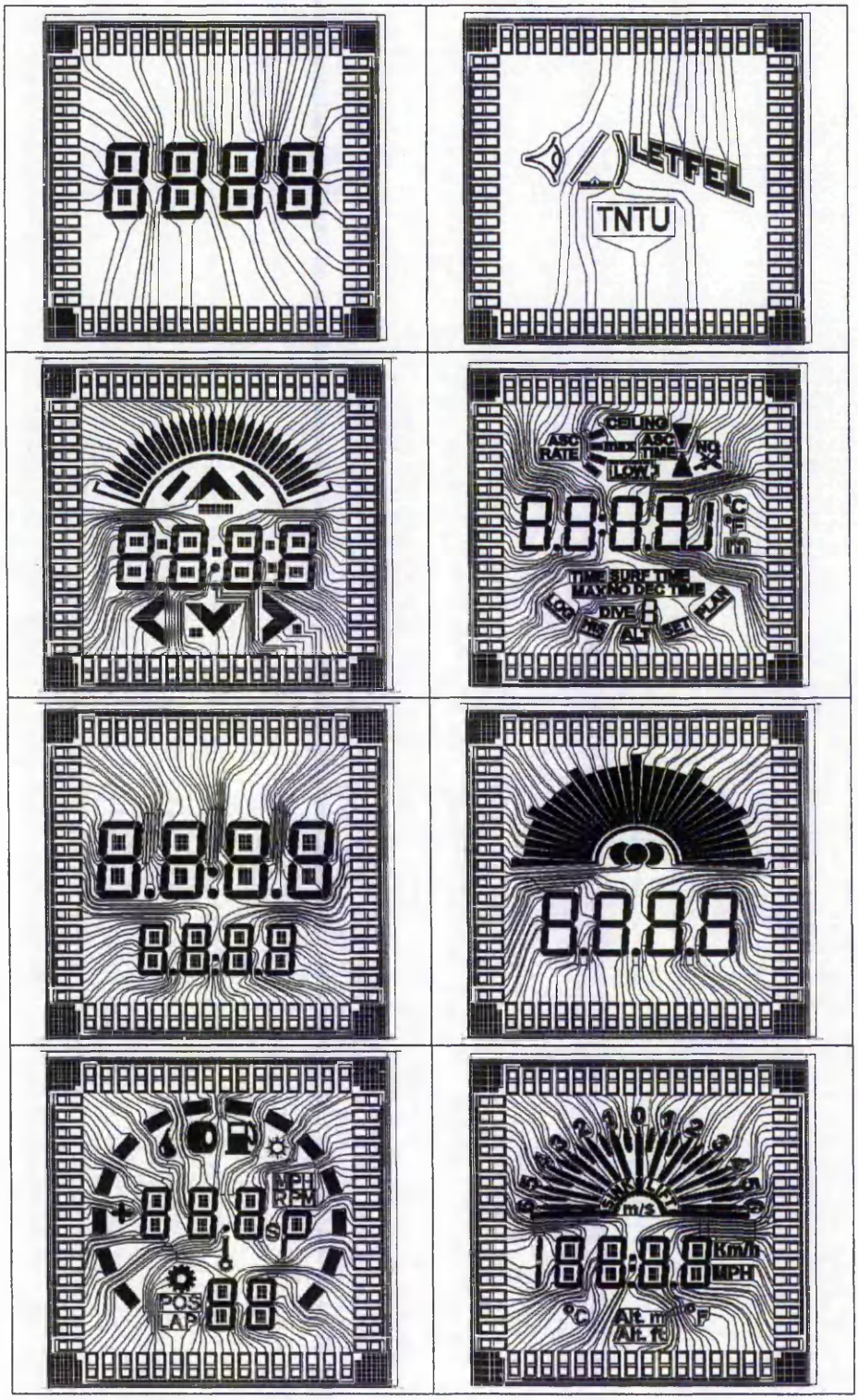
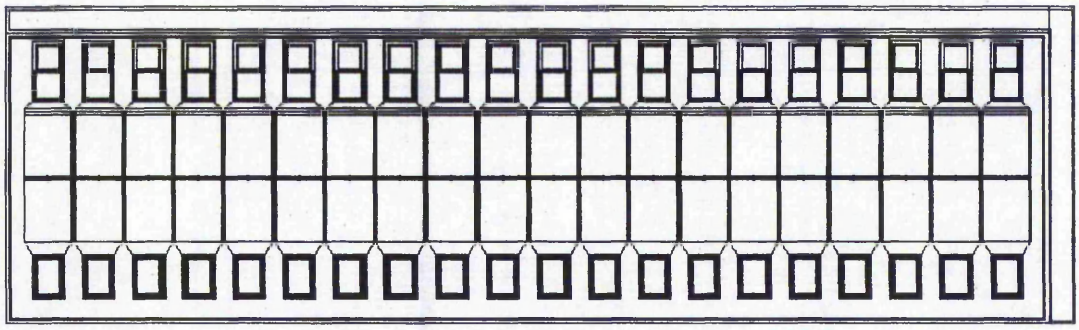
List of Appendices

Appendix A

A1 MASK SET 3: SMALL-AREA DISPLAY DEVICES (4 mm x 4 mm)



A2 MASK SET 3: LINEAR-ARRAY DEVICES (4.1 mm x 1.2 mm)



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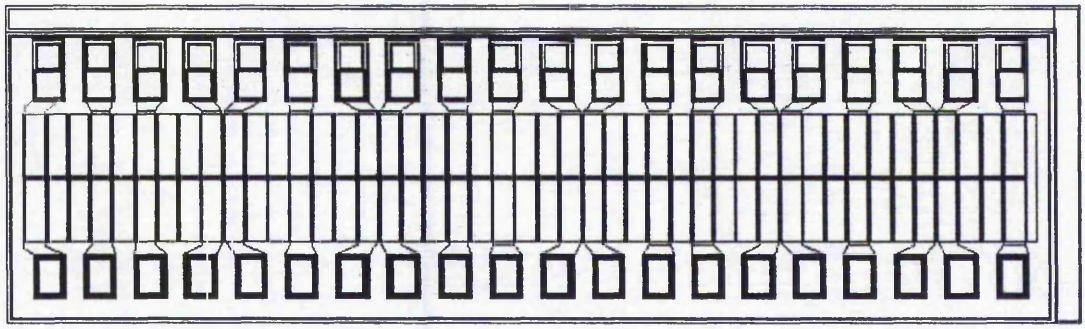
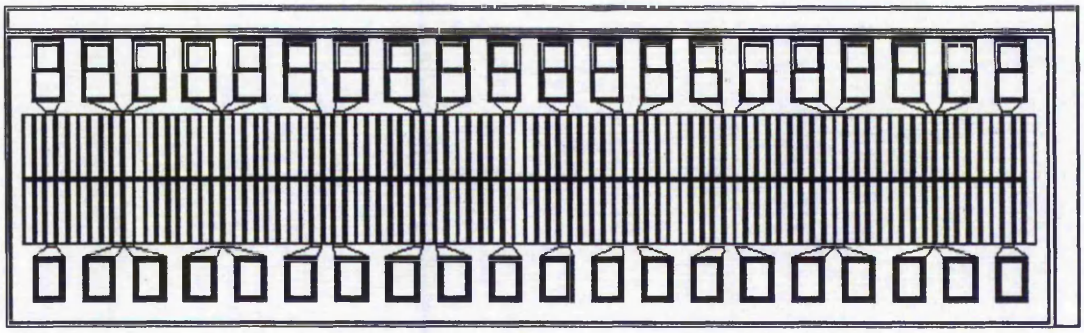
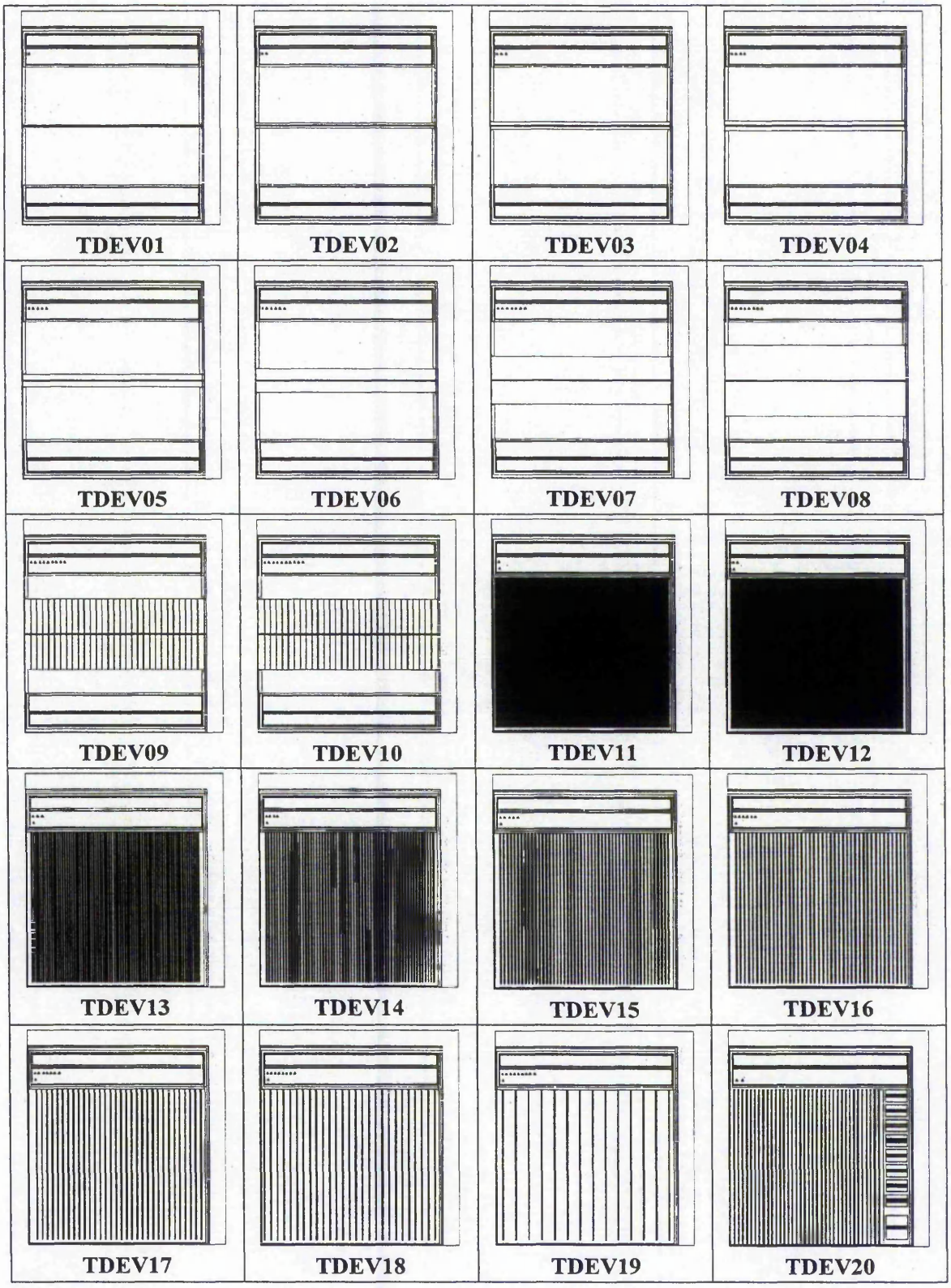


Resolution: 300d.p.i.

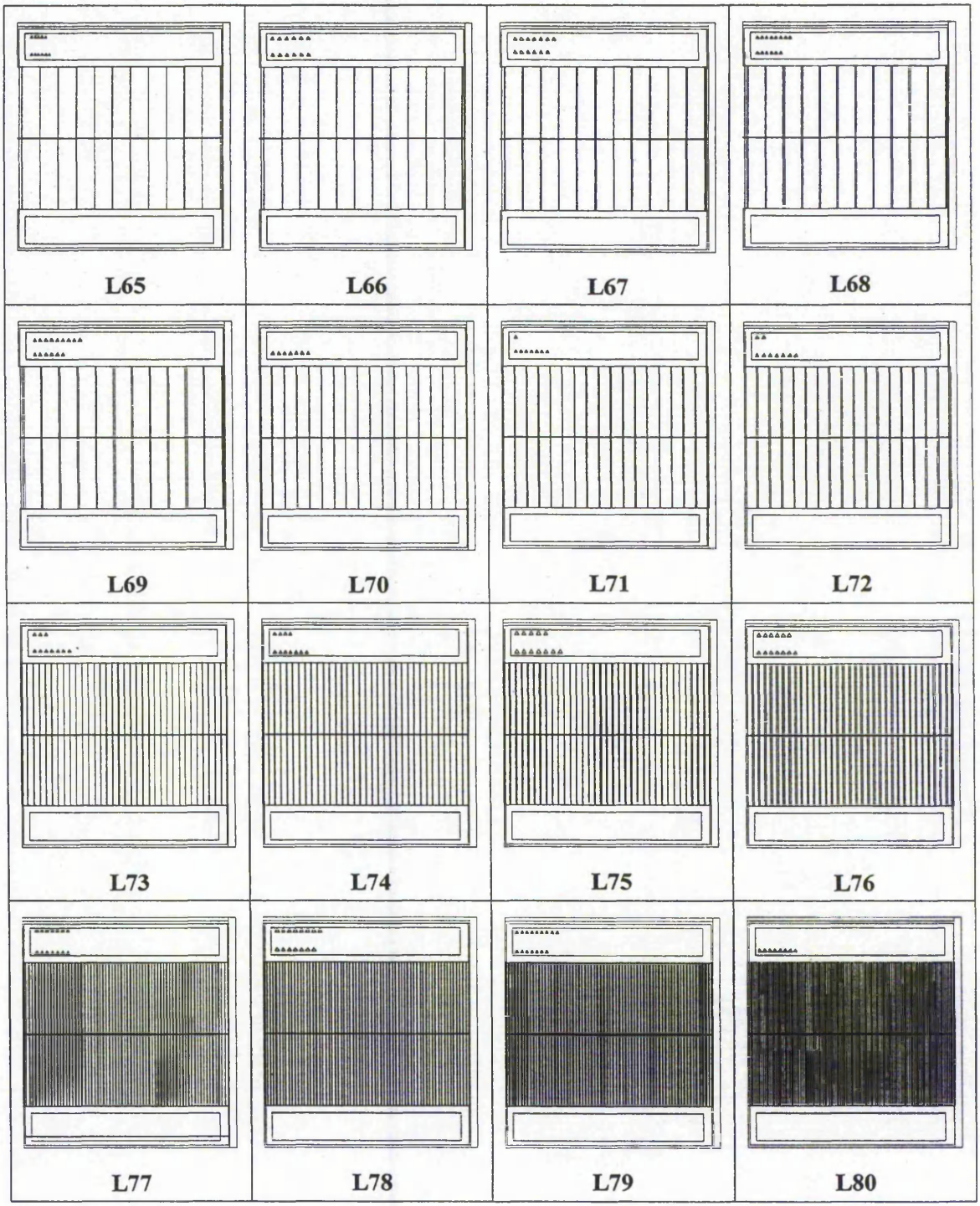


Resolution: 600 d.p.i.

A3 MASK SET 3: TEST DEVICES (1.8 mm x 1.6 mm)



A4 MASK SET 2: TEST DEVICES (1.7 mm x 1.5 mm)



Appendix B

B1 DICING OPERATION

mmLETFEL test devices were cut into individual devices using a dicing saw from Sola Basic Tempress, Model 602 at TNTU. The wafer was first coated with a layer of photoresist prior to the dicing operation, to prevent tiny pieces of chipped silicon material, i.e. edge-chipping caused by the cutting operation, to be lodged within the grooves of the active devices, thus damaging the devices. The wafer was then placed on a piece of adhesive tape which was held together by two ring-clasps, and this unit was then positioned on a metallic plate, connected to a vacuum pump, in the system. The dicing blade was mounted on the spindle, and only replaced until after the exposed cutting blade was consumed. While the wafer was being diced, water was automatically fed via the system and injected at a constant rate to act as a coolant to the heat that was generated during the sawing operation. Excess water was drained using a hose from the back of the system to a water vessel trap and which in turn had to be drained ensuring that there is no back-flow of water to the system.

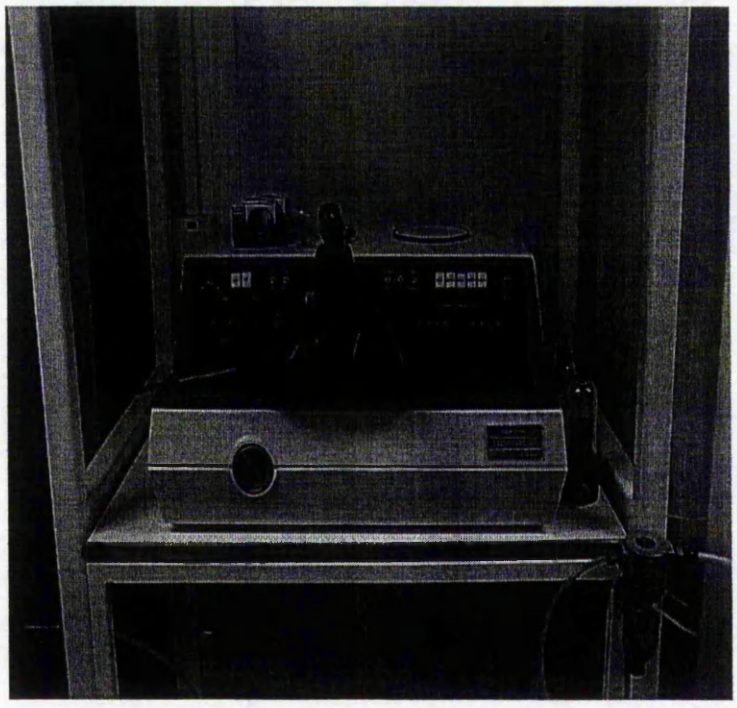


Figure B1-1: The diamond saw machine utilised for dicing of mmLETFEL devices

The system is shown in **Figure B1-1**. After the sawing operation, the photoresist was removed using acetone, and the die stored individually.

There are two types of cutting operations. The 'Scribe' operation allows cuts to be made in both directions. The first cut is made when the blade is lowered to the specified depth (z-axis) and makes its way across the wafer (x-axis), after which the blade then increments at a specified index value (y-axis) to the next street of devices to be cut. The second cut is then made when the blade is again lowered to the required depth as specified before and makes its way back to the initial horizontal position, after which it increments again at the specified index value (y-axis), and proceeds to make the next cut.

The 'Dice' operation, however, allows only one cut in the same direction. In this case, after the first cut has been made (as described in the first half of the 'Scribe' operation above), the blade is not lowered to the specified depth (z-axis), i.e. the blade remains suspended above the wafer, while it returns to its initial horizontal position. Thus no cut is made during this movement. The blade will then increment at the specified index value (y-axis) to the next street of devices to be cut, lowers to the required depth as specified before, and then proceeds with the second cut, but in the same direction as the first cut.

In all dicing operations of the mmLETFEL devices, the cutting method utilised was 'Dice'. Although the latter operation consumed twice the time needed to dice a full wafer, however this produced better quality cuts. This is because the rotation of the blade is always kept in one direction, i.e. anti-clockwise, thus by subjecting the cuts to be made to only one direction, it reduces the inconsistency observed when cuts are made in opposing directions. **Figure B1-2(a)** through **Figure B1-2(c)** illustrates these two types of sawing operation, and their significance to the quality of the cut made on the devices.

Depending on the type of base wafer used, its thickness, and the kerf widths required, a precision hubbed diamond dicing blade, series S1430 with a 4-6μm diamond grit, manufactured by Dynatex International, was selected. The blade exposure at 762-889μm allows for a total thickness of a typical test wafer with base electrodes on Si at (525 ± 50) μm, where the mmLETFEL test devices constitute (2.05 ± 0.2) μm. It also allows for the wearing down of the cutting blade to accommodate more cuts before it is discarded, lasting for at least two wafers. The blade thickness at 30-36μm allows for the required kerf width at ≈50μm. **FigureB1-2(d)** illustrates the dimensions related to the diamond dicing blade used.

Through many experimentation and calibration of the system, the suggested dicing parameters are tabulated below:

Dicing Parameters	Parameter Settings
'Spindle' lever	'Dice' and '4'
'Speed' indicator	'Lo' and '10'
'Ref' indicator	'0080' (i.e. 80μm)

Table B1-1: List of suggested dicing parameters to be used for the dicing operation

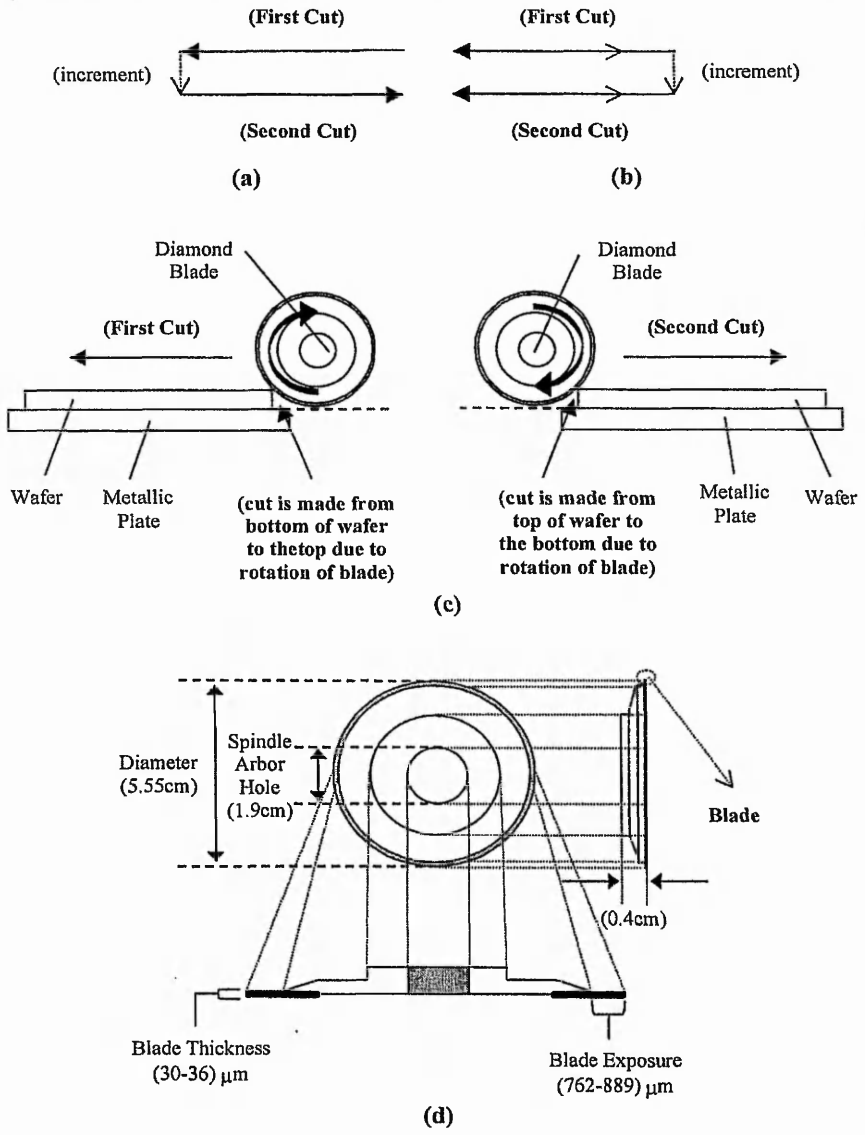


Figure B1-2: (a) 'Scribe' operation (b) 'Dice' operation (c) Illustration of the sawing operation and its significance when cuts are made in opposing directions (d) Illustration of related dimensions of a diamond dicing blade

B2 DIE ATTACH

After the dicing, the dies were attached to individual ceramic chip carriers of 24-lead or 68-lead depending on the type of test devices or displays being wire-bonded, using silver conductive paint. Upon application of the silver epoxy, the chip carrier was left to dry in air for about 10 mins, before being placed in an oven or a hot plate and heat-cured for about 10 mins at a temperature between 121°C - 148°C (250°F - 300°F). This procedure ensures good adhesion of the die to the ceramic chip carrier.

B3 WIRE-BONDING OPERATION

Wire-bonding of the mmLETFEL test devices was performed using the K&S Wedge-Bonder, Model 4123. A MicroSwiss Tungsten Carbide wedge was used with a gauge height of 0.75 inches, which was best for 1.0 mil Al wire (1% Si) with 1-4% elongation and breaking load of 17-19 gr. **Figure B3-1** shows the wedge-bonder used at TNTU.

The wire-bonding procedure is affected by several bonding parameters. These bonding parameters are set by the dials on the wedge-bonder. The Bonding Power dial regulates the ultrasonic power level, and represents the amount of energy applied to the bond. High power setting increases the ultrasonic vibration amplitude, and vice-versa for a low power setting. The Bonding Time dial regulates the duration of the ultrasonic energy and bonding force pulse applied. The Bonding Force dial regulates the downward force exerted by the wedge on the wire while the ultrasonic energy is being applied. This force is the sum of the static force of the Bonding Head (which is set by counter-weights on the armature), and the dynamic force applied by the electromagnetic Force Actuator. The Bonding Force dial controls only the dynamic force. The Search dial regulates the height of the Bonding Head in the Search position. This height is the height above the bonding surface at which the wedge stops prior to performing bonding, and this pause allows for alignment of the bonding pad with the wedge tip.

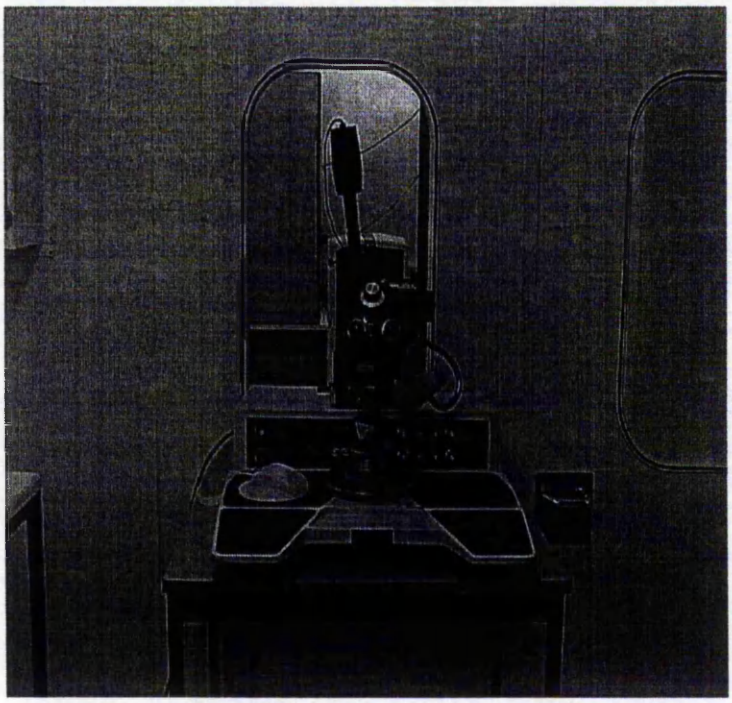


Figure B3-1: The wedge-bonder utilised for wire-bonding operation of mmLETFEL devices

Other important parameters affect the quality of the bonds made, i.e. the shape of the wire-bond. The Loop dial sets the height to which the wedge will rise after performing the first bond. The tail length and tear point adjustments are equally important in determining the tear stroke produced after each wire-bond is made. The tail length is adjusted by setting the Tail Solenoid and Tear Solenoid to the same stroke distance. And, by adjusting only the Tail Solenoid piston stroke, a gap difference between the Tail Solenoid and Tear Solenoid is created, thus establishing a Tear Stroke gap.

The bond strength depends on a few important main parameters such as:

1. metallisation, i.e. the adhesion of the die and substrate metals
2. wire type; its tensile strength and elongation
3. type of wedge
4. bonding parameter settings.

For different devices, and bonding surface materials, different bonding settings will be correspondingly different. However, the following table lists the suggested optimal bonding settings for the wire type of 1 mil Al wire used in this investigation, as mentioned earlier, as the initial starting point for the wire-bonding process to proceed.

Description of Parameters for wire-type of: 1.0 mil Al (1% Si) 1-4% elongation 17-19 gr breaking load	**Parameter Settings**
Static Bond Force	15 gr
Wire Clamp Gap	3-5 mil
Wire Clamp Force	80-100 gr
Tail Solenoid Gap (A)	30-40 mil
Tear Solenoid Gap (B)	60-80 mil
Tear Stroke Gap (C=B-A)	30-40 mil
Bonding Force	25-35 gr
Bonding Power (scale on dial)	***1-2***
Bonding Time (scale on dial)	***2-5***
Bonding Loop (scale on dial)	***2***
Bonding Search Height	***0.127 mm***

Table B3-1: List of suggested bonding parameters (in bold italics) to be used for the wire-bonding process to commence – while those parameters listed in regular font indicate the settings used by the manufacturer

Figure B3-2 illustrates an HMD optics mount and the view of a typical mmLETFEL display device viewed against a background.

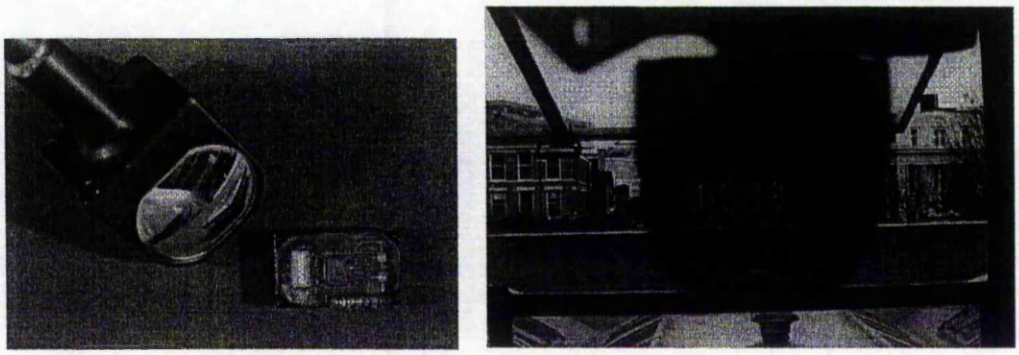


Figure B3-2: An HMD optics mount, and the view of a typical mmLETFEL display

Appendix C

C1 SPICE Model Parameters of Commercial Drivers from HOLTEK (Taiwan), UMC (Taiwan), and Supertex (U.S.A.)

SmartSpice MOSFET Model Level=3 Parameters	HOLTEK		UMC	SUPERTEX	
	HT1606 (V_{DD}=5V)	HT1607 (V_{DD}=28V)	28V Process	HV31 (V_{PP}=315V)	HV507 (V_{PP}=315V)
Device Size: L/W	-	-	3.5μm/100μm	10μm/600μm	8μm/200μm
TOX	$105e^{-9}$	$105e^{-9}$	$0.85e^{-7}$	$55e^{-9}$	$7.45e^{-8}$
NSUB	$6.643e^{+15}$	$7.945e^{+15}$	$1.5e^{+16}$	$21.64e^{+15}$	$9.162e^{+15}$
GAMMA	-	-	-	1.349947	-
PHI	-	-	-	0.735366	-
VTO	$885.8e^{-3}$	1.2	0.8	0.6982	0.4013
UO	805.7	718.1	670	581.2	714.9
VMAX	$191.2e^{+3}$	$132.2e^{+3}$	$3.6e^{+4}$	$920e^{+3}$	$1e^{+6}$
THETA	$28.64e^{-3}$	$12.61e^{-3}$	0.02	0.01432	0.03036
ETA	$233.3e^{-3}$	1	0.07	0.02485	0.01
KAPPA	$493.8e^{-3}$	$93.37e^{-3}$	0.005	$1.384e^{-6}$	0.01
DELTA	0	0	0	0.2572	0.3779
KP	-	-	-	$36.49031e^{-6}$	-
RD	47.92	51.21	320	15.725	350
RS	47.92	51.21	320	59.58333	75
RSH	20	20	-	100	6000
IS	-	-	-	$10e^{-15}$	$1e^{-14}$
NFS	$282e^{+9}$	$428.9e^{+9}$	$3.5e^{+11}$	$433.5e^{+9}$	$1.554e^{+11}$
TPG	-	-	1	-	-
XJ	$890.2e^{-9}$	$4.084e^{-6}$	$1.2e^{-6}$	$5.35e^{-6}$	$6.97e^{-7}$
LD	$2.315e^{-6}$	$3.262e^{-6}$	$0.75e^{-6}$	$555.9e^{-9}$	$1e^{-6}$
WD	$-1.527e^{-6}$	$-4.067e^{-6}$	$0.8e^{-6}$	-	-
CGDO	$0.42e^{-9}$	$0.52e^{-9}$	$3.12e^{-10}$	$3.79e^{-9}$	$1.344e^{-9}$
CGSO	$0.42e^{-9}$	$0.52e^{-9}$	$3.12e^{-10}$	$17.4e^{-9}$	$447.6e^{-12}$
CJ	$210.9e^{-6}$	$114.6e^{-6}$	$2.36e^{-4}$	$38.4e^{-6}$	$4.745e^{-5}$
VJ (PB)	$770e^{-3}$	$619.8e^{-3}$	0.71	1.1	0.5582
MJ	$454.5e^{-3}$	$390.4e^{-3}$	0.43	1.7	0.4608
FC	-	-	0.5	0.4	0.5
CJSW	$1.149e^{-9}$	$1.213e^{-9}$	$3.5e^{-10}$	$1.651e^{-9}$	$3.56e^{-10}$
VJSW (PBSW)	-	-	-	1.1	-
MJSW	$316.7e^{-3}$	$292.2e^{-3}$	0.4	0.2	0.07

C2 SmartSPICE n-channel MOSFET Model Level=3 Parameters (corresponding descriptions of model parameters in Appendix C1)

SmartSpice MOSFET Model Level=3 Parameters	Description	Units	Default Values
TOX	Oxide Thickness	m	$1.0e^{-7}$
NSUB	Substrate Doping	cm^{-3}	$1.0e^{+15}$
GAMMA	Bulk Threshold Parameter	$V^{0.5}$	-
PHI	Surface Potential	V	-
VTO	Zero-Bias Threshold Voltage	V	0
UO	Bulk Mobility	cm^2/Vs	600
VMAX	Maximum Drift Velocity of Carriers	ms^{-1}	0
THETA	Mobility Modulation	-	0
ETA	Static Feedback	-	0
KAPPA	Saturation Field Factor	-	0.2
DELTA	Narrow Width Threshold Adjusting Factor	-	0
KP	Transconductance Parameter	AV^{-2}	$2.0e^{-5}$
RD	Drain Ohmic Resistance	Ω	0
RS	Source Ohmic Resistance	Ω	0
RSH	Sheet Resistance	Ω/sq	0
IS	Bulk Junction Saturation Current	A	$1.0e^{-14}$
NFS	Fast Surface State Density	cm^{-2}	0
TPG	Type of Gate Material (+1 opposite to substrate, -1 same as substrate, 0 Al gate)	-	1
XJ	Metallurgical Junction Depth	M	0
LD	Lateral Diffusion for Length	M	0
WD	Lateral Diffusion for Width	M	0
CGDO	Gate-Drain Overlap Capacitance	Fm^{-1}	0
CGSO	Gate-Source Overlap Capacitance	Fm^{-1}	0
CJ	Zero-Bias Area Capacitance per Junction Area	Fm^{-2}	0
VJ (PB)	Bottom Junction Built-in Potential	V	0.75
MJ	Bottom Junction Bottom Grading Coefficient	-	0.33
FC	Forward-Bias Depletion Junction Capacitance Coefficient	-	0.5
CJSW	Zero-Bias Sidewall Capacitance per Junction Perimeter	Fm^{-1}	0
VJSW (PBSW)	Sidewall Junction Built-in Potential	V	0.75
MJSW	Sidewall Junction Grading Coefficient	-	0.33

C3 SPICE Model Parameters of NDMOSHV model (for the principal transistor) from Alcatel Mietec (Belgium), and corresponding descriptions of model parameters in SmartSPICE MOSFET Model Level=2 parameters.

SmartSpice MOSFET Model Level=2 Parameters	Description	Units	Default Values	Alcatel Mietec 100V Process
Device Size: L/W	Dimensions of the device size, i.e. the device length and width	μm	-	5μm/ 40μm
TOX	Oxide Thickness	m	$1.0e^{-7}$	$4.25e^{-8}$
NSUB	Substrate Doping	cm^{-3}	$1.0e^{+15}$	$3.5e^{+16}$
VTO	Zero-Bias Threshold Voltage	V	0	0.96
DELTA	Narrow Width Threshold Adjusting Factor			6.305
UO	Bulk/Surface Mobility	cm^2/Vs	600	587
UCRIT	Critical Field of Mobility Degradation	Vcm^{-1}	$1.0e^{+4}$	$108e^{+3}$
UEXP	Critical Field Exponent in Mobility Degradation	-	0	0.124
LAMBDA	Channel-Length Modulation	V^{-1}	0	$1e^{-6}$
RSH	Sheet Resistance	Ω/sq	0	813
JS	Bulk Junction Saturation Current per unit Area	Am^{-2}	0	$1e^{-3}$
LD	Lateral Diffusion for Length	m	0	$6.3e^{-7}$
XL	Masking and Etching Effects on L	m	0	0
XW	Masking and Etching Effects on W	m	0	0
CAPMOD	Capacitance Model Selector	-	2	2
CJSW	Zero-Bias Sidewall Capacitance per Junction Perimeter	Fm^{-1}	0	$2.8e^{-10}$
MJSW	Sidewall Junction Gradient Coefficient	-	0.33	0.21
NLEV	Noise Model Selector	-	0	0
TEMPLEV	Temperature Model Selector	-	0	1
TCV	Threshold Voltage Temperature Coefficient	V/K	0	$2.53e^{-3}$

Appendix D

D1 Glossary of Components terms, Model names and Node names used in SmartSPICE Simulations

Component names and descriptions

Vexc	Excitation Voltage applied across the pixel structure
Vm	Gate Voltage applied to the MOSFET model
M1	Commercial MOSFET model
Md	Alcatel NDMOSHV macro-model (nMOS at drain)
Ms	Alcatel NDMOSHV macro-model (nMOS at source)
D1 & D2	Zener diodes used to model mmLETFEL device breakdown
Dm	Diode across the commercial nMOSFET model
Dd	Alcatel NDMOSHV macro-model (diode at drain of nMOS)
Ds	Alcatel NDMOSHV macro-model (diode at source of nMOS)
Ri1 & Ri2	Resistance of the insulator layer
Rp	Resistance of the phosphor layer
Rz	Resistance of zener diodes D1 & D2
Rm	Resistance of bottom electrode (PolySi, or TiW)
Re	Resistance of top electrode (Al or tri-layer electrode i.e. TiW/Al/TiW)
Rc	Series resistance used for simulating I-V characteristics
Rd	Alcatel NDMOSHV macro-model (resistor at drain of nMOS)
Rs	Alcatel NDMOSHV macro-model (resistor at source of nMOS)
Ci1 & Ci2	Capacitance of the insulator layer
Cp	Capacitance of the phosphor layer
Cc	Series capacitance used for simulating Q-V characteristics
Csh	Shunt Capacitance of MOSFET model

Model Names

nch	Commercial nMOSFET model
ndmoshvd	Alcatel NDMOSHV macro-model (nMOS at drain)
ndmoshvs	Alcatel NDMOSHV macro-model (nMOS at source)
diodez	Zener diodes used to model mmLETFEL device breakdown
diode	Diode across the commercial nMOSFET model
dhcgs	Alcatel NDMOSHV macro-model (diodes at drain and source of nMOS)

D2 An example of a SmartSPICE Deck File for an mmLETFEL device, including top and base electrodes (with values given arbitrarily)

***mmLETFEL TDEV11**

***Circuit Netlist**

```
Vexc  1 0 sin(0 250 5k)
Re    1 2 100
Ri1   2 3 1.854e10
Rp    3 6 1.456e12
Ri2   6 7 1.854e10
Ci1   2 3 4.367e-10
Cp    3 6 1.123e-10
Ci2   6 7 4.367e-10
D1    3 4 diodez
D2    5 4 diodez
Rz    5 6 100
Rm    6 7 15

*Rc   7 0 1K
*for I-V characterisation
*Cc   7 0 9e-9
*for Q-V characterisation
```

***SPICE Model and Control list**

```
.MODEL diodez D (level=3 BV=115)
.TRAN 10n 0.3m 0
.END
```

D3 An example of a SmartSPICE Deck File for commercial drivers, in this case the Alcatel Mietec NDMOSHV model provided via EuroPractice.

***Alcatel Mietec NDMOSHV model**

***Circuit Netlist**

```
Dd 0 10 dhcgs 0.852408
Ds 0 5 dhcgs 0.094712
Rd 10 3 386.667 tc=0.00747,0
Rs 0 5 1e+09
Md 10 4 5 5 ndmoshvd w=0.00012 l=1e-06 ad=3e-10 as=3e-10
+ pd=0.000245 ps=0.000245 nrd=0.0116667 nrs=0.0116667
Ms 5 4 0 0 ndmoshvs w=0.00012 l=5e-06 ad=3e-10 as=3e-10
+ pd=0.000245 ps=0.000245 nrd=0.0116667 nrs=0.0116667
```

***SPICE Model and Control list**

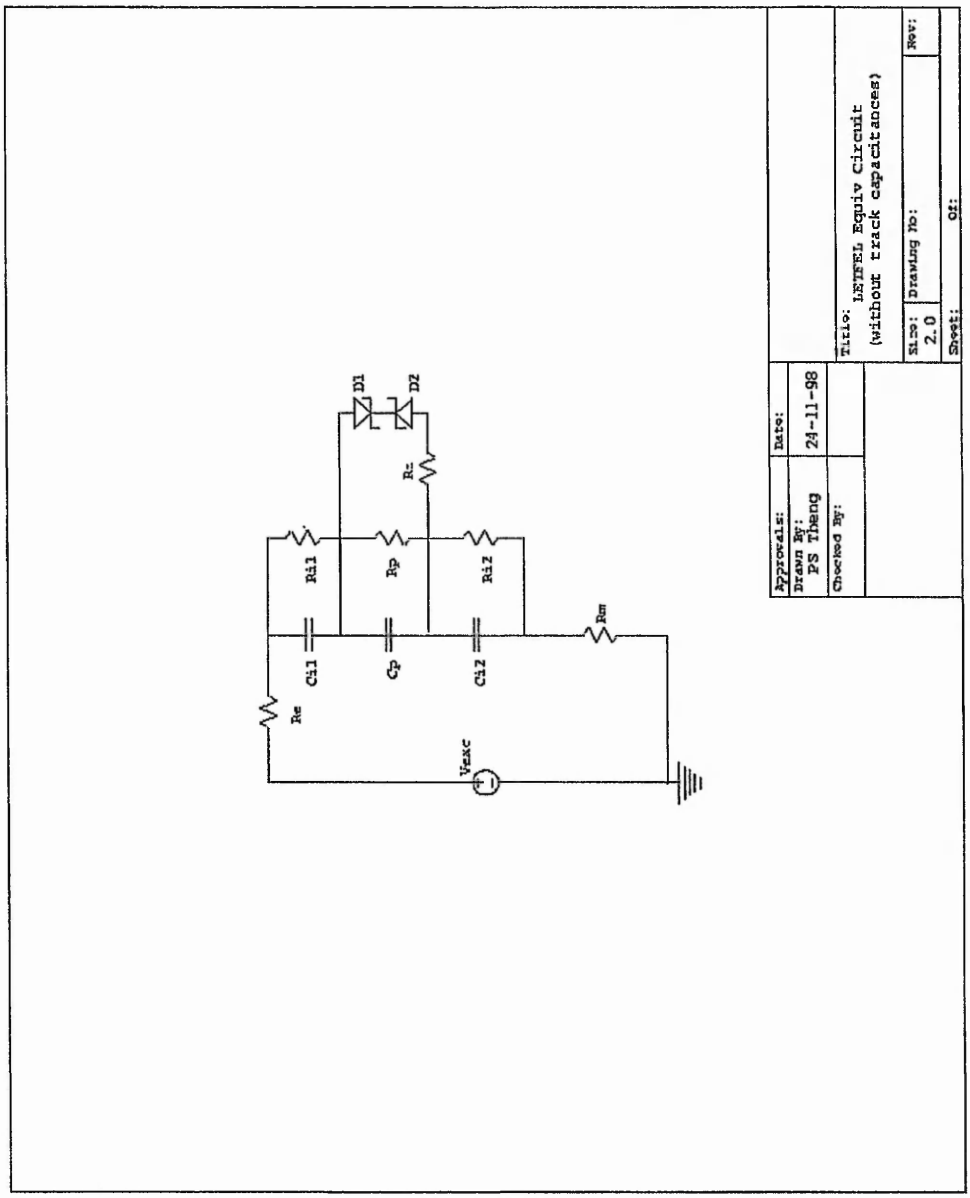
```
.MODEL ndmoshvs NMOS (level=2
+ tox=4.25e-08      vto=0.96          nsub=3.5e+16
+ uo=587            ucrit=108000      uexp=0.124
+ rsh=813           lambda=1e-06      ld=6.3e-07
+ delta=6.305       cgso=1.647e-10    cgdo=1e-14
+ cj=0.0005         mj=0.35           pb=0.73
+ cjsw=2.8e-10      mjsw=0.21         js=0.001
+ lis=2             istmp=10          ienh=2
+ capmod=2          tcv=0.00253       xl=0
+ xw=0              nlev=0            templev=1)

.MODEL ndmoshvd NMOS (level=1
+ tox=4.25e-08      vto=-0.48         nsub=1.45e+11
+ kp=6.7e-06        lambda=1e-06      lis=2
+ istmp=10          capmod=2)

.MODEL dhcgs D (
+ is=1e-16      cjo=1e-12      vj=1.079      m=0.39)
```

Appendix E

E1 Circuit diagram used to represent the mmLETFEL device in SmartSPICE Simulations



E2 Circuit diagram used to represent the integrated mmLETFEL device in SmartSPICE Simulations