MEMORY PERFORMANCE of MOS STRUCTURE EMBEDDED with LASER ANNEALED GOLD NCs

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Abstract

Memory devices having the structure of n-Si(100)/SiO_2/metal nanocrystals(NCs)/Y_2O_3/Au were fabricated and their structural and electrical characteristics have been studied extensively. Gold nanoparticles were formed via laser annealing (LA) of a thin Au layer. The aim was to investigate the use of laser annealing as an effective method to produce NC-based memory devices. In particular, laser annealing was used in order to obtain uniformly spaced NCs with an average diameter of 20 nm. Best results for Au NCs were obtained using fluence below 500 mJ/cm^2 and a small number of laser pulses (1-5). After structural characterization using SEM, electrical characterization involving capacitance-voltage and current-voltage measurements revealed good (dis-)charging behavior and memory windows around 3 V. The analysis of the experimental data showed that LA is a promising annealing technique to realize devices with electrical characteristics suitable for future memory devices.

Keywords

Nonvolatile memory; metal nanocrystals; Laser Annealing; metal nanoparticles.

Introduction

Flash memory is widely used in modern portable electronics, allowing large storage capabilities for very small scale structures The core of these memories is formed of cells

containing floating gate devices, where leakage phenomena as well as structural defects deteriorate the device performance. For example, reducing the scale of the memory cell, conventional poly-silicon floating gate flash memories are facing a severe challenge that the thinner tunneling oxide will degenerate retention characteristics due to leakage current. The use of NCs inside the floating gate oxide has been proposed as a promising method in increasing the device performance and, since the first nanocrystal (NC) memory device was proposed [1], such configurations have been extensively studied as candidates for future generation nonvolatile memory (NVM) devices. Methods of fabricating such devices have been realized by means of sputtering [2,3], CVD [4] and Atomic Layer deposition (ALD) [5,6], while subsequent thermal annealing is used to achieve good uniformity and density of the NC formation. For annealing, both the Rapid Thermal Annealing (RTA) [7] and the Laser Annealing (LA) [8,9] methods have been used, with the latter being a promising technique because it offers a high degree of control of the metal NCs formation while having the advantages of defect minimization in the oxide or at the NC-oxide interfaces. Moreover, laser annealing can produce metal NCs under the surface of the gate oxide providing further versatility and defect control [10].

The metal NCs are often used because they do offer the advantages of higher programming/erasing (P/E) efficiency, lower operating voltage and wide range of work functions [11,12]. When compared to semiconductor NCs, metal NCs having a small work function are used to produce high speed write-erase memories, while metal NCs having a large work function are used to produce lower speed write-erase memories with a larger charge capacity and a higher retention time [11]. Metal NCs with a large work-function, such as platinum (Pt), silver (Ag) and gold (Au) [12] are preferable materials due to the deep potential wells they create. Moreover, they have greater density of states around the Fermi level, hence they are less affected by the introduction of impurities during doping. The change of the Fermi energy in metal NCs is negligible compared to the Fermi level of the respective bulk material, while semiconductor NCs present an enlarged energy gap relative to the corresponding bulk semiconductor. Therefore, the use of metal NCs is still considered as a promising choice for future non-volatile memories. However, the post deposition annealing treatment is still an open issue and the optimum conditions for Laser Annealing is an interesting topic that needs further exploration. Alternating oxide and particle layers can increase the particle density and

increase the trapped electric charges [13,14]. Also, very small particles below 1nm with high uniformity have been manufactured by sputtering [15].

In this work, gold (Au) nanocrystals were uniformly distributed at the interface between a blocking oxide (40 nm Y_2O_3) and a tunneling oxide (3.7 nm SiO_2), via LA of a thin Au film deposited on n-Si/SiO_2 substrates. A range of LA conditions was investigated. RF-magnetron sputtered Y_2O_3 was used as the blocking oxide layer. Finally, Au was deposited as the gate metal electrode to complete the n-Si/SiO_2/Au(NCs)/Y_2O_3/Au (MOS) structures. A Au electrode was also used as the back contact on the silicon wafer. Subsequently, the improvements in the memory cell performance were studied by means of electrical characterization.

Experimental

A 3.7 nm SiO_2 thin film was thermally grown (at 850 ^{o}C and 10 sccm O_2) on n-type Si (100) substrate (1–5 ohm·cm) as a tunnel oxide layer. On this dielectric layer a Au layer of nominal thickness of 5nm (at this thickness the metal is a discontinuous film) was deposited using a conventional RF-magnetron sputtering system. For comparison, devices without any metal NCs have also been co-deposited to be used as reference structures.

A LA step was then performed using a multipulse KrF excimer laser system (**Figure 1**), comprising a beam attenuator (with a reflecting plate and a compensator), a homogenizer (Exitech Ltd. Type EX-HS-700D), projection optics (field lens and projection lens at x5 magnification) while a computer controlled X-Y-Z stage was used to manipulate the sample and allow the laser to process different areas on its surface. By adjusting the attenuator, different fluences were achieved at the focus spot on the sample surface. Furthermore, the number of pulses was varied thus achieving uniformly dispersed nanoparticles with almost spherical shape. The laser spot delivered onto the samples was set, by an appropriate mask, to be a 2.5 × 2.5 mm^2. By varying the fluence (from 300 $mJ{\cdot}cm^{-2}$ to 600 $mJ{\cdot}cm^{-2}$) of the laser spot and the number of pulses (from 1 to 20 pulses), it was possible to control the density, uniformity and size of metal NCs [16]. Finally, a blocking oxide layer of Y_2O_3 with thickness of 40 nm was deposited by RF magnetron sputtering. MOS capacitors (with an area of 0.785mm^2) were defined by DC sputtering of Au gate electrodes using a shadow mask, while Au metal electrodes were used as back ohmic contacts. **Figure 2** shows the final structure of the complete MOS device.

The size and uniformity of the Au NCs were examined by means of Electron Microscopy (SEM). The electrical characteristics of the corresponding MOS devices such as capacitance-voltage (C-V) and capacitance-time measurements as well as Program/Erase (P/E) cycles were performed with an Agilent 4284A LCR meter at high frequencies (10 kHz to 100 kHz). The Current-Voltage (I-V) curves were measured using a Keithley 617 Electrometer together with a Keithley 230 voltage source. All measurements were performed at room temperature in a dark shielded probe station.

Results and Discussion

The procedure described in the previous paragraphs was used to produce a variety of memory devices, having the n-Si(100)/SiO_2/Au(NCs)/Y_2O_3 structure, with variable NC configurations because of the different treatment resulting from the various laser annealing parameters.

In **Figures 3(a,b,c,d)** the SEM images of the as deposited layer of gold as well as NCs fabricated via laser annealing with the same fluence (500 mJ·cm^{-2}) and 1, 5 or 10 laser pulses respectively are shown. The thin Au layer shows some island formation and a complete coverage of the SiO_2 surface. The results are similar to those obtained for the same number of pulses but with fluences varying from 300 mJ·cm^{-2} to 500 mJ·cm^{-2}. Fluence was found to be a very important parameter as it was observed that using very low fluence (200 mJ·cm^{-2}) and one laser pulse only, no NCs could be created. For a certain number of LA pulses, higher fluences were creating a wider spread in NC sizes (from 1nm to 70nm), thus leading to a bimodal distribution. On the other hand, by increasing the number of LA pulses, for a given laser beam fluence, a higher number of small NCs were created without complete elimination of the bigger ones. Therefore, a small (1-2) number of pulses was found to be more effective in avoiding the coexistence of very small and large NCs.

A statistical analysis of the dimensions of the NCs is presented in **Table 1** while a graphical representation is shown in **Figures 4(a,b,c)**. The results for the devices that were laser annealed with 1 pulse (Figure 4a) show a mean NC diameter of 22.3 nm, while larger sized NCs are very rarely observed. However, the use of 5 and 10 laser pulses (Figures 4 b,c) produces simultaneously large (diameters up to 70nm) and small (diameters 1-5nm) Au NCs.

The devices annealed with fluences between 300 mJ·cm^{-2}and 600 mJ·cm^{-2} and 1-5 pulses,

showed the best electrical characteristics hence, these results are discussed hereafter. High frequency Capacitance-Voltage (C_{hf}-V) measurements were used to examine the memory properties through the study of P/E loops at different ranges of applied gate voltages. Control devices with the same thickness of the oxides but without NCs were also measured in order to distinguish the unique properties of the NCs.

Typical results are shown in **Figures 5(a,b)** for MOS devices with or without Au NCs respectively. Regarding the samples containing NCs, the C-V characteristics show a hysteresis window in a clockwise direction that broadens at higher voltage ranges. The hysteresis effect declares that charges are trapped in metal NCs and higher applied gate voltages will result on more charging of the NCs, which leads to wider hysteresis loops. In particular, an increase of the negative applied gate voltage shifts the C-V curves towards more negative V (x-axis) values, indicating that holes tunnel from the Si substrate to the Au NCs, where they are captured. On the other hand, an initial positive applied gate voltage, shifts the C-V curves towards more positive values indicating that electrons tunneling from the n-Si substrate are stored in the Au NCs. On the contrary, the control devices shown in Figure 5(b) did not show a hysteresis loop at all**,** which is a clear indication that the oxide layers are free of any process-induced bulk or interface charges. Therefore the memory window observed in the Au NC containing devices can only be associated to the presence of these NCs.

From Figure 5(b) the dielectric constant (K) of Y_2O_3 was calculated to be around 15, which is close to values reported in the literature [17,18] for sputtered films. Another interesting issue regarding the quality of the deposited layers and the effect of LA on the trapped bulk or interface charge was obtained from a careful measurement of the control and NC containing devices. As can be seen in figure 5b (which was chosen as a typical device) the flat band voltage ($V_{fb)}$ of the control devices was ranging from +0.5V to +1V which is in perfect agreement with the Au/n-Si metal-semiconductor work function difference [19]. For the Au NCs containing devices the C-V at a frequency of f=100 kHz was always recorded as a “fresh” curve, that is the C-V of the unstressed device. The applied gate voltage range during this measurement was always from -1.5V to +1.5V and the V_{fb} was recorded.

The insulating properties of the oxides and the current conduction mechanisms of the corresponding MOS devices were investigated by means of current-voltage (I-V) measurements. Typical I-V characteristics are shown in **Figure 6,** for the same devices used in the C-V measurements. The current conduction mechanism of the NC containing devices was a

space charge limited one and was attributed to the polycrystalline nature of the Y_2O_3 films [16]. It should be emphasized here that Y_2O_3 was not post deposition annealed as the main aim of this work was to study the Au NCs produced after LA prior to any additional annealing step. Moreover, it was found that the conduction mechanisms were changing with the average size, the uniformity and the mean distance between the NCs. The LA processed devices present a clear negative Vg shift (compared to the control devices) which is due to the positively charged NCs as the devices are initially biased at inversion.

In order to test the charge retention performance of the Au-NCs, the MOS devices were first biased at +4 V for 30 s and then at flat band voltage (V_{fb}) to measure an increasing C–t curve. In this case, electrons that tunnel from the Si substrate through the SiO_2 barrier are trapped in the potential well of the Au NCs. When the device was biased at -4 V (inversion) for 30 s, the decrease in capacitance with time was monitored at flatband. Alternatively, a periodic application of a narrow range of gate voltages (always at depletion and close to the expected V_{fb}) was used in order to monitor the V_{fb} change with time. Both measurements gave almost identical results in terms of the measured time constants and in **Figure 7** the retention time of an MOS capacitor structure embedded with Au NCs is given where both Program/Erase (P/E) characteristics are depicted. As shown, after a period of time for negative bias stress, the V_{fb} of the MOS capacitor is reduced by some degree, which suggests that the electrical state of the MOS capacitor is altered. Since the higher voltage corresponds to the electron charged state of the Au NCs and the lower voltage corresponds to the electron discharged state, the diminishing trend of the V_{fb}–t curve can be translated into the charge loss behavior of Au NCs.

The retention characteristics for both electrons (programming) and holes (erasing) can be explained with a two stage behavior: an initial fast decaying stage and a subsequent slow decaying one. These two stages can be attributed to two different mechanisms acting simultaneously: the slow charge relaxation occurs due to electrons trapped deep inside the Au NCs while the fast charge relaxation is due to carriers moving in or out of other traps present in the gate stack. These are either due to oxygen vacancies present in the Y_2O_3 layer or surface states at the NCs or states at the interface between the two oxides. All these traps act as leakage paths for charges to escape easily [8,12,16,17]. Similar results have been reported for MOS capacitors containing either metal [20,21,22,23] or semiconductor NCs [24,25,26,27,28]. To investigate and differentiate the effects of the low emission-excimer laser annealing (LEM-ELA) process on Au NCs and oxide traps, a charge-relaxation–based analysis was adopted

according to a similar analysis explained in refs [8,12]. The various charge relaxation mechanisms were obtained by fitting the V_{fb} retained versus time curves to the double charge relaxation equation:

$$V_{fb}retained = V_1 \cdot \exp\left(\frac{-t}{\tau_{NC}}\right) + V_2 \cdot \exp\left(\frac{-t}{\tau_{traps}}\right) \quad \text{Eq. 1}$$

where, τ_{NC} is the charge relaxation time constant of charges trapped in the Au NCs and τ_{traps} the corresponding time constant of all other bulk, surface or interface traps. It should be mentioned here that the change of V_{fb} with time is directly related to the charge trapped through the well-known equation [19]

$$Q_{tr} = C_{ox} \cdot \Delta V_{fb} \quad \text{Eq. 2}$$

Therefore the time constants calculated from the plots in Figure 7 characterize the charge retention characteristics of the devices. The retention time graph is characterized by two decay regimes: an initial fast and a subsequent slow decay. The fast time constants vary from 10 to 80 s for different fluences and number of pulses. On the contrary, the slow processes have time constants in the range 200 – 1000 s. For the case shown in Figure 7 the fast stage has a time constant of 24 s for Programming and 9 s for the Erase state. The corresponding slow parts have time constants of 700 s or 324 s respectively. This slow part, which is related to charge trapped in the NCs, is rather good while the fast part needs curing or post deposition annealing of the oxides to remove/repair most of the damage due to LA [8].

With increasing fluence of the laser beam at constant number of pulses, the charge relaxation slowed, and the retention performance is improved. However, at a constant fluence experiment, the device performance deteriorates by increasing the number of pulses. This could be attributed to the large number of small NCs surrounding the larger ones, which creates leakage paths for the charge to escape. It is therefore very important to combine the LA process with a post LA curing step in order to enhance the dielectric properties of the oxides and remove any unwanted traps, which decrease the retention times of the devices.

Decay of the initial memory window from 2.984 V to 0.393 V was observed as time elapses. Extrapolation of the data up to 10 years shows that the initial memory window drops to 0.279 V at room temperature. We suggest that the poor retention properties in comparison with state of the art values reported elsewhere [29,30] result from the relative large size of NCs and the polycrystallinity of Y_2O_3 cap layer, which was not annealed. Considering these results, further

study is required in order to create more smaller NC (without the co-existence of larger ones) and improve the retention properties for NVM applications.

Finally, the hole injection (electron detrapping) efficiency under high Program (Erase) conditions of +4.0 V (-4.0 V) is depicted in Figure 8 for the devices with the retention characteristics that were discussed above (LA with fluence of 500 $mJ \cdot cm^{-2}$ and 3 pulses). The speed characteristics are poor and need pulses longer than 10 s in order for the devices to reach the maximum memory window. These results are in agreement with the findings of a very fast discharging mechanism due to bulk or interface defects in the oxides.

Conclusions

The important result of this work was the demonstration of an effective and well performed use of Laser Annealing in producing Au nanocrystals to be used as trapping centers in Si/SiO_2/Au NCs/Y_2O_3/Au MOS structures. The laser fabrication technique showed that using higher fluence (400 mJ/cm^2 - 600 mJ/cm^2) and less than 5 pulses of the KrF laser give the optimum results in terms of NC uniformity and low leakage currents. The electrical characterization showed that Au NCs fabricated via Laser Annealing can be used in flash memory devices providing good electrical characteristics due to the creation of high quality and high homogeneity metal NCs. Measuring the read/write/erase capabilities of the device, memory windows of approximately 2.9 V were demonstrated. Future work involves further understanding of the role that the laser annealing in creating better refined metal NC sizes and subsequently improved retention time device performance. Optimization of the technique is the aim of such a task, and current experiments are performed in standardizing such a procedure.

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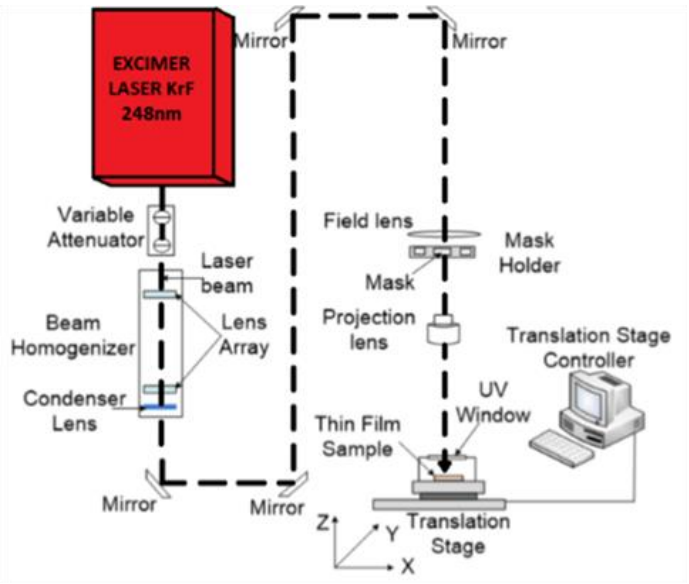


Figure 1: *Schematic configuration of the KrF excimer laser annealing system used.*

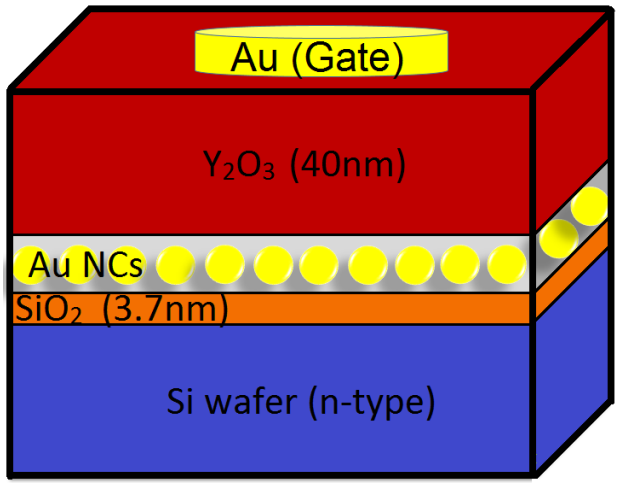


Figure 2: *Memory device structure.*

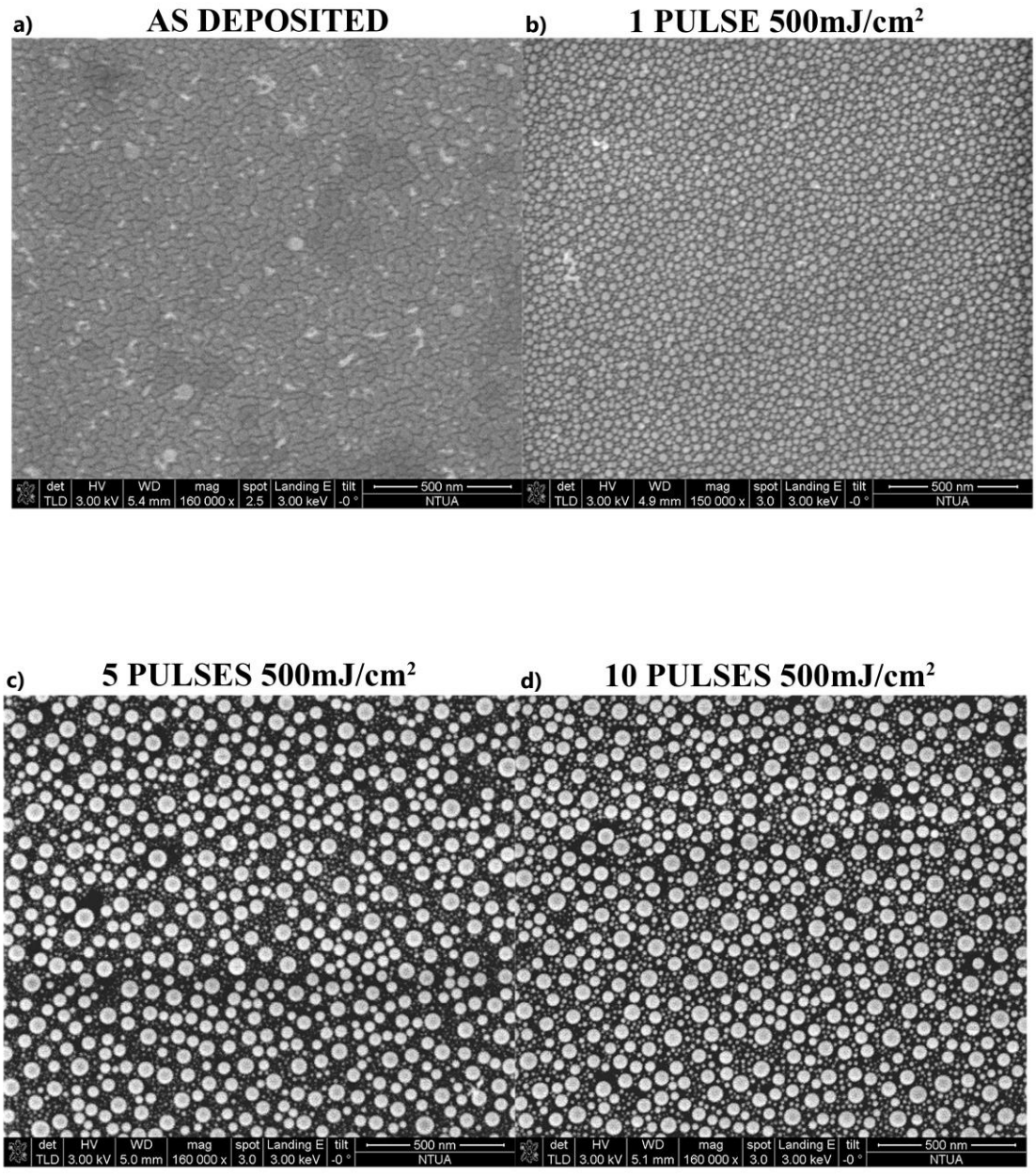
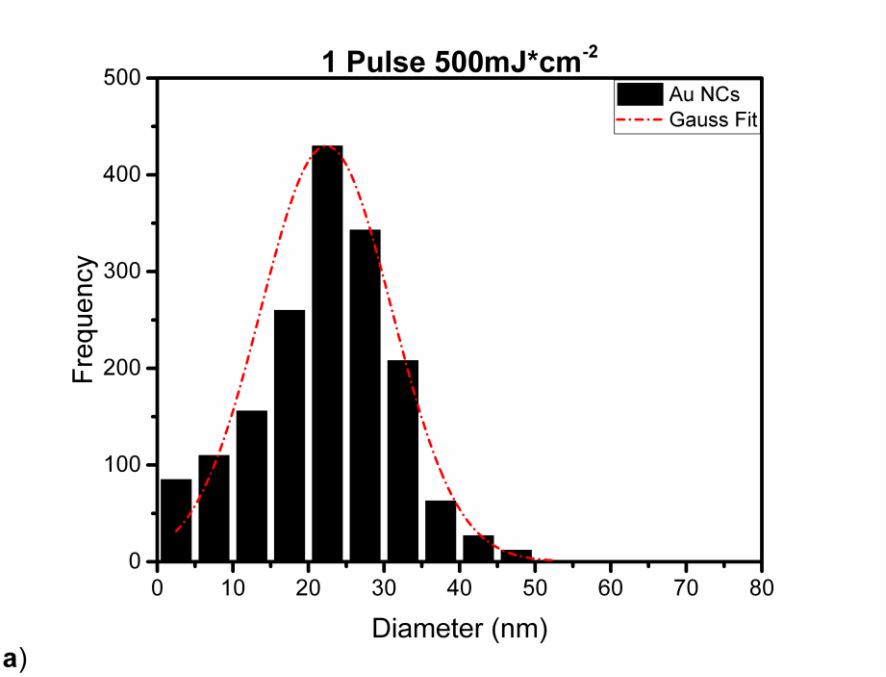


Figure 3: *SEM picture of the (a) as deposited Au film and NCs created after laser annealing at 500mJ/cm2 with (b) one pulse, (c) five pulses and (d) ten pulses.*


1 Pulse 500mJ*cm-2
Au NCs
Gauss Fit
Frequency
Diameter (nm)
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100
200
300
400
500
0
10
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50
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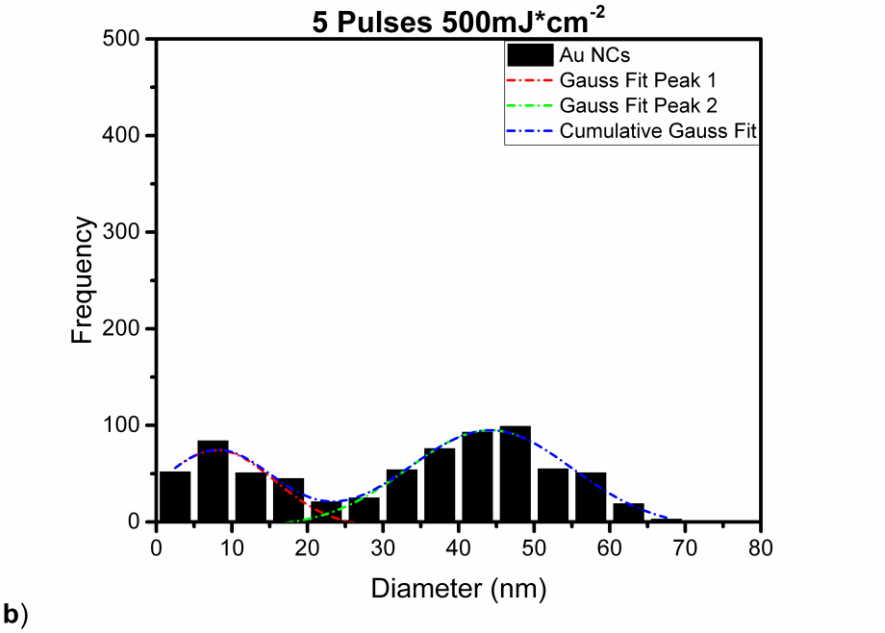
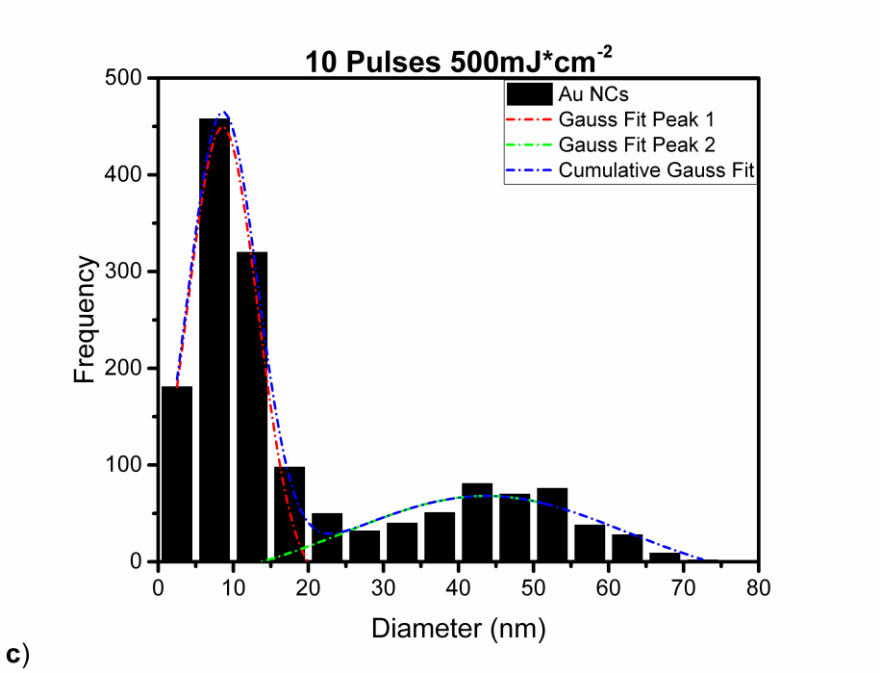
80

a)


5 Pulses 500mJ*cm-2
Au NCs
Gauss Fit Peak 1
Gauss Fit Peak 2
Cumulative Gauss Fit
Frequency
Diameter (nm)
0
100
200
300
400
500
0
10
20
30
40
50
60
70
80

b)

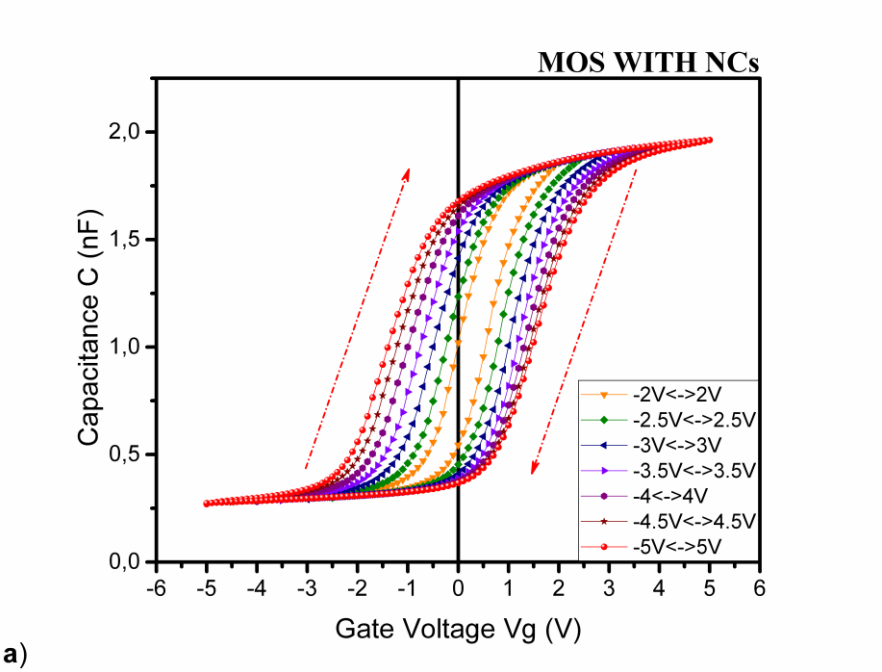


c)

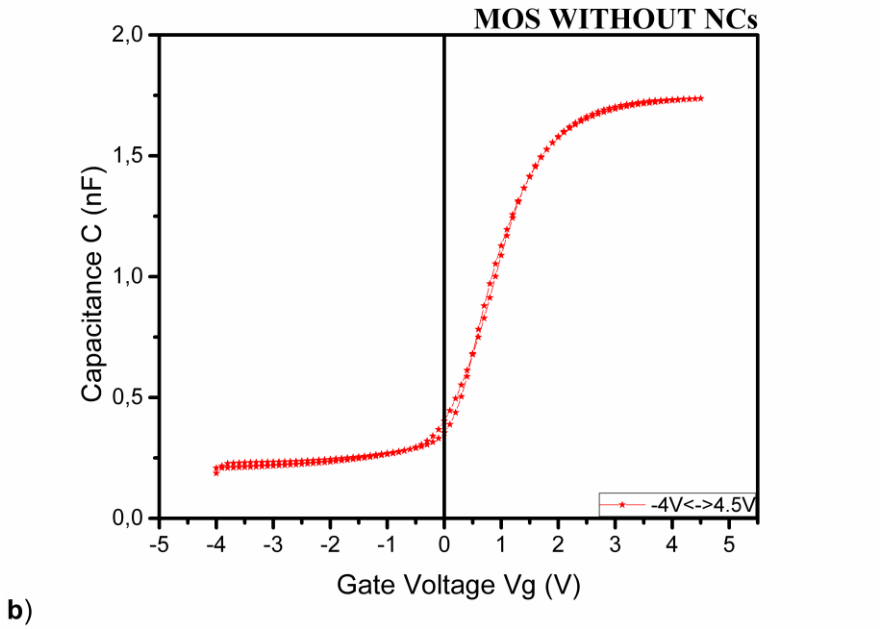
Figure 4: *Column chart of formed Au NCs fabricated using a KrF laser at a fluence of 500mJ/cm2 with (a) 1 pulse, b) 5 pulses and c) 10 pulses. Fitted lines are guides to the eye only.*

Samples LA with fluence 500 [mJ/cm2]	**1 pulse**	**5 pulses**		**10 pulses**	
		First Peak	**Second Peak**	**First Peak**	**Second Peak**
Average diameter [nm]	22.3	8	44.2	8.6	43.7
Standard deviation [nm]	8.7	7.6	10.9	4.7	18.6
Surface density [# NCs/cm^2]	$7.98 \cdot 10^{10}$	$3.10 \cdot 10^{10}$		$6.50 \cdot 10^{10}$	

Table 1: *Statistical analysis of Au NCs fabricated via LA with fluence 500 mJ·cm-2 with different number of laser pulses.*



a)



b)

Figure 5: *C-V measurements of MOS devices (a) with Au NCs, fabricated using a KrF laser with a fluence of 500 mJ/cm^2 and 3 pulses and (b) without NCs.*

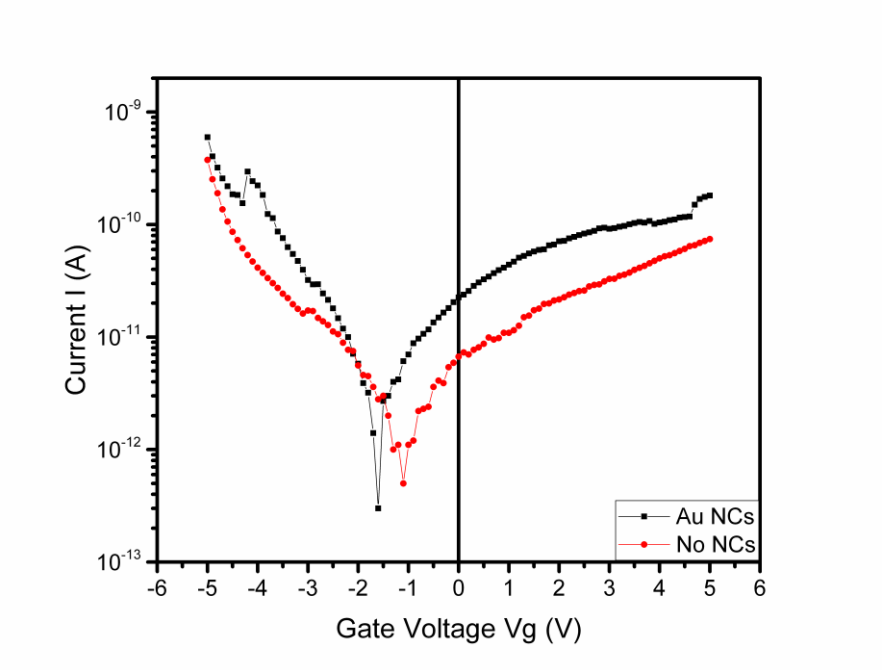


Figure 6: *I-V characteristics of MOS device with and without Au NCs.*

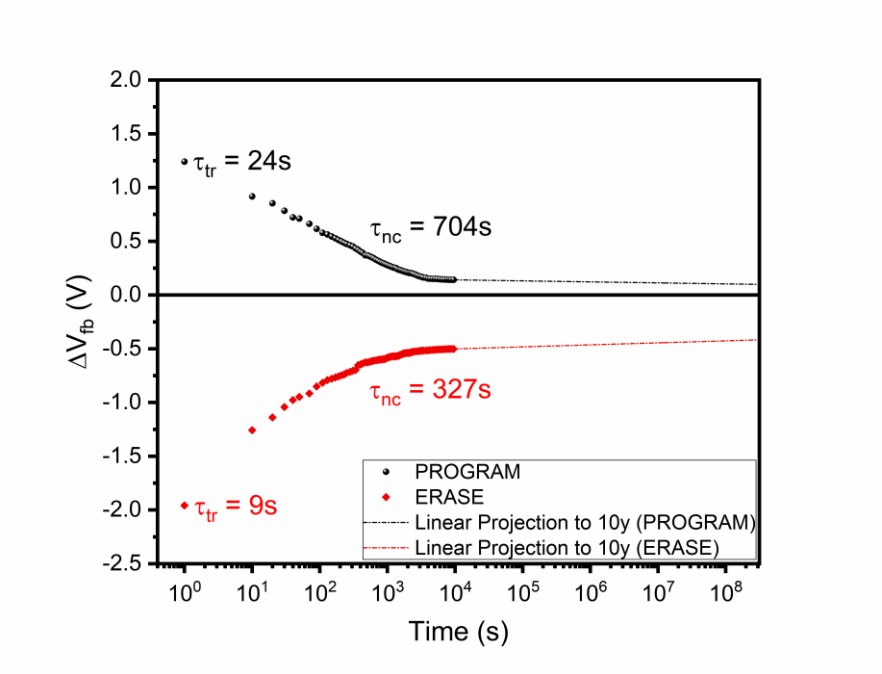


Figure 7: *Retention time characteristics for MOS device containing Au NCs after LA with a fluence of 500 mJ/cm^2 and 3 pulses.*

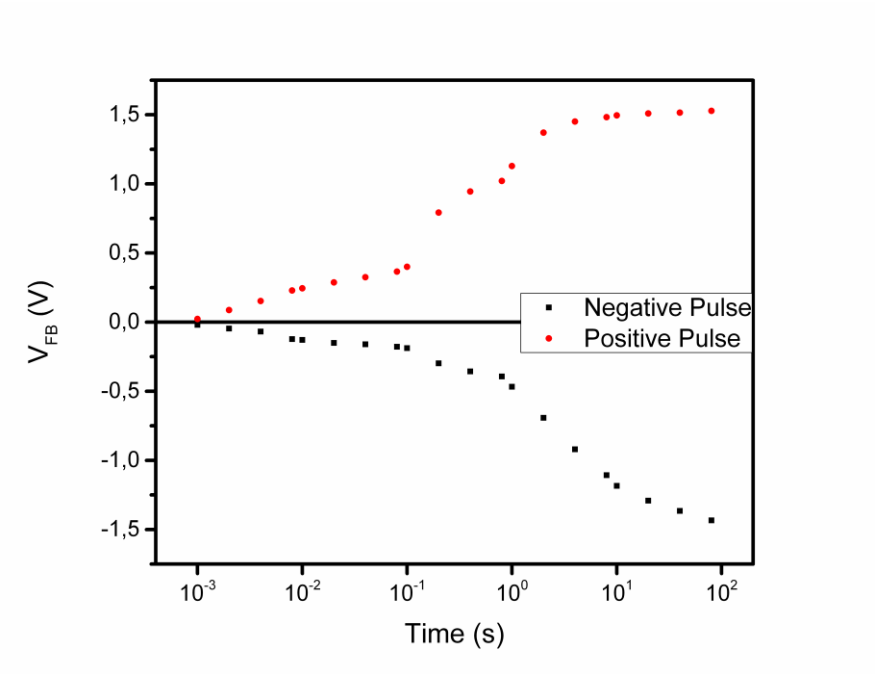


Figure 8: *Hole injection efficiency under high Program (Erase) conditions of +4.0V (-4.0V).*