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Flexible FETs using ultrathin Si microwires embedded in solution processed dielectric and metal layers

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Abstract

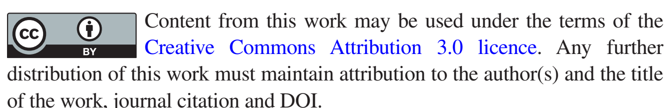
This work presents a novel manufacturing route for obtaining high performance bendable field effect transistors (FET) by embedding silicon (Si) microwires (2.5 μm thick) in layers of solution-processed dielectric and metallic layers. The objective of this study is to explore heterogeneous integration of Si with polymers and to exploit the benefits of both microelectronics and printing technologies. Arrays of Si microwires are developed on silicon on insulator (SOI) wafers and transfer printed to polyimide (PI) substrate through a polydimethylsiloxane (PDMS) carrier stamp. Following the transfer printing of Si microwires, two different processing steps were developed to obtain top gate top contact and back gate top contact FETs. Electrical characterizations indicate devices having mobility as high as 117.5 $cm^2 V^{-1} s^{-1}$. The fabricated devices were also modeled using SILVACO Atlas. Simulation results show a trend in the electrical response similar to that of experimental results. In addition, a cyclic test was performed to demonstrate the reliability and mechanical robustness of the Si μ-wires on flexible substrates.

Keywords: transfer printing, Si microwires (μ-wires), flexible electronics, field effect transistors, PDMS

(Some figures may appear in colour only in the online journal)

1. Introduction

Flexible electronics have attracted significant interest in recent years due to increasing demand in a range of applications such as robotics, prosthetics, health monitoring, etc., which require conformability of electronic systems to 3D curved surfaces [1]. Some of the driving features for flexible electronics are the requirements such as conformable integration to nonplanar surfaces, portability, foldability and large area coverage [2–4]. A cost-effective and reproducible method for constructing such electronic systems is much needed and therefore the research in this area is heading towards merging of the well-established microelectronics technology and conventional coating and printing techniques [2, 5–7]. A remarkable interest has been shown towards printing of organic materials due to their solution processability in ambient environment. Organic materials have the advantages of mechanical flexibility, low material and fabrication cost. Further, they are often compatible with roll-to-roll processing and the thermal budget of polymeric substrates. Despite these attractive features, obtaining high-performance devices from organic semiconductor remains a major challenge [8–10]. Devices made of organic materials typically have low charge carrier mobility (~1 with respect to ~1000 $cm^2 V^{-1} s^{-1}$ of single crystal Si) [10–12], which makes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them much slower to respond than crystalline Si built devices. Furthermore, poor stability and short life of the organic materials make them a poor choice for electronic systems requiring better performance and high durability. A large number of applications, especially where faster communication and computation is needed, require high-performance flexible electronics [9, 12].

In this regard, the electronics based on a mix of both organic and inorganic materials could be an attractive option as high-mobility inorganic semiconductors would enable devices with faster speed and stable performances. In past, using polycrystalline Si in place of organic materials helped in overcoming some of the performance related challenges, but this came at the cost of complex procedures and sophisticated setups for achieving suitable uniformity [13–15]. Thinning down the standard Si wafers by mechanical or chemical-mechanical polishing is another approach, which has been explored to realize high-performance flexible electronic circuits [16, 17]. However, flexible chips are more prone to damage either during the thinning process because of the brittle nature of Si wafer or caused by small dislocations within the crystal. Overcoming issues related to small mismatches and cavities in the material crystal pose further challenges for wafer thinning route as these might rapidly propagate in the form of cracks during or after the thinning process. In this regard, the miniaturized structures such as Si nano/microwires could offer better solutions [18, 19]. The viability of Si nano/microwires for high-performance flexible electronics has been demonstrated recently with high temperature processing steps performed on the donor wafer and relocating or transferring the wires to flexible substrates [9, 10, 17, 20–23]. The transfer of wires to secondary flexible substrates can be carried out either by dispersing them in a solution or through a stamp-assisted dry transfer printing technique [5, 8, 18, 21, 23, 24]. However stamp assisted transfer printing is preferred as it guarantees the orientation of finished or polished surfaces for post-processing of transfer printing for devices' fabrication.

The frequently reported devices with dry transfer printing of Si are back-gated FETs, where the dielectric layer is restricted to a single type of material, which is also used as the adhesive layer [10, 24, 25]. Devices developed with such configuration have potential applications in microfluidics and biological sensors where the semiconductors wires are left exposed for direct interaction with the external stimuli [18]. On the other hand, a number of physical sensors such as pressure, temperature, proximity, humidity and many other electronic devices can be developed in structures that have a direct interface of Si microwires with transducer materials. In this study, a new manufacturing technique is proposed and optimized for the development of both top and back-gated FETs on PI substrate by embedding Si microwires in solution-processed materials. A reliable and cost-effective manufacturing route is the focus of this research. The processing steps for deposition of diverse gate dielectrics and screen-printed metallic contacts within the thermal budget of PI substrate are presented along with proof of concept devices. A single Si microwire (50 μm wide) is selected for the fabrication of a typical FET in the shape of back and top gated structures. The detailed description of technology, device designs and simulation results are presented in the following sections.

2. Microwire designs and fabrication

The manufacturing process begins with the definition of Si-microwires on SOI wafers through a top-down method, which involves standard photolithography and etching steps. The SOI wafer (Soitec, *p*-type Boron (B) doped with resistivity of 15–20 Ω cm and a device layer with thickness of 2.5 μm) is selected as the donor or mother wafer to obtain microwires with similar dimensions such as thickness, width and length. The thickness of microwires is alike due to the well-controlled thickness of top Si layer i.e. above the buried oxide layer in SOI wafer. Using deep reactive ion etching (DRIE) the vertical trenches (with depths up to the buried oxide) are realized between the microwires. The modules with different lengths and widths of microwires were fabricated in parallel arrays of 20 wires, as shown in figure 1. Different dimensions of the microwires were investigated to understand and evaluate the influence of interface between carrier stamp and Si microwires and hence optimize the transfer yield. The widths of microwires investigated in this study were 10, 20, 30, 40 and 50 μm. Similarly, the lengths of the wires were 200, 500, 1000, 20 000, and 50 000 μm. The width of the trenches also plays an important role during etching of the buried oxide layer as well in the first transfer-printing step. For this purpose, the trenches with varying widths i.e. 10, 20, 30, 40 and 50 μm were realized. Anisotropic etching is desired to develop high aspect trenches with vertical cut at 90° and uniform edges, which was achieved with DRIE. Before initiating the under-etching of buried oxide from microwires, the trench edges were completely cleaned of all the passivation and organic residues. To do this, the microwires were bathed in piranha solution prepared by H_2SO_4 and H_2O_2 in 3:1 respectively, followed by rinsing in deionized water. The standard etchant for SiO_2 i.e. 40% buffered hydrofluoric (BHF) is used to etch away the buried oxide and release the microwires completely until the anchored points at the ends. To ensure the complete release of the wires, samples were retained in the etchant solution for 10 extra minutes from the time required for complete under-etching of the oxide layer. After completing the etching step, the microwires are gently cleaned with deionized water and dried in furnace at 100 °C. The post-processing steps after under-etching the oxide layer were performed with great care to ensure that the microwires remain tethered to the donor wafer. In current study, transfer printing of 50 μm wide wires are explored and the same were ultimately used for field effect transistors.

3. Experiments and characterization

The PI substrate (25 μm thick) is selected for the development of FETs, owing to their good stability and high thermal budget ~ 300 °C. PI substrate was cleaned with isopropanol, deionized water and attached to a glass slide, which is used as a temporary carrier and removed after the process is complete.

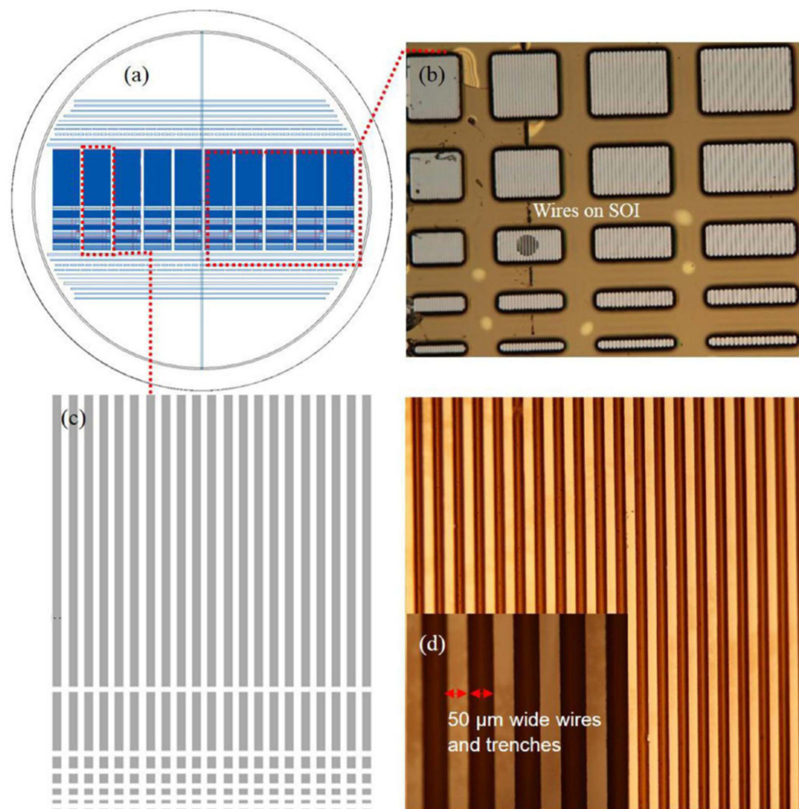

Figure 1. Microwires design, with corresponding lengths and modules, (a) wafer-scale design of microwires, (b) microscopic image of individual block of Si microwires, (c) array of 200, 500, 1000, 2000 and 5000 μm long wires, and (d) microscopic image of etched wires.

For better hydrophilic property and enhancing the adhesion of subsequent layers, the substrates were treated by plasma oxidation and subsequent layers were printed immediately. This step is essential for the back-gated FET structure, as the silver gate electrode was to be patterned with screen-printing technique. As screen-printing is nearer to manufacturing, the patterning of back-gate electrode using screen-printer is a step towards low-cost manufacturing of the flexible FETs. The physical and electrical properties of metal patterning through screen printing is described in detail elsewhere [26]. Converse to the back-gated FETs, the SU-8 which acts as the primary adhesive layer for receiving Si microwires was directly spin coated on PI substrate after treatment with oxygen plasma for the development of top-gated FETs. Following sections describe the fabrication of flexible FETs from arrays of Si microwires.

3.1. Transfer printing of Si microwires

The transfer of Si microwires can take the route of either wet assembly or a stamp assisted dry transfer technique. Dry transfer of Si microwires through a carrier stamp is the preferred approach for deterministic placement of microwires and to guarantee the same orientation of top surface of microwires for subsequent processing layers of devices. Further, the crystallinity and doping profile are assured to remain on the top of microwires as developed initially on the SOI wafer. The materials that could be easily molded in different structures with the clear and uniform surfaces are desired for transfer stamps. In this regard, PDMS (poly (dimthylsiloxane)) is a natural choice as in addition to the easy molding in different shapes, its viscoelasticity also enhances the transfer printing with possibility of tuning the peel off rate of the stamp. To increase the transfer yield in the first transfer step, a planar surface of the stamp is desired for a conformal contact with the microwires and to maximize their interface area with the microwires. A slight misalignment or gap between the two surfaces can result in a weaker bond, which may not be sufficient enough to detach the microwires from the donor wafer, especially at their tethered positions. For this purpose, a dedicated mold was designed to hold two polished Si wafers at a defined distance and the PDMS (base: curing agent, 10:1) was poured between them to be molded. Prior to dispensing PDMS within the mold, the wafers were silanized to obviate the development of stronger bonds between molding wafers and PDMS, which ultimately helps in removal of PDMS stamp from the wafers. After filling the mold the PDMS is kept for polymerization in a furnace at 60 °C for 3 h.

Transfer printing of Si microwires to PI is accomplished in two steps through the PDMS stamp as shown in figure 2. A thicker stamp is used for easy handling and also to avoid breaking of the wires during the transfer process. Thicker stamp also aids in keeping a large peel-off angle, which is an essential requirement in the first transfer step to avoid cracking of the Si microwires during the course of detachment. PDMS stamp was treated with oxygen plasma to tune its surface properties for better pick-up of microwires from the donor wafer. Other parameters enhancing the detachment

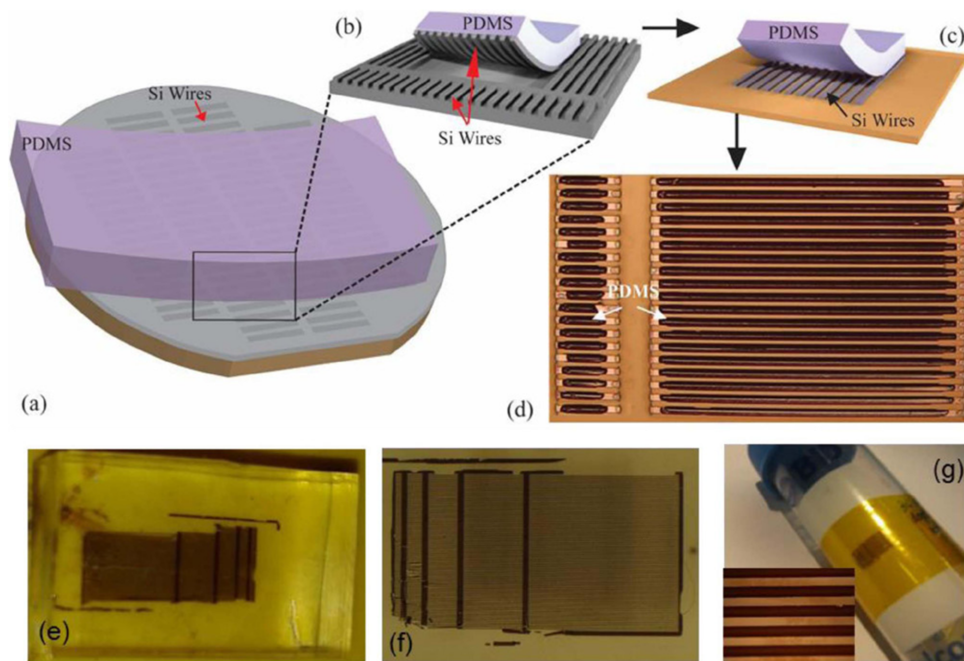

Figure 2. Fabrication of Si microwires and transfer printing to temporary transfer substrate. (a) Patterning of wires and under-etching of buried oxide, (b) transferring Si wires from wafer to PDMS stamp, (c) stamping PDMS with microwires on final receiver substrate, (d) peeling off PDMS, leaving behind microstructures on PI. (e) Corresponding experimental step for transfer of Si to PDMS from mother wafer, (f) experimental results of transferring Si wires to PI substrate after removing PDMS stamp, (g) PI substrate with transferred Si microwires wrapped around circular shaped object [1, 17].

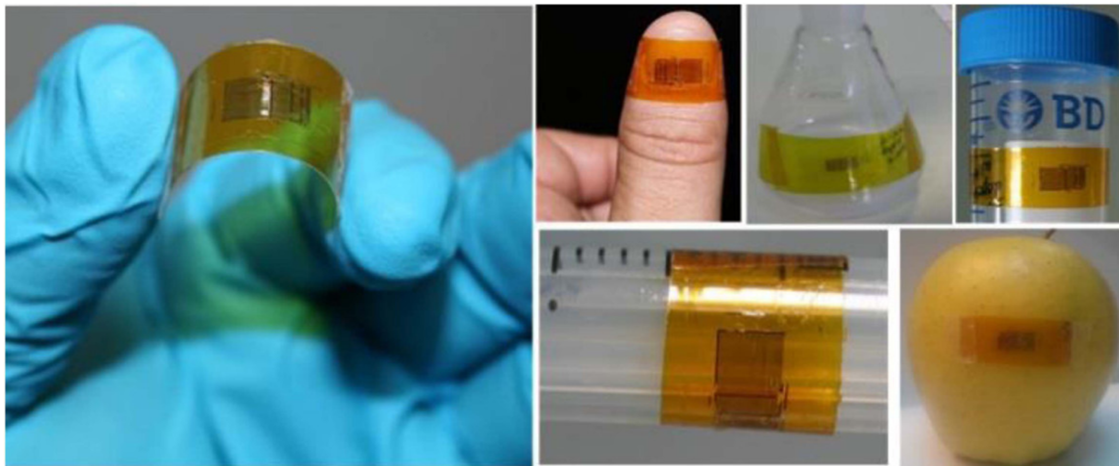

Figure 3. Transferred Si microwires on PI substrate and attached to various objects with different orientations and radius of curvatures.

of tethered wires from the donor wafer include over-etching of oxide under the wires and the peel-off rate. More than 95% yield of microwires transfer was achieved in the first transfer step as shown in figure 2(f), which is a significant improvement over our previous results [20]. In the second transfer step, a stronger adhesive is needed on receiver substrate so as to detach the microwires from PDMS stamp. Therefore, SU-8 (a high contrast photoresist and sensitive to ultra violet (UV) light) is used as the adhesive layer. SU-8 has the desired level of stickiness when partially sintered, and hardens after complete sintering. A thin layer of SU-8 is spin coated at 5000 rpm to achieve thickness of about ~800 nm. This layer is partially sintered by putting it on a hotplate at 90 °C for 80 s. PDMS stamp with Si microwires is then brought in conformal contact with SU-8 layer and passed through UV light for complete sintering. The transparent PDMS allows UV light to pass through the spaces between the microwires, which results in the hardening of SU-8. The UV light is also used on the sideways and backside of the substrate to complete the sintering process. As a result, 100% transfer yield is achieved after removing back the PDMS stamp as shown in figures 2(e) and (f). Finally, the SU-8 layer is hard baked at 130 °C for 30 min in a furnace and subsequent layers are deposited for development of FETs. Figure 3 shows microwires on PI substrates placed on objects with different curvatures. The SU-8 layer is also used as the gate dielectric for back-gated FETs. The thickness of SU-8 layer was optimized to suit its use both as the adhesive and the dielectric layer.

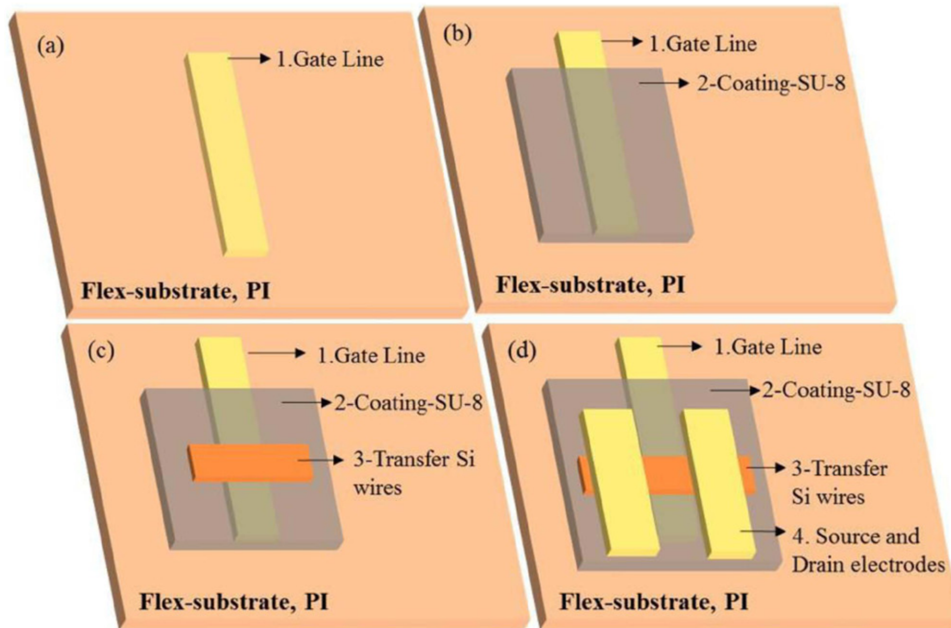

Figure 4. The process flow showing the step by step material layers deposited for a back-gated FET. The numbering shows the sequence of steps performed for developing each layer for the development of the field effect transistor from a single Si microwire. (a) Screen printed back-gate lines on PI substrate. (b) Spin coating of dielectric adhesive layer. (c) Transferring Si microwires on adhesive layer. (d) Patterinig source and drain on top of Si microwire.

3.2. Fabrication of FETs structures

The efficacy of transferred miniaturized Si microwires can be authenticated by their potential use in an active device. For this purpose the transferred Si microwires are incorporated within layers of dielectric and metallic materials to complete the manufacturing steps for a typical FET structure. Two types of structures are investigated in this work. These are: (a) back-gate top contact, and (b) top-gate top contact FETs. For the back-gated FETs shown in figure 4, the silver (Ag) gate electrodes are screen-printed on PI substrate. The adhesive layer is then spin coated, which is followed by transfer of Si microwires. This is followed by micro spotting of Ag paste for source and drain contacts. The processing steps for the back-gated FETs are shown in figure 4. The back-gated FET structure has single dielectric material (in this case, SU-8), which is also the essential adhesive layer needed for transferring of Si microwires. SU-8 is the most suitable material in the proposed fabrication process, as it also possesses suitable optical properties such as high contrast and sensitivity to UV light. The optical transparency is required for the overlay registration accuracy of the Si microwires with the underlying patterns of back-gate electrodes. As explained earlier, the sensitivity to the UV light also helps in the hardening of SU-8 before PDMS stamp is removed in the transfer print process. The UV curability makes the transfer printing process robust and helps us achieve 100% microwires transfer yield in the second transfer step. In this regard, the SU-8 layer in back-gate FETs has to meet the trade-off between thicknesses needed for better performance of the transistor (when its use as dielectric is considered) and for its use as adhesive to detach Si microwires from PDMS stamp. To meet both the requirements, the recipe for spin coating was optimized and SU-8 was coated at 5000 rpm to achieve a thin layer of ~800 nm.

To expand the field of applications of Si microwires and make process compatible with a wide range of dielectrics or transducer materials, top-gated FET structure is desired. This approach can also lead to processes, whereby organic materials could be integrated with the inorganic semiconductors. This will ultimately result in low-cost fabrication as a result of the lower cost of organic materials and their solution processability. In this case the top dielectric and metal layers also serve as the encapsulation layer for the Si microwires and protect them from harsh environment. Embedding the brittle Si microwires in suitable solution-processed materials could also improve overall bendability and prevent breaking of wires during bending [16]. The construction of top-gated FETs starts with the spin coating of SU-8 layer on top of cleaned PI substrate, with the same spinning recipe as described above for the back-gated FETs. The design and process steps for the top-gated FET utilizing a single Si microwire, are shown in figure 5. After transfer printing of Si microwire and hard baking of the SU-8 layer, silver (Ag) paste is patterned on top of Si microwire using micro-spotting technique. After thermal treatment of the Ag paste, the dielectric material was spin coated on top of these patterns and Si microwire. To make the process robust, a UV-curable dielectric material was selected. The spin speed was kept at around 5000 rpm where thickness achieved was in the range of 300–400 nm. The variation in the thickness is due to the non-planar surface as a result of Si microwire on the PI substrate, which hinders the uniform spreading of the dielectric material and thus results into non-uniform thickness of the final layer.

The mechanical reliability and adhesion of Si microwires under different bending radii was investigated through

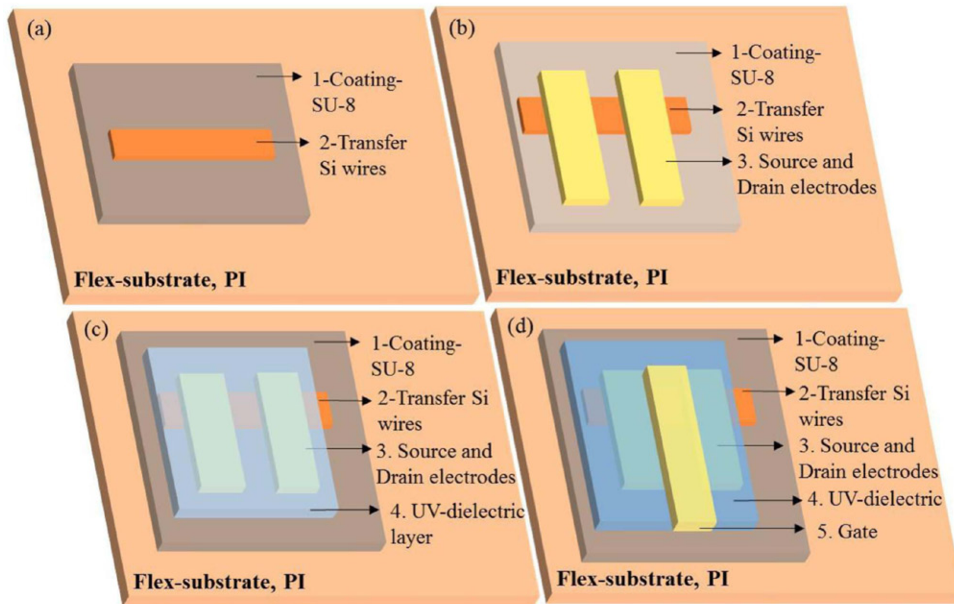

Figure 5. The process flow showing the step-by-step materials layers deposited for top-gate FET. (a) Spin coating adhesive layer on PI substrate. (b) Transferring Si microwires on adhesive layers, followed by patterning source and drain contacts. (c) Spin coating UV-dielectric layer. (d) Patterning top metal layer as a gate electrode.

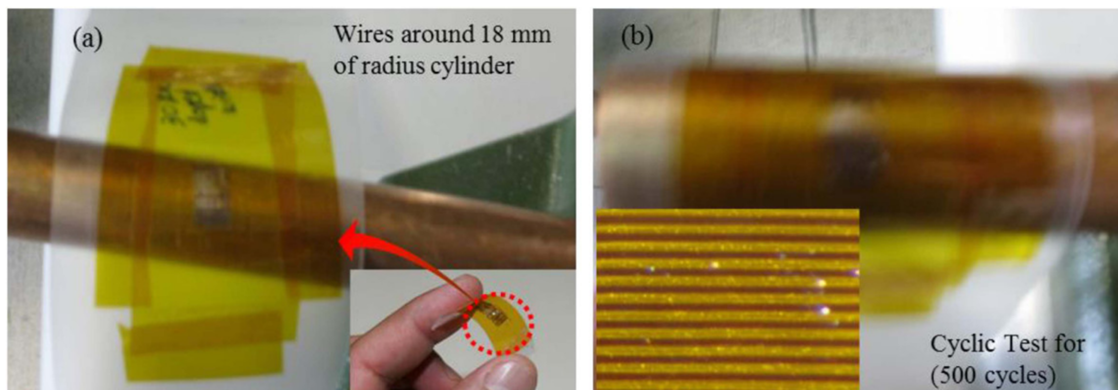

Figure 6. Cyclic test for testing cracks or delamination of Si microwires from the adhesive layer. (a) PI substrate containing Si microwires is fixed to a separate plastic sheet and wrapped around different size nonplanar surfaces. (b) During the cyclic test. The inset image shows wires after the cyclic test.

cyclic tests. The physical robustness of the structures was evaluated by observing crack propagation and delamination of the microwires from the receiver substrate. Substrate was wrapped around different circular and nonplanar shapes for one time bent as shown in figure 3, while cyclic tests were performed for repeated bending of the microwires. During the course of cyclic tests, the secondary PI substrate containing the microwires are attached to a separate plastic sheet as shown in figure 6, where it is revolved around cylinders with outer diameters of 8, 12 and 16 mm. Bending tests are performed through the plastic sheet for about 500 cycles around each cylinder and observed under an optical microscope for cracks or delamination from the substrate. By observing all the microwire arrays under an optical microscope, we observed no cracks or delamination of the wires from the adhesive layer after cyclic tests, which confirm the mechanical robustness of the wires.

3.3. Micro-spotting for metallization

The micro-spotting is performed using a custom-made tool comprising of a precise positioning setup and tungsten needle of micrometer size tip. The needle in the setup is clamped with a steel rod, which is free to move in 3D. The tungsten needle is used to pick up a small droplet of Ag paste from solution and source and drain contacts are realized by micro spotting at the desired areas and simultaneously observing it through a microscope. The spacing between the two electrodes defines the effective channel area of the FETs on the Si microwire. After deposition of the dielectric layer, the gate electrode is designed to align over the effective channel areas, making it possible to realize a field effect transistor at the crossing. Each transferred block contains a parallel array of 20 microwires of 50 μm wide each. Amongst these, a single microwire is selected for the construction of FET devices

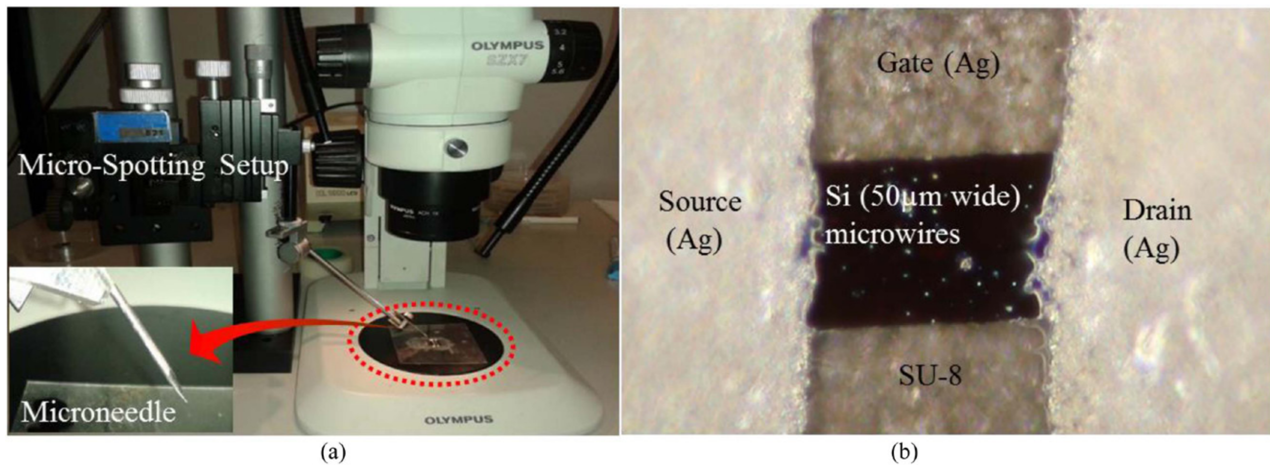

Figure 7. (a) Micro-spotting tool for Ag metallic contacts of FETs, (b) developed FET structure by using a single Si microwires as the semiconductive layer, silver (Ag) for source drain and gate and SU-8 as the adhesive and dielectric layer.

to investigate its physical and electrical characteristics. The proposed approach is unique as the aspect ratio, which is conventionally used to set the current in transistors, can simply be changed with increasing the number of Si microwires in a single block or by increasing the number of electrodes on a single wire, assuming 100% overlay registration accuracy of gate electrodes is possible. Figures 7(a) and (b) show the micro-spotting tool used for patterning of Ag paste for the source and drain contacts and a typical FET structure realized by using this micro-spotting tool. The order of patterning is different for top and back-gated structures. Micro-spotting is applied only for source and drain patterning on top of Si microwire in the back-gate FETs, whereas the source and drain are patterned in the first place in top-gate FETs by micro-spotting followed by spin coating of dielectric layer and again micro-spotting of the top gate. The edges of the source and drain patterns are not uniform, as the low viscosity Ag paste tends to spread irregularly after micro spotting. This non-uniformity could be reduced either by using smaller droplets or by using a more viscous solution, which has a low co-efficient of spreading.

Simulations of the proposed designs were initially performed with SILVACO Atlas by assuming a Si strip. The dielectric materials were defined by using existing models for the standard materials of MOSFET technology. Simulation results by using close matching dielectric properties of the material used in experiments i.e. UV-curable dielectric are shown in figure 8, which presents the output and transfer characteristics of the device. The output characteristics of the simulated devices showed similar behavior as obtained with experiments. The small deviation in the experimental results (in figures 9 and 10) is due to the non-ohmic contacts of the Ag paste with lightly doped Si microwires. The silicide contacts made by using Ag paste on top of Si microwires also contribute to the lower values of output currents in the experimental results. Further, the semiconductor and dielectric interface also affects the performance of the device. On average, the device's response with different dielectric materials simulated with the same model show similar trend of performance to the experimental results.

Electrical characterizations of both devices were performed in ambient environment using semiconductor parameter analyzer (4156C, Agilent). By efficient transferring of 50 μm wide wires onto PI substrate, the FET device fabricated from a single microwire has a channel length and width of ~60 μm and 50 μm respectively. The channel length of the microwire based FET is dependent on the high-resolution patterning of metals for source and drain contacts. Being a manual technique the channel length is controlled in close ranges to ~60 μm. On the other hand the channel width can be well controlled, as the standard lithography tools set the width of Si microwires, which defines the channel-width. In these experiments, the maximum width i.e. 50 μm wires are selected due to the good transfer yield. The Si-microwires FETs on PI substrate were characterized and figures 9(a) and (b) and 10(a) and (b) show the plots for the output and transfer current–voltage (I–V) characteristics of the back-gated and top gated FETs respectively. The field-effect mobility (μ_{FE}) of devices was extracted using $\mu_{FE} = L_G g_m/(W_G\, C_G\, V_D)$, where L_G (~60 μm) and W_G (50 μm) are the physical dimensions of the gate length and width respectively. The highest value of field effect mobility recorded was 117.5 cm^2 V^{-1} s^{-1} and this was achieved with top-gated UV-curable dielectric material. The mobility achieved with the bottom gated SU-8 was 69 cm^2 V^{-1} s^{-1}. The threshold voltage measured through extrapolation in the linear region show 2.75 V and 3.25 V for bottom and top gate FETs respectively. As the Si-microwires are not heavily doped so the linear region indicates the large parasitic resistance associated with the source and drain contacts, the behavior that is similar to a small schottky barrier FET. The small parasitic resistance indicates the need for further doping of the Si-microwires and optimization of the patterning in future to obtain ohmic contacts and lowered barrier for charge carriers. The output and transfer curves in figures 8 and 9 show clear saturation behavior at larger positive biases. Further, the gate dependence of the curves confirms the operation of the device inversion mode of the p-type microwires. All devices were operated in the inversion mode requiring a positive gate voltage to turn on the device. The back-gated FETs showed poor modulation of the channel conductance due to

Figure 8. Simulation performed with similar structures and materials properties as used in this work. (a) Simulated FET model for top gated FET, (b) output response, and (c) transfer curve of the simulated device.

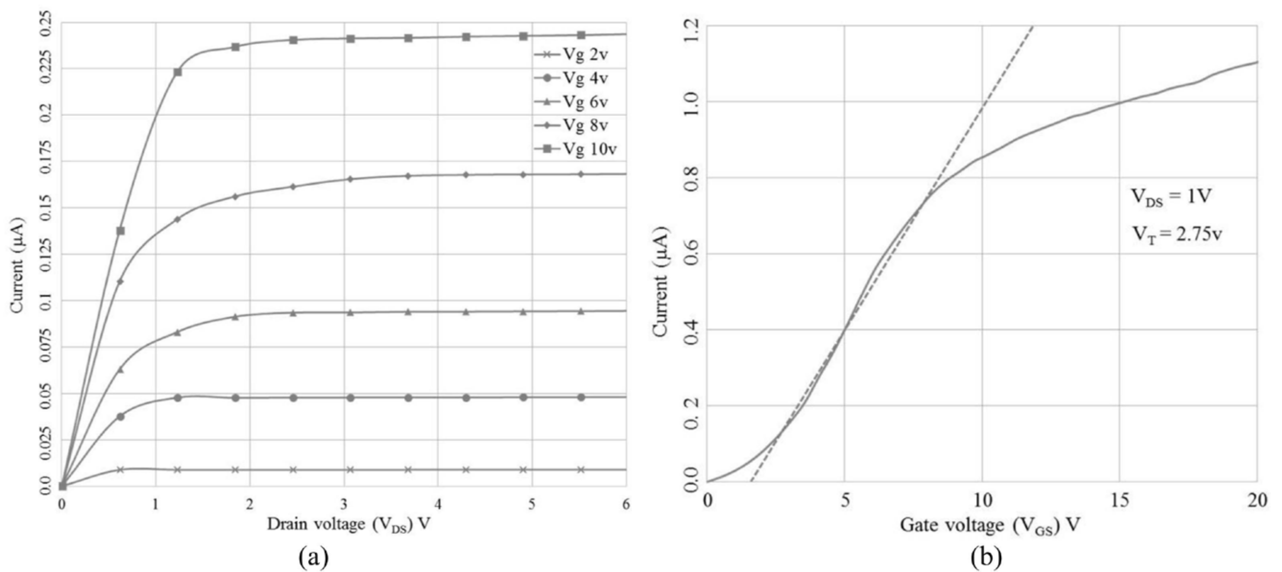

Figure 9. (a) Output response with SU-8 3010 as dielectric material in a back gated FET, and (b) transfer curve with UV-DuPont as dielectric material in back-gated FET.

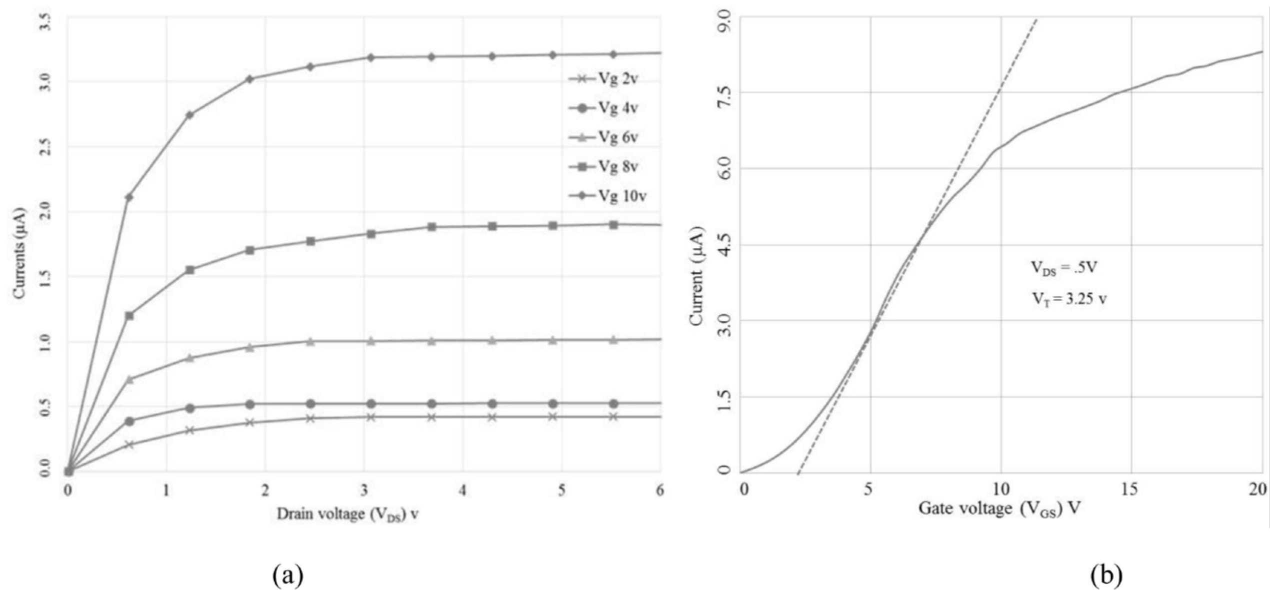

Figure 10. (a) Output curve of UV-DuPont dielectric as dielectric material for top-gated FET. (b) Transfer of UV-DuPont as dielectric material for top-gated FET.

the increased thickness of SU-8 gate dielectric accompanied by the thickness of the Si microwires (2.5 μm). The fabricated FETs were also tested after cyclic tests and the electrical characteristics remained the same as observed in figures 9 and 10 before the cyclic tests. The mobilities achieved with the top-gated FETs are in the ranges needed for applications in flexible electronics circuit such as inverters, ring oscillators and as an active matrix for displays on polymeric substrates [27].

4. Conclusion

In summary, a reliable and cost-effective manufacturing route is presented for top and back-gated FETs on flexible PI substrates by incorporating single crystal Si microwires in diverse solution processed dielectric and adhesive materials. Si microwires are obtained by top-down fabrication approach and transferred to an adhesive layer on PI substrate by using PDMS assisted transfer printing. The back-gate electrode is screen-printed, which is a step towards low cost manufacturing. Results validate the top and back-gated FETs and the use of different dielectric materials in fabrication of these FETs. The feasibility of embedding Si-microwires within layers of solution-processed materials, opens new avenues for fabrication involving both microfabrication and printing tools. The physical and mechanical characterizations of the devices are performed by doing cyclic bending tests by monitoring the cracks or delamination of the microwires from the adhesive layer of flexible substrate. The *I–V* measurements show a better range of performance as compared to the devices developed from organic based materials.

The back-gated FETs have great potential for chemical and gas sensing applications due to the direct interaction of the stimuli with the Si microwires. Similarly, the top gated configurations provide an opportunity to deposit diverse transducers such as piezoelectric, pyroelectric or ferroelectric materials to develop sensors for measuring physical parameters such as tactile, soft touch and temperature. The behavior similar to schottky barrier FET needs further investigation for the devices to offer an alternative for future flexible and large area printed electronics. To enhance the performance of FETs, potentially the metal-semiconductor interfaces could be processed through silicidation instead of using heavily doped semiconductors.

Acknowledgments

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