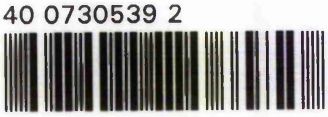


PERFORMANCE STUDIES OF THIN FILM ELECTROLUMINESCENT (TFEL) DEVICES

Murugesan Sethu

A thesis submitted in partial fulfilment of the requirements of
The Nottingham Trent University for the degree of
Doctor of Philosophy

Electrical and Electronic Engineering Division
The Nottingham Trent University
Nottingham, U.K.

September 2002

Abstract

The study of mechanisms that contribute to the characteristics of Alternating Current Thin Film Electroluminescent (ACTFEL) display devices are presented. Primarily the investigation is based on Y_2O_3 thin film insulator, ZnS:Mn thin film phosphor and ACTFEL devices, which were fabricated by radio frequency magnetron sputtering with the effects of deposition parameters, post deposition annealing temperature, and source material. An extensive study was performed of the thin film Y_2O_3 grown on silicon (100) substrate for its role as a high dielectric constant insulator material. The reproducibility problem associated with this thin film material was addressed whereby the lifetime of the sputtering target was identified to be a contributing factor. The crystallite structural growth of the oxide is empirically compared with its charge properties. In general, the interface state density between the sputtered Y_2O_3 and Silicon has a high value, extending to 10^{13} cm^{-2} eV^{-1} in some discrete state, however the density was significantly reduced by thermal treatment in vacuum. Thin film ZnS:Mn deposited at 200 °C substrate temperature has the best crystallinity both on Silicon and on Y_2O_3 thin film and hence has the best phosphor efficiency. Additionally, annealing the thin film also improved the phosphor efficiency, unlocking the true potential of the phosphor, which was mainly due to an increase in number of radiative sites. The interfacial charge density and distribution at the interface of the insulator/phosphor is shown to be critical in determining the operation characteristics of the ACTFEL device whereby annealing and ageing affects it. Devices annealed at 400°C had the most stable ageing behaviour. SiON insulator ACTFEL device exhibited a large positive shift in LV characteristics, which was primarily due to a decrease in SiON layer capacitance. Both Y_2O_3 and SiON insulators ACTFEL device have advantages and disadvantages associated with their use.

Preface

The need for an interface between the human visual system and machine information database has ensured that optoelectronic displays have a key role in our everyday life. These optoelectronic devices rely heavily on the discipline of optics and solid state physics, which are the fundamental expectation for work on this subject. The interpretation of what is meant by optoelectronic covers the interaction of light with matter in gaseous, liquid or solid form and the devices, which depend on these interactions.

The Cathode ray tube has proved to be an outstandingly efficient light-emitting device with excellent colour capability for use in information displays. However the current push for flat panel displays is quite intense, and much confusion exists as to where development and commercialisation will occur most rapidly. The success of a technology is governed by its survival through the three gateways, which are Market, Management and Technology.

From a technological viewpoint, Thin Film Electroluminescent (TFEL) devices have many advantages such as lightweight, wide viewing angle, solid-state, bright, and high-contrast emission. All these aspects are very amenable for manufacturing a practical flat panel information display.

The purpose of this work is to give an understanding of the technology. Most of the important operation physics are dealt with. This understanding is indispensable for better perception of the failure mechanism and is necessary for a correct measurement of parameters. The stress here is on its underlying assumption and limitations and how one would employ the presented methods to derive the device characteristics of interest.

M. Sethu

Acknowledgements

This thesis would not have been possible without the contribution of many individuals, to whom I would like to extend my thanks,

Firstly, my supervisor and mentor, Professor Clive B. Thomas for providing me the opportunity to undertake this study, his support and encouragement and his challenging methods, which exceptionally contributed toward my personal development as a researcher.

Dr. Wayne M. Cranton, my second supervisor for his contribution, understanding and kindness, which ensured continuous progress of the research programme.

Dr. Costas Tsakonas for his timely help which considerably improved my understanding of semiconductor physics and MIS theory. In this respect, I would also like to thank Dr. Jörg Rüdiger my friend, for his professional support in my work.

Sincere thanks also goes to Dr. Robert Ranson for all his help, especially for the organisation of the fabrication laboratory. The other members of the Optoelectronic research group, A. Liew, D. Koutsogeorgis, T. Nam and my ex-colleagues, Dr. E. Mastio, Dr. M. Craven and Dr. P. Theng for their contribution to the on going success of the team. The technicians of the Electrical & Electronic Division and Judith Kipling from Mechanical Division for all their help during my time at the university.

Prof. J. Silver from Greenwich University for performing the Raman measurements on my samples. Dr. E.K. Evangelou from Ioannina University, Greece for giving me the opportunity to visit that university and broadening my horizon in high-κ thin film materials. Prof. H.S. Reehal from South Bank University for allowing me to use the Ellipsometer for refractive index measurement. EPSRC for loaning me the thermal imaging system.

Dr. R. Stevens from Rutherford Appleton Laboratory for providing the SiON samples and his collaborative participation with the research group. Lite Array Inc., USA for providing the commercial ACTFEL panels and some of the financial support, which kept me motivated.

All my teachers that have been a part of my life, without them I would not have been able to undertake further studies.

My dearest friends both here in the UK and elsewhere for their invaluable support during those challenging periods of my life. The Hindu Youth Group, UK, which actively kept me fit, both mentally and physically.

Finally, I am eternally grateful to my beloved family members for their love, which I have to admit was the most important of all. My brother and sisters for providing me the provisions, which I couldn't have done without. Dr. M.V. Moorthy and Dr. Pushpam Moorthy for their loving attention on my well being during my time in the UK. A heartfelt thanks to Surina, for her continued love, patients and encouragement. My mother to whom I dedicate this thesis for everything she has done for me.

List of Publications

Electrical and Crystallinity Study of Yttrium Oxide Thin Film for use in ACTFEL device, M. Sethu, *PREP 2001, University of Keele, U.K.*

Materials Processing and Device Engineering for Laterally Emitting Thin Film Electroluminescent Miniature Displays, W.M. Cranton, C.B. Thomas, D. Koutsogeorgis, E. Mastio, M. Craven, R. Stevens, R. Ranson, M. Sethu, J. Rudiger, S. Barros, A. Liew, C.Tsakonas and P.Theng, *Microdisplays 2001, Society of Information Displays Digest of Paper, Pg. 102*

Miniature Transverse TFEL Displays, W.M. Cranton, C.B. Thomas, D.C. Koutsogeorgis, R.M. Ranson, S.C. Liew, C. Tsakonas, M.Sethu, *IDMC 1-20.4 2002, Korea*

Electrical and Structural Characteristics of r.f. magnetron deposited Y_2O_3 films on n-silicon, E.K. Evangelou, M. Sethu, C.B. Thomas, S. Cocco, D.T. Dekadjevi, M. Fanciulli, G. Seguini & S. Spiga, *Si-Workshop 2002, Genova, Italy*

Electrical Characterisation of Behaviour and Ageing Mechanism of Alternating Current Thin Film Electroluminescent Device, M. Sethu, C.B. Thomas, C.M. Cranton & R.M. Ranson, *The 7th Asian Symposium on Information Display, 2002, Singapore*

Statement of Original Work

The work presented in this thesis represents the author's contribution to the ongoing research at the Nottingham Trent University. The research programme is to understand the physics and engineering of Thin Film Electroluminescent display devices and to investigate all the mechanisms contributing to device performance. Experimental approach has been demonstrated to achieve this goal.

The author was responsible for the deposition and characterisation of all the thin film materials employed in this programme. The author also designed and commissioned all the characterisation systems as presented in this work, including all the software programmes utilised for the measurements and automation.

Table of Contents

Chapter 2

Experimental Engineering

Chapter 3

Properties of Y_2O_3 Thin Film

Chapter 4

Capacitance Analysis of Y_2O_3 MIS Diode

Chapter 5

Properties of ZnS:Mn Phosphor

Chapter 6

Characteristics of ACTFEL Device

Chapter 7

Thesis Conclusions

Appendix A

Appendix B

Appendix C

Appendix D

Appendix E

List of Equations

List of Equations

List of Figures

List of Figures

List of Figures

List of Figures

List of Figures

List of Figures

List of Tables

List of Abbreviations

A	Ampere
AC	Alternating Current
ACTFEL	Alternating Current Thin Film Electroluminescent
Al_2O_3	Aluminium Oxide
Al	Aluminium
a.u.	Arbitrary Units
$BaTiO_3$	Barium Titanate
$BaSrTiO_3$	Barium Strontium Titanate
°C	Degree Celsius
CATS	Computer Aided Thermograph Software
CCD	Charge Couple Device
CRT	Cathode Ray Tube
CSC	Charge Storage Capacity
CV	Capacitance versus Voltage
DC	Direct Current
DCTFEL	Direct Current Thin Film Electroluminescent
EL	Electroluminescence
eV	Electron-Volts
FWHM	Full Width at Half Maximum
FOV	Field Of View
GPIB	General Purpose Interface Bus
H_2	Hydrogen
H_2S	Hydrogen Sulphide
HV	High Voltage
IV	Current versus Voltage
ITO	Indium Tin Oxide
LASER	Light Amplification by Stimulated Emission of Radiation
LDB	Localised Destructive Breakdown
LETFEL	Laterally Emitting Thin Film Electroluminescent
LV	Luminance versus Voltage

List of Abbreviations

MIS	Metal Insulator Semiconductor
MOS	Metal Oxide Semiconductor
Mn	Manganese
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
N.A.	Numerical Aperture
NTU	Nottingham Trent University
O_2	Oxygen
OpAmp	Operational Amplifier
pA	Pico Ammeter
PMT	Photo Multiplier Tube
PC	Personal Computer
PL	Photoluminescence
QV	Charge versus Voltage
Si	Silicon
Si_3N_4	Silicon Nitride
SiO_2	Silicon Dioxide
SiO_xN_y	Silicon Oxynitride
SO_2	Sulphur Dioxide
Ta_2O_5	Tantalum Oxide
TFEL	Thin Film Electroluminescent
UPS	Uninterruptible Power Supply
UV	Ultra-Violet
wt%	Weight percentage
XRD	X-Ray Diffraction
Y	Yttrium
Y_2O_3	Yttrium Oxide
ZnO	Zinc Oxide
ZnN	Zinc Nitride
ZnS	Zinc Sulphide
ZnS:Mn	Zinc Sulphide doped with Manganese

List of Symbols and Variables

Å	Angstrom
A	Area
a	Lattice constant
α	Phosphor field ratio
α_{op}	Light attenuation coefficient
χ	Semiconductor electron affinity
cm	Centimetre
C_{acc}	Accumulation capacitance
c	Velocity of light (3×10^8 m/sec)
C_{FB}	Flatband capacitance
C_{FBS}	Silicon surface capacitance at flatband
C_i	Insulator layer capacitance in ACTFEL device
C_{ins}	Thin film insulator layer capacitance
C_{inv}	Inversion capacitance
C_m	MIS diode capacitance
C_p	Phosphor layer capacitance in ACTFEL device
C_s	Silicon surface capacitance
C_{se}	Sense Capacitance
Ct	ACTFEL capacitance
°	Degree
ΔC	Change in capacitance
ΔV	Change in voltage
d	Thickness
d_{hkl}	Plane spacing
di	Distance between two charges
d_p	Phosphor layer thickness
D_{it}	Density of interface state traps
εi	Permittivity of the insulator
ε_r	Relative dielectric constant

List of Symbols and Variables

ε_o	Permittivity of vacuum (8.85×10^{-12} F/m)
ε_S	Permittivity of Silicon ($11.9 \times \varepsilon_o$)
E	Energy
E_{bd}	Breakdown field
E_F	Fermi level
E_i	Intrinsic Fermi level
E_{th}	Phosphor threshold field
F	Farad
F_P	Field across the phosphor layer
γ	Charge distribution factor
h	Plank's constant (4.1×10^{-15} eV sec)
hkl	Miller indices
i(t)	Instantaneous current
I_{dis}	Current induced by ACTFEL device capacitance
I_{ext}	Externally measured current
I_0	Maximum intensity
I_T	Tunneling current
k	Boltzmann's constant (1.4×10^{-23} j/K)
kHz	Kilohertz
λ	Wavelength
λ_n	Debye length
L	Luminance
μ	Dipole moment
μC	Micro-Coulomb
mm	Millimetre
MV	Mega-Volt
η	Efficacy
n	Refractive Index
n_i	Intrinsic Silicon carrier concentration (1.45×10^{10} cm^{-3})

List of Symbols and Variables

nm	Nanometre
N_d	Donor doping density
ϕ_m	Metal work function
ϕ_{ms}	Work function difference between metal and semiconductor
ϕ_s	Semiconductor work function
ψ_S	Silicon surface potential
P	Power / dielectric polarisation
q	Charge on the electron (1.6×10^{-19} coulomb)
q(t)	Instantaneous charge
Q	Charge
Q_{ext}	Externally measured charge
Q_f	Oxide fixed charge
Q_{int}	Pre-clamping interface charge
Q_{it}	Interface state charge
Q_m	Mobile ionic charge
Q_{ot}	Oxide trap charge
Q_S	Silicon surface charge
R	Resistance
θ	Angle
θ_i	Incident angle
θ_t	Transmission angle
τ_p	Photoluminescent decay constant
t	Crystallite size
T	Temperature
V	Voltage
V_{bd}	Breakdown voltage
V_{FB}	Flatband voltage
V_G	Gate Voltage
V_{ins}	Voltage across the insulator

List of Symbols and Variables

V_{TFEL}	Voltage across TFEL device
V_{th}	Threshold voltage
W_m	Maximum depletion width
x	Material length

Research is to see what everybody else has seen
and to think what nobody else has thought.

Albert Szent-Gyorgyi

To my mother,
for everything she has done for me

CHAPTER 1

INTRODUCTION

1.1 Electroluminescence

Electroluminescence is a process by which a material generates non-thermal radiation from the excitation of an electron[1]. In 1752, Benjamin Franklin showed this phenomenon caused by electrical discharge occurring on a grand scale in lightning[2]. This method of producing cold light occurs from the excitation of high-energy electrons reacting with a substance, which is unlike the conventional black body radiation from an incandescent tungsten filament. In 1936, French physicist, Destriau observed such light was emitted from the phosphor compound, Zinc Sulphide when a high electric field was applied[3]. This mechanism of producing light has been the basis of many modern phosphor based information displays. The various kinds of phosphor devices and by the manner the phosphor is applied are given in Table 1.1. With the advancement of thin-film process technology in the 1960's and the introduction of a stable Electroluminescence display panel design in 1974[4], a significant amount of the more recent display development efforts has been directed to Thin Film Electroluminescent devices[5]. However, the nature of the device characteristics requires more understanding than that which is available presently, for further improvement to push this technology forward among its rivals.

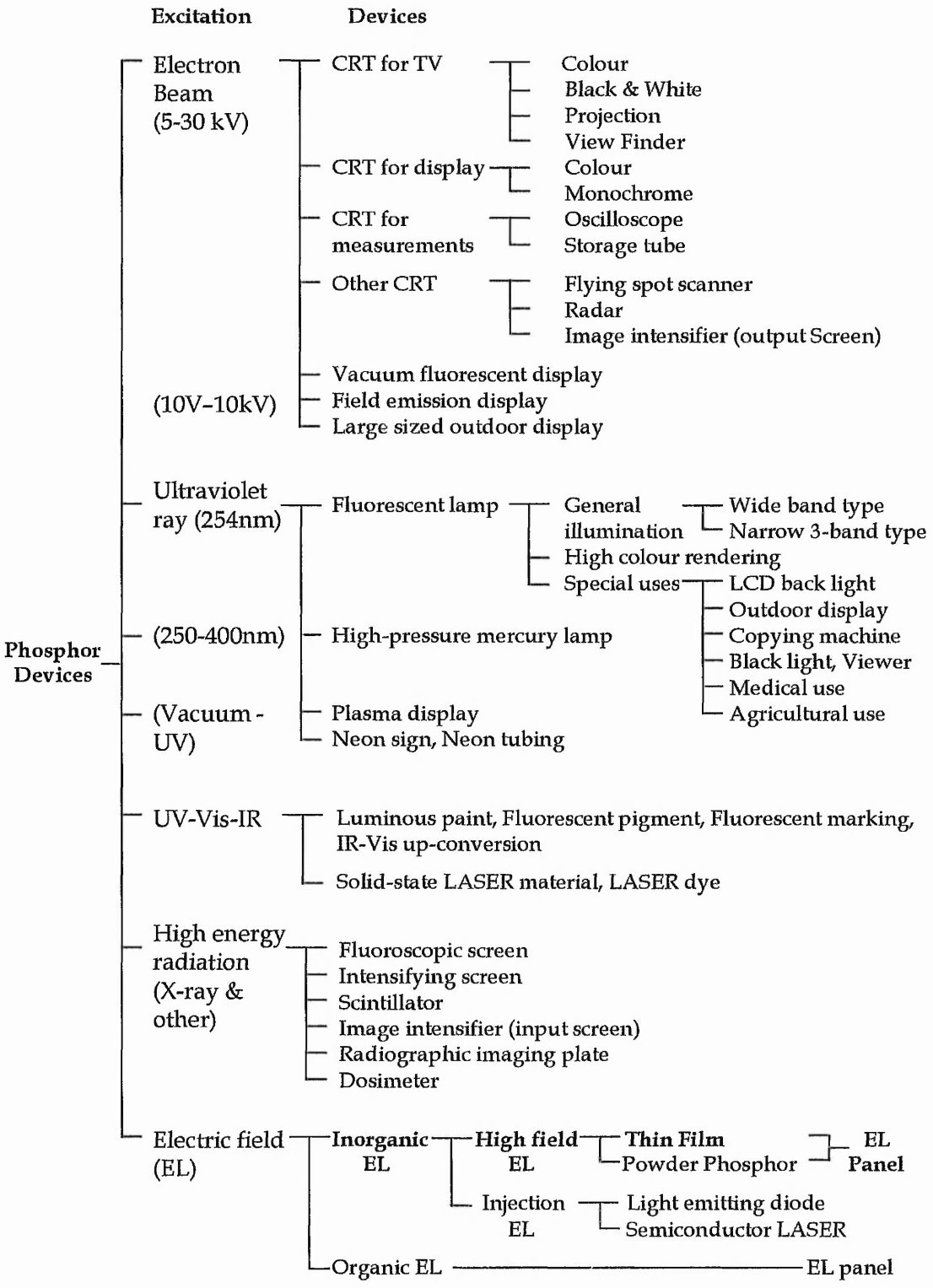


Table 1.1 Phosphor devices and application[6].

1.2 Alternating Current Thin Film Electroluminescent device

A Thin Film Electroluminescent (TFEL) device can be driven by either Direct Current (DC) or Alternating Current (AC). This work focuses on the Alternating Current Thin Film Electroluminescent (ACTFEL) device. This Optoelectronic device is very amenable for manufacturing lightweight, wide viewing angle, solid state, bright, high-contrast and pleasant to the eye emissive flat-panel display. A typical ACTFEL structure is shown in Figure 1.1.

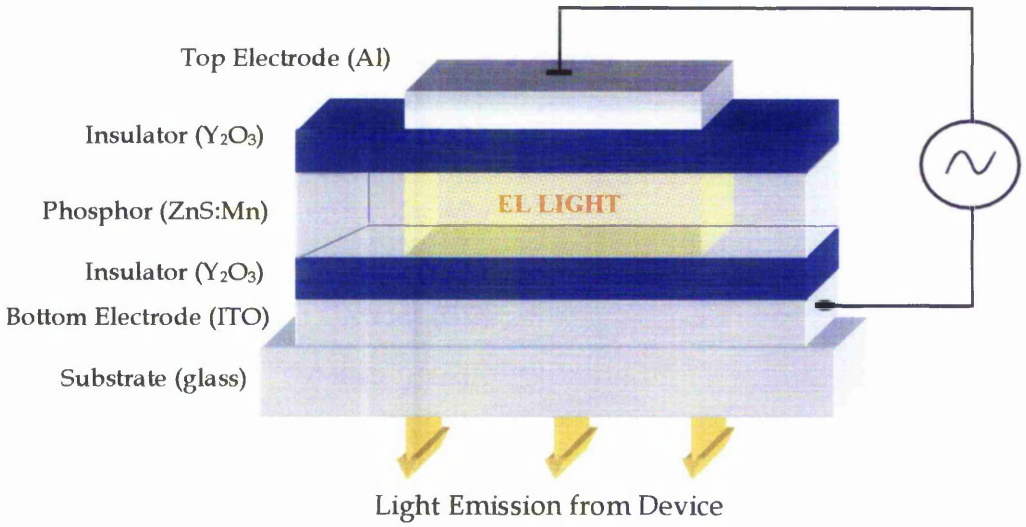


Figure 1.1 Schematic of a typical Alternating Current Thin Film Electroluminescent device[4].

It consists of an active light emitting thin film phosphor, sandwiched between thin film dielectric claddings and electrodes[7,8,9]. Light is emitted from this double-insulator Electroluminescence (EL) device when voltage above threshold (V_{th}) of alternating polarity is applied between the Indium Tin Oxide (ITO) and the top Aluminium (Al) electrodes. Majority of the light produced exits vertically through the ITO electrode. No light is emitted from the Al electrode side as most light would be scattered and reflected from its mirror-like interface.

The phosphor is typically a wide-bandgap semiconductor doped with an activator material[10]. Emission colour can be tuned by doping with different materials. In this study, the phosphor host material is Zinc-Sulphide (ZnS), which is doped with Manganese (Mn). The dopant acts as an activator to produce yellow-orange light[11], centered at 585nm in the visible spectrum with a spectral bandwidth of 40nm[5]. The ZnS:Mn host-dopant combination is the most efficient phosphor[6,12], to date. The EL mechanism can be described with the energy-band diagram of the ACTFEL device[13,14] as shown in Figure 1.2.

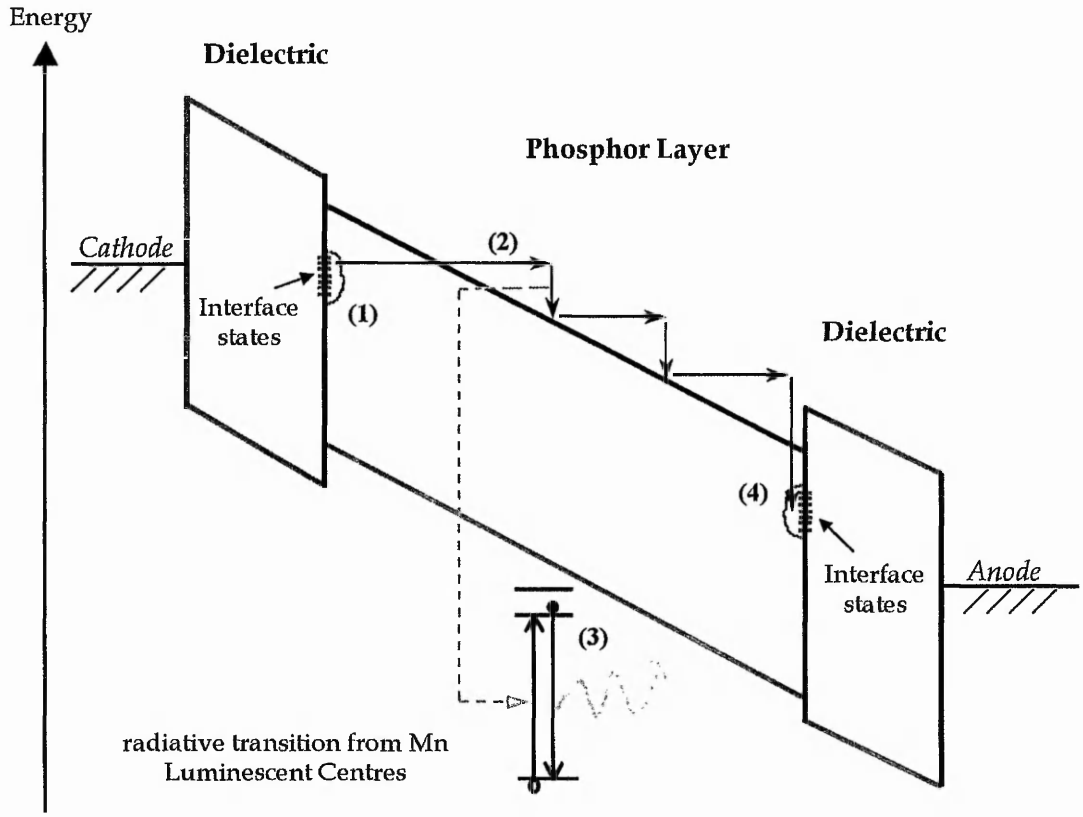


Figure 1.2 Energy-band diagram of the double-insulating-layer-type ACTFEL device, shown for a single polarity. (1) electrons are injected from the interface states by high-field-assisted tunneling. (2) electron accelerates and gains kinetic energy due to applied field. (3) impact-excitation of manganese luminescent centres, which then cause radiative transition. (4) electrons travel through the phosphor to be trapped at the anode phosphor-insulator interface.

The primary source of electrons is located at the ZnS, phosphor-insulator interface, known as interface states[4,13,14,15]. Electrons are injected from the interface states into the conduction band[16] of the phosphor at applied voltage above V_{th} or field across the phosphor layer in excess of 10^8 V/m by high-field-assisted tunneling[17,18].

The alternating voltage on the electrode causes an alternating electric field in the insulator and phosphor layer. Due to the electric field in the phosphor layer, injected electrons are accelerated and gain sufficient kinetic energy to become hot electrons to excite luminescent centres. Excitation is a result of direct impact by hot electrons with activator ions (Mn^{++}) located at luminescent centres. Light is emitted as the activator ions relax from an excited state[13]. Travelling electrons along the phosphor layer, are finally trapped at the phosphor-insulator interface states on the anode side, causing polarisation. When the polarity of the alternating voltage is reversed, the process is repeated in the opposite direction. The interface states serve not only to emit electrons but also to receive and store them[19]. The near-interface polarisation assists the overall field in the next cycle.

Each of the processes described above are essential for the continuous operation of the thin film structure to generate light. In an ideal ACTFEL device, under normal operating condition, these processes should take place without changes in device characteristics, efficiency or operation parameters. The light emission from a TFEL device is given by

$$\boxed{L = \eta P} \qquad \text{Eq. 1.1}$$

where L is the flux in lumens, η is the efficiency in lumens per watt and P is the power dissipated in generating the light. The factors concerning the efficiency are directly related to the engineering of this device. In addition previous study and experiments undertaken for this work demonstrates that brightness degradation and device failure occurs during device ageing, hence reducing efficiency. A review of the potential phenomena responsible for determining the device efficiency and reduction in the performance of ACTFEL device is detailed in the following section.

1.3 Review of EL Performance Mechanisms

1.3.1 Material Properties

As discussed previously, the ACTFEL device consists primarily of a phosphor film sandwiched between two insulators. In this study, ZnS:Mn, phosphor and Yttrium Oxide (Y_2O_3), insulator were mainly used. These materials are deposited using radio frequency magnetron sputtering. Structural analysis has shown that these thin films grown on single crystal (100) silicon wafer using this growth technique are polycrystalline[20,21]. The quality of the crystalline structure of each individual layer grown one on top of another is believed to be dependent upon the base layer used for deposition. Also, fabrication conditions such as growth temperature[22,23], and post deposition annealing[24] affects the thin film material properties.

A polycrystalline structure does impose difficulties in distinguishing fundamental Localised Destructive Breakdown (LDB) from those relating to material artefacts such as grain boundaries and other layer inhomogeneities. A phosphor layer sandwiched by two electrodes is the simplest of an EL device. This type of structure is a typical Direct Current Thin Film Electroluminescent (DCTFEL) device and is the building block of an ACTFEL device. The ZnS:Mn, phosphor layer at low applied field, has high resistivity and is essentially an insulator. Above a critical field, typically between 0.5 and 2.0 MV/cm, current increases rapidly with voltage and simultaneously electroluminescence is observed. Therefore non-uniformity of the layer would pose a serious design flaw, with different threshold voltages. Additionally, non-uniformity would also result in high field region more vulnerable to tunnel breakdown[25]. Study on DCTFEL devices has revealed that the nature of the breakdown event itself and of the associated damage does seem to depend on the crystal quality of the ZnS:Mn layer[26].

The encapsulation with insulators on either side of the phosphor layer forms a capacitive ACTFEL device. The insulator layer is a series capacitor to the phosphor layer with a fraction of the applied voltage dropping across the insulators. Therefore the insulator capacitance will influence the threshold voltage for tunnelling to occur. The

insulators do also provide the current limitation necessary for preventing device failure during normal operation and hence plays an important role in prolonging operating lifetime. Since the insulating material is directly related to the stability of the ACTFEL device[27] it is therefore important to select a high-quality dielectric material for optimum engineering of this device.

The preferred parameters for the insulator are high dielectric constant and breakdown strength, desirable insulator/phosphor electronic interface properties[28], low leakage current[29] in the order of picoAmpere at the operating voltage, stable electro-optical properties during operation and suitable refractive index. It is also important to have a good structural coordination (adhesion) between the insulating layers and the emitting layer[28,30]. In Table 1.2, a summary of the important parameters for some insulators found in literature is given. The table contains a list of materials, which could be used in the construction of ACTFEL devices.

Material	Refractive Index	Energy Bandgap (eV)	Breakdown Strength (MV/cm)	Relative Dielectric Constant
SiO_2	1.4 – 1.5	8.9	10	3.9
SiO_xN_y	1.5 – 2.1	5.1	9 – 26	3.9 – 7
Al_2O_3	1.5	8.7	7	8.5 – 10
Ta_2O_5	2.2 – 2.5	4.2	4.5	25
Y_2O_3	1.9	5.5	3.85	10 - 18
Si_3N_4	2.1	5.1	10	7.5
$BaTiO_3$	2.4	2.5 – 3.9	0.42	300 - 2000
$SrTiO_3$	1.9 – 2.2	3.6	0.3 – 4	150 - 400
$BaSrTiO_3$	2.1 -2.4	3.2 - 4	4	> 870

Table 1.2 A summary of dielectric and optical properties for some insulators material, which could be used in ACTFEL device construction[28,31,32]. The values given are a guideline only because it depends on the deposition parameters.

The crystal structure, light attenuation coefficient and refractive index of the layers are important factors for optical light propagation within an ACTFEL device. This property of the device is explained in Chapter 2. It has been reported that sputtered phosphor films produce disordered polycrystalline columnar structures[33]. Also, the mean grain size of the thin film increases when post-deposition annealing is performed above 450°C, which induces higher saturation brightness[34,35,36]. Therefore, it was an important aspect of this research to correlate the crystalline properties of the thin film with the Electro-Optical behaviour of the ACTFEL device.

Light emission from the phosphor is a cause of direct impact by energetic electrons with activator ions located in favourable location. Generally Mn^{++} ions sit as isoelectronic substitute on a Zn site in the ZnS lattice, to maintain charge neutrality. These sites could potentially become luminescent centres. In an as deposited phosphor film, these locations are initially associated with defects. It has been demonstrated that following an annealing process these ions become located in a more beneficial Zn-vacancies in the crystal lattice to form a more efficient luminescent centres[24,36]. This is evidenced by an increase in saturation brightness and a reduction in the number of non-radiative decay centres, deduced from the increase in decay time constant. Consequently the effect of Mn incorporation with host ZnS lattice as a function of annealing temperature would be an important factor for consideration, which is discussed in Chapter 5.

Two causes of degradation due to the material could be either bulk electron traps within the phosphor or traps associated with interface states. Interface states are presently the primary source of charge, however such states may well be a principal cause of weakness particularly under high field stressing. Some have avoided the use of interface states by utilising injection layers[12], however, these pose new fabrication challenges. It was also found that the chemical volatility between the phosphor and insulator material near the interface causes instability of device characteristics[37,38]. Therefore the study on changes at the interface, which lead to reduction in the efficiency of the device, was carried out. Various techniques are used to relate the effect of these trap properties on device performance, which is presented in Chapter 6.

The optimum Mn concentration for use in ZnS host material is an important parameter to produce a high brightness device[13,39]. In this respect, degradation in crystallinity was observed when the Mn concentration is too high[40,41], which would reduce device brightness. Additionally, at high Mn concentrations, a "red wing" at about 600-620 nm would appear in the spectrum, causing a shift of the peak wavelength towards longer wavelenghts[5]. This is not desirable in certain applications and could also cause instability in the spectrum during operation. Fabrication temperature has been reported to also have an influence on the actual Mn concentration incorporated in the deposited phosphor film[40,42].

It has been suggested that electrons travelling through the phosphor take certain preferred paths[42,43]. It is believed that a preferred path is the result of inhomogeneities in the phosphor layer; also irregularities in the insulator-phosphor interface that cause high field regions where electrons are preferentially emitted. The electrons will excite and exhaust the Mn radiative sites along this route thus reducing the efficiency of the phosphor film. Thus heterogeneity of the Mn distribution maybe a possibility for current non-uniformity within the phosphor layer[35]. Hence structural study was performed on the thin film to provide a better understanding on the influence of the factors that cause the device breakdown and degradation characteristics, presented in Chapters 5 and 6.

Additionally, sulphur vacancies are believed to be responsible for many instabilities in the phosphor. This type of vacancy is believed to produce space charges forming defects in the bulk of ZnS. However, this type of defect can be reduced with the introduction of H_2S in the growth and annealing process, which has demonstrated a promise towards this goal[44]. The existence of space charge could alter device electrical characteristics during operation and may act as a degradation mechanism.

The ACTFEL device is fabricated as a non-aged device structure allowed by the process route designed. When the device is operated by the application of electric field, various changes continuously takes place during its lifetime. The factors, which could influence the device characteristics, will be discussed in the next section.

1.3.2 *Effects of Electric Field*

The ACTFEL device operates with electric fields in the order of 10^8 V/m. Any imperfections in the thin film phosphor or insulators could cause a short between the electrodes and a destructive current of high amplitude to flow through the device. Several types of breakdown are possible due to instabilities within the electrodes. These breakdowns arise mainly from micro breakdowns, which are related to thermal runaway or electronic avalanching within the dielectric layer[35]. Evidence for this is the appearance of arcing propagating as filaments, which travel across the aluminium electrode.

Dielectric breakdown in thin films is one effect of a catastrophic failure of the device and was given priority in the study. This study is important for constructing high efficiency TFEL device[45,46] since it provides an understanding of the maximum field that can be applied to the device before breakdown occurs.

Electroluminescence occurs in a TFEL device when voltage above threshold is applied between the cathode and anode of the device as illustrated in Figure 1.1. The inner field at the cathode interface influences the supply of primary carriers, which determines device brightness. The applied voltage controls the inner phosphor field by the capacitance division ratio between the phosphor and insulator layer. Hence changes in this ratio during operation will shift the Luminance versus Voltage characteristic rigidly along the voltage axis[47,48,49]. However this shift was found not to change the luminance versus input power characteristics[4]. Nevertheless the operating characteristics of the ACTFEL would be influenced. The degree of this degradation effect depends on the type of dielectric material utilised[28,50]. Hence the stability of the electrical properties of the phosphor and insulator layer during operation is very important. It has been reported that atomic rearrangement taking place in the ZnS:Mn layer on the application of high field, alters the device characteristics during the beginning of the ageing process[51].

Polarisation near the interface is also an important part in the operation of an ACTFEL device. The phosphor/insulator interface injects high-energy electrons into the bulk by

high-field-assisted tunnelling. Under AC operation, at the end of each cycle an accumulation of charge occurs at the opposite interface of the device. These charges will be trapped into the interface traps creating a momentary internal polarisation near the interface. This phenomenon is an important characteristic as it increases the effective electric field, thus increasing the overall efficiency of the device in the next cycle[7,47]. However, due to continuous impact of high-energy electrons at the interface, either changes to the interface states or a redistribution of traps could occur; thus influencing the efficiency of this operating mechanism.

The presence of electron traps in the form of sulphur vacancies due to non-stoichiometry between the Zinc and Sulphur of the phosphor material will also influence the electrical behaviour of the device. There is some evidence suggesting that the trap distribution can change over time and hence affect device characteristics. Furthermore, the sulphur vacancies associated with donor traps facilitate Poole-Frenkel emission, in addition to the usual tunnelling from interface states[48]. Hence a reduction occurs in the number of hot electron and the overall luminance of the device. Unpaired Zinc, Sulphur or impurity atoms create isolated ions within the bulk of the phosphor layer and these charges could migrate due to the application of electric field. An accumulation of positive charges at the interface could occur due to continuous device operation. Isolated charge migration has been found to cause asymmetrical device behaviour after some ageing[52,53,54]. Methods of eliminating or reducing sulphur vacancies for example as discussed previously should be of importance in the process of producing TFEL display devices with improved degradation characteristics.

From characterisation of virgin devices, one observation is that the luminance characteristic is not stable during the first few minutes of operation. A plausible explanation for this instability is believed to be associated with changes in the space charge distribution during ageing. Ionised sulphur vacancies are positively charged and are believed to behave as centres to neutralise the negative charges, which affects the device characteristics[55]. A detail and systematic investigation was carried out to identify the cause of this instability with the result being presented in Chapters 5 and 6.

1.3.3 *Environmental Effects*

A good ACTFEL display must provide a reliable operation in a wide range of ambient conditions[28]. However, the environmental operating conditions such as humidity, reactive ambient gases and temperature[56] have an impact on the ageing characteristic of the device. Humidity has been found to be a cause of device degradation[57]. It has been proposed that moisture reaches the ZnS:Mn interface by diffusing through the upper layer of Y_2O_3. Electrolysis of the water molecule could take place during excitation. Hydrogen (H_2) and oxygen (O_2) gases are generated within the device and this gas pressure cause uplift of the Y_2O_3 layer to provide a poor electric field at the ZnS:Mn layer. It has been proposed that a back passivation layer which acts as a protective buffer layer preventing moisture from reaching the active insulator layer could prevent uplifting or peeling of the aluminium electrode[35].

Experiments revealed some of the influences of exposing the operated device in ambient condition. A study was done by operating non-passivated ACTFEL devices in vacuum and in normal ambient conditions with results being presented in Chapter 6.

1.4 Aims

The research undertaken for this thesis was directed towards studying the materials and device parameters, which influence the performance of ACTFEL devices. This involved identifying mechanisms responsible for reducing device performance and for determining the lifetime of this light-generating device.

1.5 Objectives

Investigate the influence of the combination of materials, device processing and operating conditions, on the behaviour of the ACTFEL device.

Identify optimum material processing to improve the individual thin film material utilised in the construction of the ACTFEL device. Characterise the dielectric properties of these materials, and correlate with its structural properties.

Improve understanding of the ACTFEL operation mechanisms, by utilising specialised measurement techniques. Develop experimental characterisation systems to facilitate these measurements.

Utilise understanding to modify the device fabrication processes in order to enhance the device behaviour and indicate the innovations necessary to enhance the performance of ACTFEL device.

1.6 Overview of Thesis

This chapter summarises the history of electroluminescent devices. This is followed by an explanation on the working principles of an ideal ACTFEL device. It also gives a review of mechanisms, which could affect device behaviour. This would provide a background to the aims and objective of the research.

Chapter two details sample preparation and the work to date concerning the design, construction and commissioning of test equipment used in this research with a brief discussion regarding the theory behind each measurement.

Chapter three will discuss the dielectric properties of Y_2O_3 thin films as a function of thickness, growth and processing parameters. It also involves structural studies of the material relating to its electrical characteristics.

Chapter four deals with investigating the integrity of Y_2O_3 thin films. Capacitance analysis technique is presented to explain the nature of various oxide charges. Also given are the interface state density of this thin film with n-type silicon substrate as a function of annealing temperature.

Chapter five details the study done on ZnS:Mn phosphor of its electrical, structural and photoluminescence efficiency as a function of growth and processing parameters.

Chapter six gives the observations made of changes occurring to the ACTFEL device during operation. The causes of the behavioural changes are also given. It also carries results of a comparative study performed on Y_2O_3 and SiON insulators ACTFEL devices.

Chapter seven details the conclusions of the research done for this Ph.D. thesis. Proposals are made for the engineering of an high performance ACTFEL display device utilising Y_2O_3 insulator. It also details the views for further work.

1.7 References

1 J.I. Pankove, Electroluminescence, Springer-Verlag, 1977

2 H.W. Leverenz, Luminescence of Solids 1968, Dover Publications.

3 G. Destriau, Journal de Chim. Physique (France), 33 1936 Pg.587

4 T.Inoguchi, M.Takeda, Y.Kakihara, Y.Nakata and M.Yoshida, Proc. of SID digest 1974 Pg. 84

5 A.N. Krasnov & P.G. Hofstra, Progress in Crystal Growth Characterization of Materials, 2001 Pg. 65

6 S. Shionoya & W.M. Yen, Phosphor Handbook, CRC Press 1999

7 Y.A. Ono, Electroluminescent Displays, World Scientific Publishing Co. Pte. Ltd 1995

8 D.H. Smith, Journal of Luminescence 23, 1981 Pg.209

9 C.N. King, Journal of SID, 4/1 1996 Pg.1

10 G. Blasse & B.C. Grabmaier, Luminescent Materials, Springer-Verlag Berlin Heidelberg 1994

11 H. Kobayashi, S. Tanaka, V. Shanker, M. Shiiki, T. Kunou, J. Mita and H. Sasakura, Phys. Stat. Sol. (a) 88, 1985 713

12 P.D. Rack & P.H. Holloway, Materials Science and Engineering, Reports : A Review Journal, R21 1998 Pg. 171

13 P.M. Alt, Proceedings of the SID 1984, 25/2 1984 Pg. 123.

14 R. Mach and G.O. Mueller, Review Article, Semicond. Sci. Tech.,6 1991 Pg. 305

15 A. Aguilera, V.P. Singh, IEEE Transactions on Electron Devices, 41/8 1994 Pg. 1357

16 S. Bhaskaran, V.P. Singh & J.C. McClure, SID 94 Digest 1994 Pg. 133

17 R. Stevens, A.A. Hassan, W.M. Cranton, International Symposium on optical System, Scotland SPIE Proceedings 2774 1996

18 S.M. Sze, Physics of Semiconductor Devices, 2nd Edition, John Willey & Sons, Pg. 97.

19 E. Bringuier, J. Appl. Phys. 66/3 1989 Pg. 1314

20 E.A. Mastio, M.R. Craven, W.M. Cranton, J. Appl. Phys. 1999 Pg.2562

21 Y. Nakanishi, Y. Fukuda, Y. Hatanaka, Appl. Surface Science 1991 Pg.297

22 A. Mikami, K. Terada, K. Okibayashi, J. Appl. Phys. 1992 Pg. 773

23 T.R.N. Kutty, J. of Thin Solid Films 1985. Pg. 223

24 A.F. Cattell, A.G. Cullis, 5th International Thin Film Congress 1981.

25 J.G. Rascon, V.P.Singh, J.C. McClure, F.S. Pool & D.C. Morton, Proceedings of 8th Int. Workshop Inorganic and Organic Electroluminescence, 1996, Pg. 153

26 A.P.C. Jones, D.Y. Watts, A.W. Brinkman, J. of Crystal Growth 1986 Pg. 880

27 S.S. Sun and R Khormaei, SPIE, 48 1992 Pg. 1664

28 A.N. Krasnov, Thin Solid Film (Review article), 347, 1999 Pg. 1

29 J.C. Hitt & J.F. Wager, J. Appl. Phys., 90/6 2001 Pg. 2711

30 Y. Nakanishi, S. Mori, T. Nakamura, H. Tatsuoka, H. Kuwabara & Y. Hatanaka, Mat. Chem. & Phys., 43 1996 Pg. 292

31 G.D. Wilk, R.M. Wallace & J.M. Anthony, J. Appl. Phys. (Review), 89/10 2001 Pg. 5243

32 T.S. Nam, Private Communication, Nottingham Trent University.

33 T. Matsuoka, J. Kuwata, M. Nishikawa, Japanese J. Appl. Phys. 1988 Pg. 592

34 A. Izrael, P. Thioulouse, R. Tueta, Journal De Physique 1984. Pg. 903

35 R. Menn, R. Tueta, Izrael, International Display Research Conference 1982. Pg. 38

36 A. Fuh, R.P. Gallinger, P.Schuster, J. Adolph & O. Caporaletti, Thin Solid Films, 207 1992 Pg. 202

37 Y.H. Lee, I-J. Chung & M-H. Oh, Appl. Phys. Lett. 58/9 1991 Pg. 962

38 T. Matsuoka, M. Nishikawa, J. Kuwata, Y. Fujita, T. Tohda & A.Abe Japanese J. of Appl. Phys., 27/8 1988 Pg. 1430

39 W.M. Cranton, Ph.D. thesis, University of Bradford 1995.

40 H. Xian, P. Benalloul, C. Barthou, Thin Solid Film 1994. Pg. 193

41 C-W. Wang, T-J. Sheu, Y-K. Su & M. Yokoyama, Japanese J. Appl. Phys., 36/1/5A 1997 Pg. 2728

42 S. Gupta, J.C. McClure, V.P. Singh, Thin Solid Films 1997. Pg. 33

43 A. Izrael, R. Menn, P. Thioulouse, 8th European Congress on Electron Microscopy 1984 Pg. 1265

44 C. Tsakonas, C.B. Thomas, J. Appl. Phys. 1995 Pg. 6098

45 W.E. Howard, IEEE Transactions on Electron Devices, Ed. 27/7 1977 Pg. 903

46 S.K. Tiku & S.H. Rustomji, IEEE Int. Display Research Conference, 1988 Pg. 36

47 R.Mach , in 5th International Workshop Electroluminescent 1990. Pg. 85

48 G.O. Müller, Regina Mach, Roland Reetz, SID 1988 Pg. 23

49 M.K. Jayaraj & CpG. Vallabhan, Bull. Mater. Sci., 14/1 1991 Pg. 49

50 R. Mach & G.O. Muller, Springer Proc. in Physics, 38 1989 Pg. 264

51 N.A. Vlansenko, A.I. Beletskii, Z.L. Denisova, Ya.F. Kononets & L.I. Veligura, Proceedings of 8th Int. Workshop Inorganic and Organic Electroluminescence, 1996, Pg. 259

52 J-I Watanabe, M. Wakitani, S. Sato & S. Miura, SID Digest 1987 Pg. 288

53 S. Shih, P.D. Keir & J.F. Wager, J. Appl. Phys., 79/9 1995 Pg. 5775

54 A.Abu-Dayah & J.F. Wager, J. Appl. Phys., 75/7 1993 Pg. 3593

55 R. Khormaei, N.K. Christopher, E.C. Richard, SID Proceedings 1991 Pg.74

56 B. Soenen, J.V. Bossche & P.D. Visschere, J. Appl. Phys., 82/10 1997 Pg. 5241

57 K. Okamoto, M. Wakitami, S. Sato, S. Miura, S. Andoh & S. Umeda, SID proceedings 1983. Pg. 16

CHAPTER 2

EXPERIMENTAL ENGINEERING

2.1 Hypothesis of the Experiments

The investigation of ACTFEL mechanisms responsible for reducing device performance involved, firstly, the interrogation of the individual layers used in the construction of the device. Therefore the thin film materials were first deposited as individual layer on semiconductor substrates. Emphasis was then placed on the measurement and characterisation of each material's properties as a function of fabrication parameters to ascertain the optimum condition. A series of characterisations, which involved electrical and structural study, was performed on the thin film materials.

Specifically engineered measurement systems were then used to investigate ACTFEL devices in relation to the material properties. This chapter deals with the design details of the fabrication and measurement systems utilised for this study.

2.2 Fabrication of the ACTFEL device

2.2.1 Thin Film Deposition

The fabrication of an ACTFEL device involves sequential deposition of the individual layers described in Chapter 1 on the surface of a substrate. The individual thin film layers were sputter deposited onto n-type 100mm Silicon single crystal substrate unless otherwise stated. The growth chambers designed, commissioned and maintained by the NTU Optoelectronic Research group utilise radio frequency magnetron sputtering in an argon environment[1]. The schematic of the chamber design is shown in Figure 2.1 and a picture of the main fabrication chamber in shown is Figure 2.2.

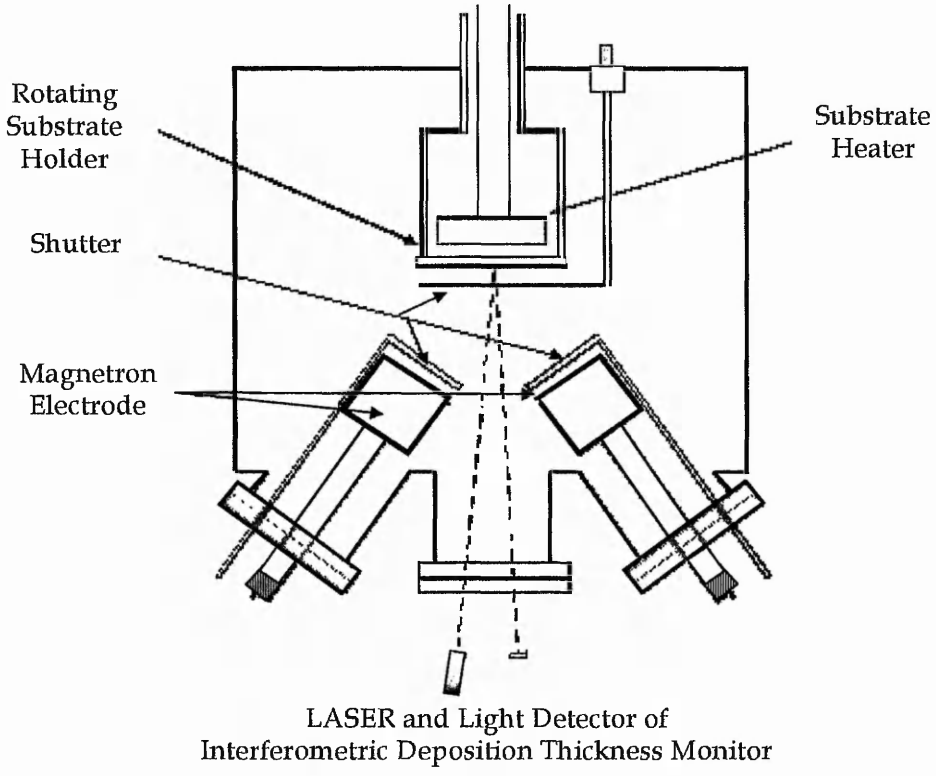


Figure 2.1 Schematic layout of the chamber configuration utilised for the depositions of the thin film materials.

All films of Y_2O_3 and ZnS:Mn used for this research were fabricated utilising this chamber. The pre-growth chamber base pressure is maintained via a diffusion pump at nominally 2.0 x 10^{-7}mbar. During deposition the argon pressure is maintained at approximately 4 mbar. For Y_2O_3 thin film deposition, the substrate temperature was maintained at 190 °C, utilising a substrate heater shown in Figure 2.3. In a previous investigation, it was found that at this temperature the dielectric has the best properties[2]. Also, it was found that this dielectric thin film grown at 200 °C produced a good crystalline ZnS film grown over the dielectric layer[3]. In addition, high deposition temperatures were found to make the dielectric more sensitive to post-deposition treatment[4]. In the case of ZnS:Mn, the deposition temperature was varied to study the optimum condition with the results being presented in Chapter 5.

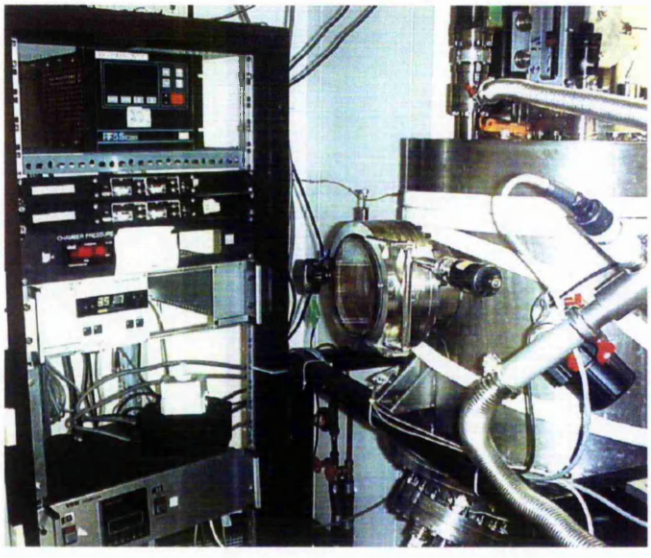


Figure 2.2 Picture of the main radio frequency sputtering chamber utilised to deposited the Y_2O_3 and the ZnS:Mn thin films for this research.

Prior to deposition, the substrates were prebaked under vacuum at 750 °C to remove moisture on the surface of the wafer. The deposition plasma is created by applying 120W power to the 7.5cm diameter target, positioned 15cm from the substrate. The Y_2O_3 target is a solid target with a purity of 99.9%, manufactured by Cerac Inc. For ZnS:Mn,

pressed powder and solid targets were used from a source material manufactured by Phosphor Technology Ltd.

During deposition the wafers were rotated at 10 rpm to improve uniform film growth, at the preset growth temperature. The thickness of the growing films was monitored in-situ using an interferometric technique[5]. The LASER utilised has a wavelength λ of 650nm. Using the condition for destructive interference in the thin film, the thickness t of the film could be calculated by Eq. 2.1.

$$t = \frac{m\lambda}{2n} \qquad \text{Eq. 2.1}$$

where m is the order number of sequential minima (or maxima) and n is the refractive index of the thin film deposited.

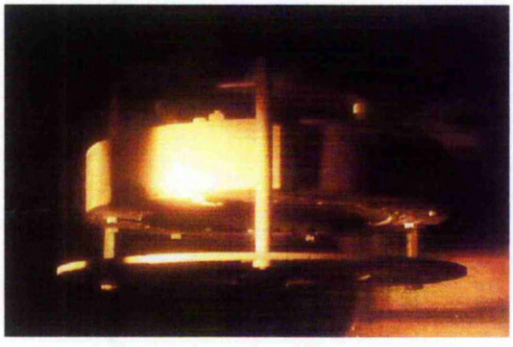


Figure 2.3 Picture of the substrate heater used for maintaining the substrate temperature during deposition and for post-deposition annealing.

Post-deposition annealing was performed using a substrate heater in the same multi-purpose chamber in vacuum under 2.0×10^{-7} mbar unless otherwise stated. In order to maintain minimum growth tolerance between different annealed samples, some of the 100mm wafers were cleaved to smaller piece and each piece annealed individually at different temperatures. The annealing temperatures investigated are 200, 300, 400, 500 and 600 °C in comparison with non-annealed samples grown at 190 °C.

2.2.2 *Metalisation and Patterning*

Aluminium (Al) contacts with a thickness of approximately 200 nm were formed by thermal evaporation in vacuum under 1 x 10^{-6} mbar. Utilising a Stainless Steel contact mask such as shown in Figure 2.4 and Figure 2.5, aluminium patterns were formed on the top surface of the thin film. In some cases, especially for thin film capacitance measurements, 300 nm thick Al was deposited on the silicon surface by thermal evaporation in order to improve electrical back contact.

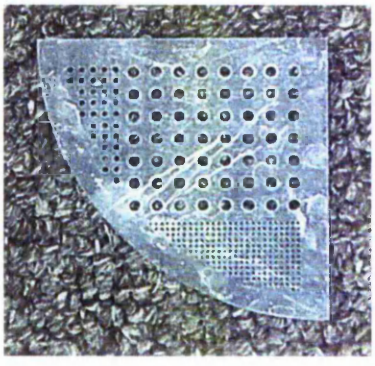


Figure 2.4 Stainless Steel contact mask used to deposit aluminium electrode on the surface of thin films to form diodes. The largest hole has a diameter of 2mm, medium is 1mm and the smallest being 0.5mm. These circular diodes are used for MIS study described in Section 2.3.3.

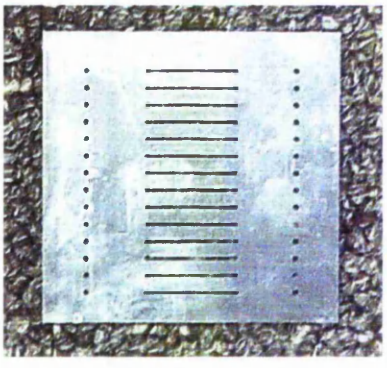


Figure 2.5 Stainless Steel contact mask used to deposit aluminium electrode on the surface of thin films ACTFEL structure to form edge-emitters device described in Section 2.4.2.

2.3 Electrical Characterisation

2.3.1 High Voltage Amplifier

A High Voltage (HV) power Amplifier was specifically designed and constructed for operating the ACTFEL device. This fundamental unit was primarily used in the characterisation of ACTFEL devices for this study. The amplifier utilises Apex PA89 high voltage Operational Amplifier (OpAmp) driven from four International Power supply module IHB250, enabling the amplifier to reach 1000V peak to peak. The amplifier is set to have a maximum output current of 55mA. A circuit diagram and the OpAmp datasheet is included in Appendix A. A Thurlby Thandar Programmable Function Generator TG1010, is used for waveform generation. The function generator has the capability to be remotely programmed via a Personal Computer (PC) and define parameters for the output waveform. The amplifier with a set gain of 50 is used to amplify the signal to a level required for ACTFEL device operation and testing.

2.3.2 ACTFEL Current and Charge measurement

Employing a sense capacitor or resistor in series with the ACTFEL device, Charge-Voltage (QV) or Current-Voltage (IV) measurements can be performed. These measurements are important tools for modelling the ACTFEL device to account for the electrical behaviour in response to the drive voltage. In Figure 2.6, a schematic diagram of the circuit configuration is given. The resistor, R is used to measure the instantaneous current flowing through the device. The capacitor, C_{se} is connected in series to the device to form a Sawyer-Tower circuit[6]. This circuit is used to measure the instantaneous transferred charge within the ACTFEL device during operation. A large sensing capacitor is employed to minimise the voltage drops across C_{se}, hence minimising the effect on device operation. The R and C_{se} values used are 1 KΩ (1%) and 100 nF (%5) respectively. The actual C_{se} value (considering the capacitor tolerance and line capacitance) at the device probing point was measured, using a calibrated capacitance meter. The measured C_{se} value is 98.6 nF.

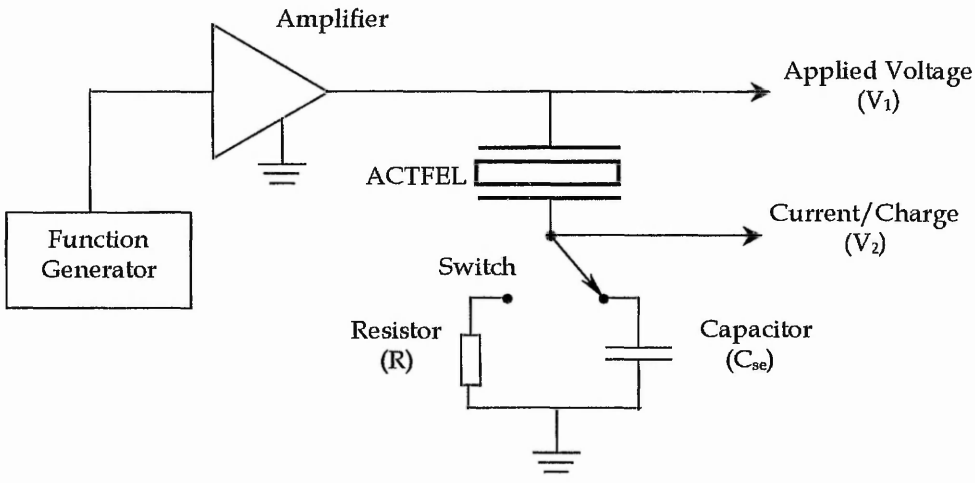


Figure 2.6 Block diagram of the Current/Charge measurement unit. V_1 represents the horizontal and V_2 represents the vertical display axis on an oscilloscope, which yields the IV or QV curve.

QV or IV plot for the ACTFEL device were obtained via an oscilloscope linked to a computer. The Lissajous plot is obtained by connecting points V_1 and V_2 to the oscilloscope inputs whereby the resulting motion is the sum of two independent oscillations[7]. The high input impedance of the oscilloscope will ensure minimum discharging occurs into the measurement unit. More details are given in Section 2.4.1. The instantaneous voltage drop across the ACTFEL device $V_{TFEL}(t) = V_1(t) - V_2(t)$, where $V_2(t)$ is the voltage drop across the sense component measured for high voltage AC signal applied to the circuit. The switch is used to select the sensing component enabling either current or charge to be measured.

The instantaneous charge in the device may be calculated by utilising Eq. 2.2

$$\mathbf{q(t) = C_{se} \times V_2(t)} \qquad \text{Eq. 2.2}$$

and the instantaneous current through the device may be calculated by using Eq. 2.3.

$$\mathbf{i(t) = V_2(t) / R} \qquad \text{Eq. 2.3}$$

2.3.3 *Capacitance, Current and Breakdown Measurement*

A dedicated Capacitance/Current as a function of a Voltage (CV/IV) probe station was constructed for thin film material electrical characterisation. Pictures of the system are shown in Figure 2.7. Capacitance is measured using a Hewlett Packard 4192A, LF Impedance Analyser. Current is measured using a Hewlett Packard 4140B, Pico Ammeter (pA). The probe station is encapsulated in a metal cabinet to avoid magnetic and ambient light interference during measurement.

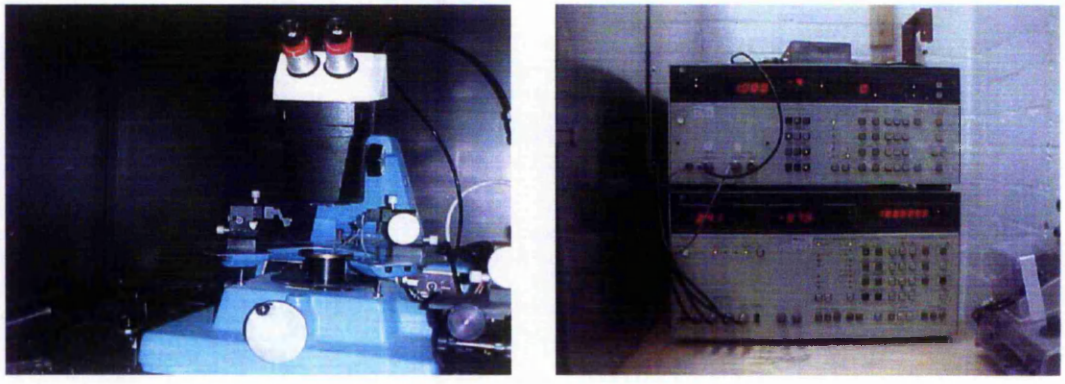


Figure 2.7 Left - Picture showing the Probe Station. Right - Picture of the Capacitance-Bridge, HP 4192A and Current meter, HP 4140B. The Probe station is placed in a darkened and electrically shielded cabinet.

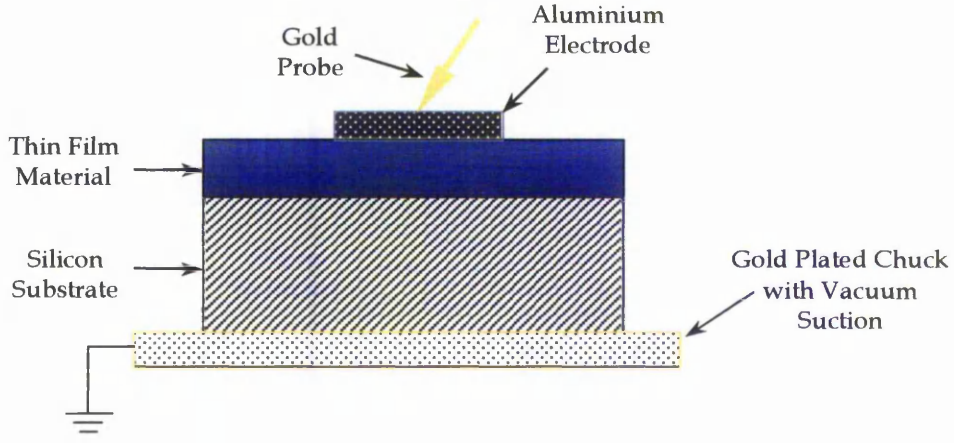


Figure 2.8 Cross section of Metal Insulator Semiconductor diode testing schematic.

CV and IV measurements were carried out on Metal Insulator Semiconductor (MIS) structures as shown in Figure 2.8. Probing on to the Aluminium metal contact is performed using a 0.2 mm gold wire probe.

A typical CV curve of an MIS structure with n-type silicon is shown in Figure 2.9. The graph could be divided into three regions corresponding to, accumulation, depletion and inversion. The theory behind the measurement and the regions are detailed in Chapter 4.

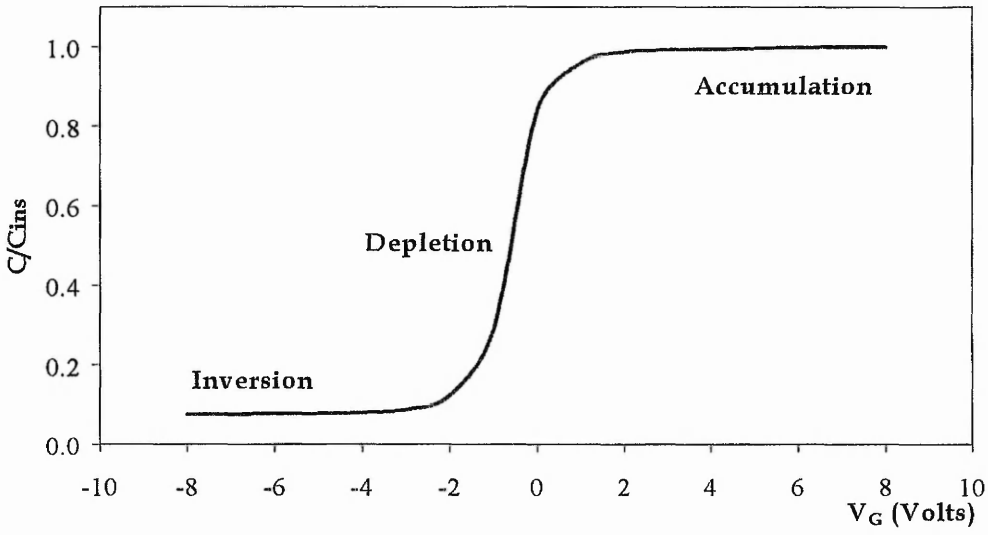


Figure 2.9 A typical normalised Capacitance versus Voltage characteristics for a Metal Insulator Semiconductor diode of n-type silicon.

In the accumulation region, the measured capacitance is primarily due to the insulator capacitance. Therefore it is possible to determine the relative dielectric constant (ε_r) of the insulating material from the capacitance at accumulation solely from geometry.

The Capacitance of the insulator is given by[8]:

$$C_{acc} = \frac{\varepsilon_r \varepsilon_0 A}{d} \qquad \text{Eq. 2.4}$$

where C_{acc} is the capacitance in the accumulation region, ε_r is the relative dielectric constant of the material, ε_0 is the permittivity of vacuum given to be 8.8542×10^{-12} F/m,

with the capacitance being measured for the area A of the active material (i.e. the area of the top electrode) and d is the thickness of the thin film material.

Leakage currents through the insulator were studied using similar MIS structures. The current measurements were taken at intervals of 5-sec with 0.5V step size. Extending this measurement to breakdown facilitates a dielectric breakdown test, where breakdown voltage is the voltage necessary to provide rapid increase in current either due to avalanching or thermal runaway within the dielectric. Thermal breakdown in a material is a consequence of Joule heating generated by current flow whereas Avalanche breakdown is due to quantum mechanical tunneling of electrons from the valence band to the conduction band[9].

Breakdown Voltage, V_{bd} is measured by increasing the DC voltage across the thin film material gradually up to a point where catastrophic current flows through the diode.

Hence breakdown field, E_{bd} is,

$$E_{bd} = \frac{V_{bd}}{d} \qquad \text{Eq. 2.5}$$

AC breakdown voltage measurements were also performed utilising a resistor as a current sensor, described in the previous section. A HV 5kHz sine wave was used for this measurement as it was also used to drive the ACTFEL devices. The peak voltage applied across the diode is ramped up until a catastrophic sudden increase in current is observed and was recorded as the insulator V_{bd}.

E_{bd} and ε_r are some fundamental characteristic of an insulating material, and are used as a figure-of-merit, known as Charge Storage Capacity (CSC) at breakdown

$$CSC = \varepsilon_r \varepsilon_0 E_{bd} \qquad \text{Eq. 2.6}$$

2.4 Luminance and Imagery Characterisation

2.4.1 *Computerised Probe Station*

A computer controlled system was designed and commissioned to perform automated characterisation measurements on the ACTFEL device. It could perform measurements of brightness, current, charge, video capture during ageing measurements with user defined waveform drives to excite the probed ACTFEL device. The system arrangement is shown schematically in Figure 2.10. The probe station is a Xynetics Wafer Prober Model 1034X6A that was rebuilt by Harmbridge Ltd. It is fitted with a Charge Coupled Device (CCD) camera for optical alignment and dynamic monitoring of the device under test during measurement.

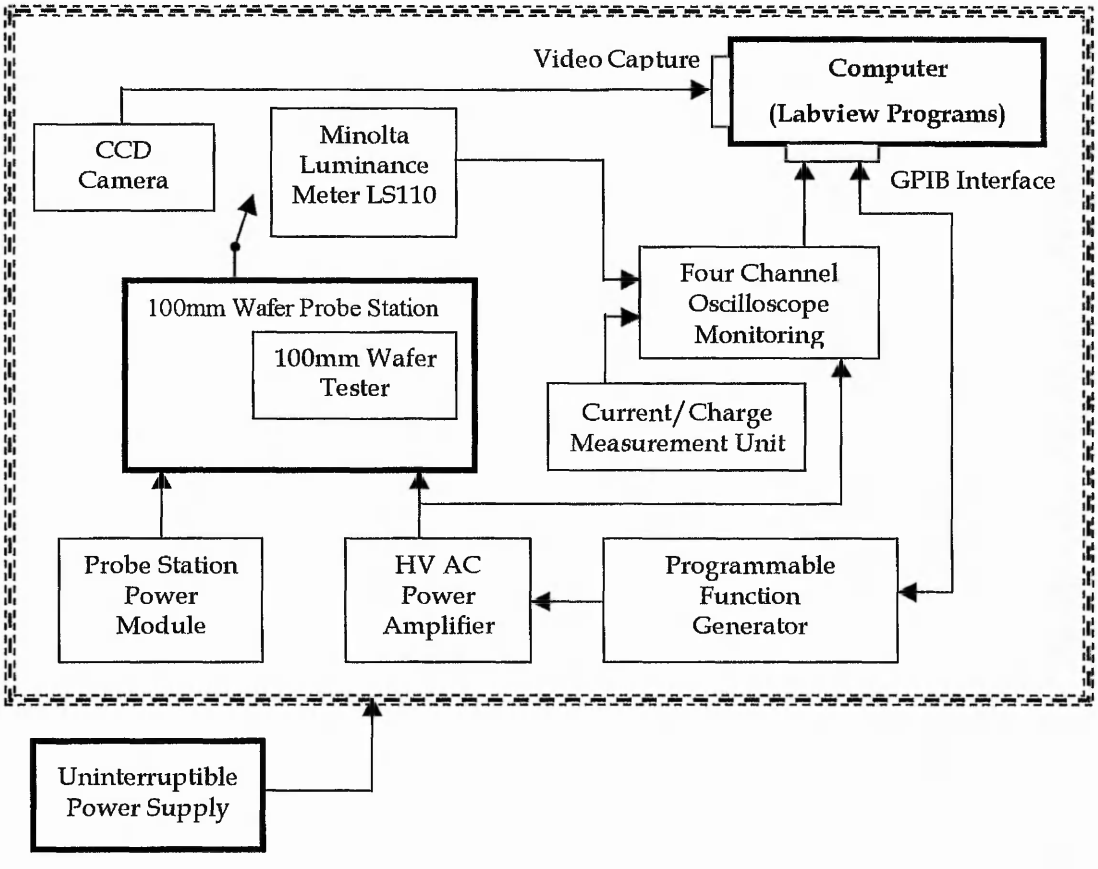


Figure 2.10 Schematic diagram of the computerised wafer Probe Station utilised for ACTFEL device characterisation.

The probe station is encapsulated in a metal cabinet to avoid magnetic and ambient light interference during measurement. Picture of the probe station is shown in Figure 2.11 and the control unit in Appendix B. The system is placed in a class 10 clean room for controlled environmental conditions. All equipment is powered from Patriot SMT1000T Uninterruptible Power Supply (UPS) system with 1000VA capacity and up to 15 minutes blackout runtime. The UPS facilitates backup procedure, during a mains power failure.

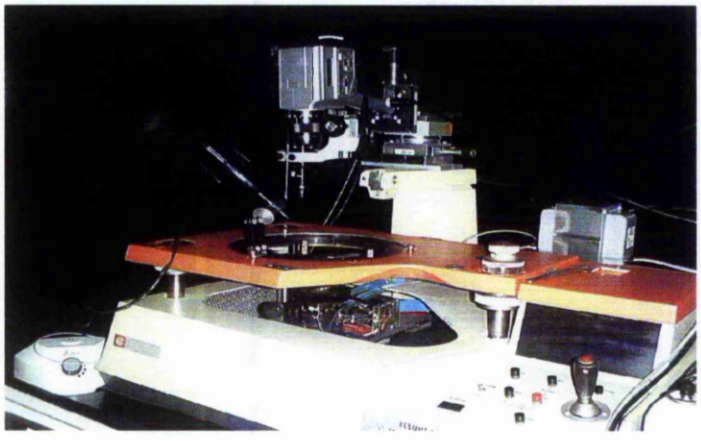


Figure 2.11 Picture of 1034X wafer Probe Station, with facility of luminance and video monitoring of ACTFEL display device.

The Pulnix TM7A CCD camera is used for optical alignment of the device that requires probing and investigation. The video signal from the camera is read via a video capture card. With this arrangement the system has the ability for continuous video monitoring of the device. On the same arm of the CCD camera, a Minolta LS110 luminance meter is attached. It is possible to switch between the CCD camera and the luminance meter, which feeds continuous luminance information of the device under test to the computer via a Tektronix TDS220 oscilloscope. Another oscilloscope of similar type is used to monitor the voltage applied across the ACTFEL device. A total of four channels could be monitored at any given time, which includes the transferred charge or current through the ACTFEL device. The computer communicates with the oscilloscope and function generator via a General Purpose Interface Bus (GPIB) port. All measurements performed are controlled via specific programs developed by the author using Labview programming language. (Subroutine hierarchy diagrams are given in Appendix E)

2.4.2 *Edge Emission Luminance Measurement*

The Lateral Emitting Thin Film Electroluminescent (LETFEL) device structure has been a pioneering work at NTU, Optoelectronic Research group[10,11,12].

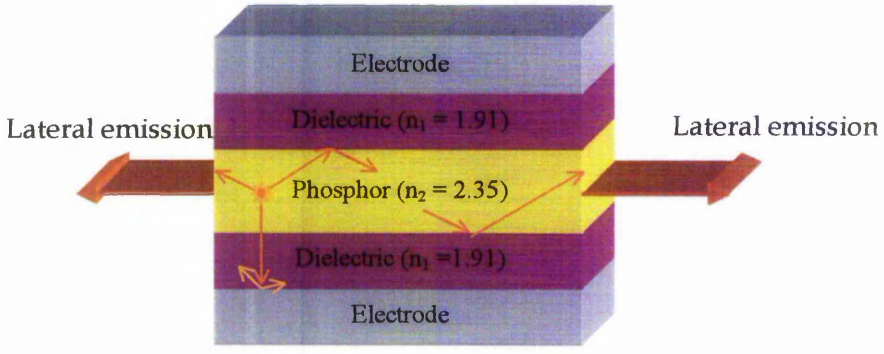


Figure 2.12 Schematic cross section of ACTFEL device structure showing lateral emission.

The double insulating layer structure of the ACTFEL device causes a light-trapping (or wave-guiding) effect in the ZnS:Mn phosphor layer. This effect is due to the total internal reflection occuring at the phosphor and dielectric layer interface[13] by incident light greater than the angle of total reflection, according to Snell's law :

$$n_2 \sin\theta_i = n_1 \sin\theta_t \qquad \text{Eq. 2.7}$$

where θ_i is angle of incident to the interface and θ_t is the transmission angle relative to the normal of the interface. n_2 and n_1 are the refractive indices of the two materials, ZnS:Mn phosphor and Y_2O_3 insulator respectively. A Plas Mos SD 2100 Thin Film Measurement system was used to measure the refractive index, which revealed n_2 to be 2.35 and n_1 to be 1.91, measured as individual layers on Silicon (100) substrates. Utilising Eq. 2.7, for total internal reflection with θ_t=90°, would give the critical incident angle to be 55°. Assuming each Mn site is an isotropic source, the majority of the EL emission is trapped within the phosphor layer operating as an optical waveguide as shown in Figure 2.12. Furthermore the metallic electrode interface of this type of structure would scatter light at its mirror like surface, causing most light to be highly attenuated in the plane normal to the interface.

In effect, the luminance efficiency is much greater at the edge of the thin film structure[1] and provides the reason for the edge-out measurements. The preparation of the sample is the same except that the emission facet is at the edge. In order to access this point the wafers are cleaved using two sharp objects, e.g. tweezers, as shown in Figure 2.13.

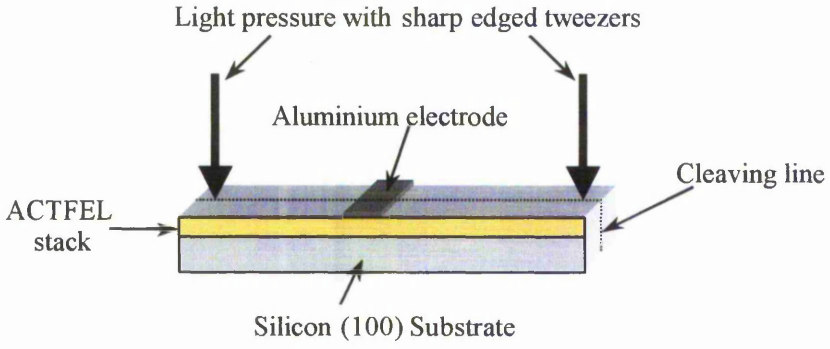


Figure 2.13 Diagram showing the process of cleaving a TFEL device in preparation for an edge-out device.

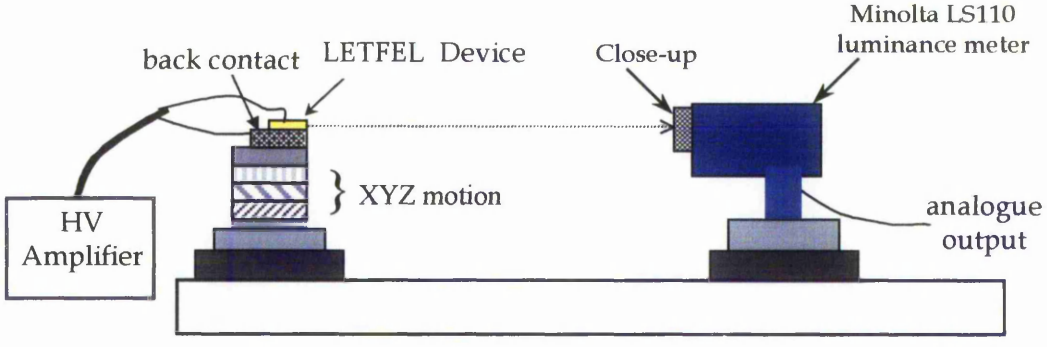


Figure 2.14 A schematic diagram of the LETFEL Edge-out EL measurement system.

The measurement system was designed to operate principally the same way as the probe station, explained in the previous section with the exception being that the direction of the light is parallel to the surface of the TFEL device. The schematic of the system is shown in Figure 2.14. A Close-up lens is attached to the luminance meter, since the measurement area of the TFEL device is small. The Minolta close-up lens No.122 has a measuring diameter of 1.1 mm at the measuring distance of 323mm. A Photo Multiplier Tube (PMT) is also used to detect light generated from the ACTFEL device. This arrangement for transient luminance capture is shown schematically in Figure 2.15.

The use of a PMT enables the capture of high-speed luminance variations at each interface due to excitation of AC high fields driven at frequencies up to several kHz. In Figure 2.16, a picture of an edge-emission device test block is shown whereby EL light is collected via a fibre optic cable. The fibre optic cable could also be fed into a visible light spectrum analyser. The spectrum analyser used is Ocean Optics model S2000, which can perform radiometric luminance measurement over wavelengths between 350nm and 850nm.

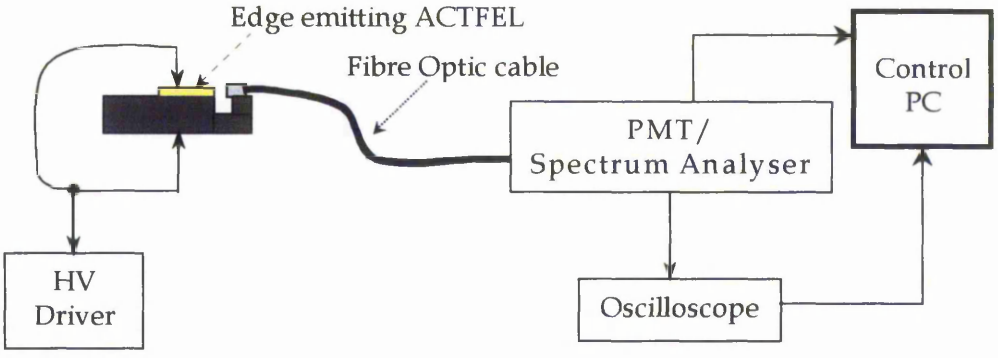


Figure 2.15 Transient/Spectrum Analyser measurement configuration for LETFEL device.

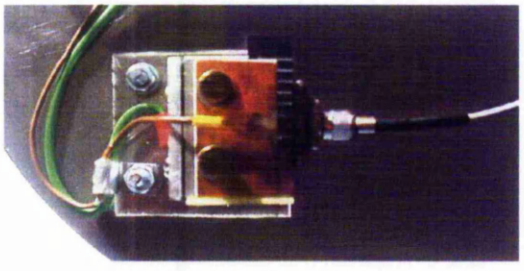


Figure 2.16 A picture of the edge-emission fibre optic luminance detection block for ACTFEL display device.

Another important parameter in LETFEL operation is the light guiding property of the phosphor material. Changes in light attenuation coefficient (α_{op}) of the phosphor material, which maybe caused by structural differences (Chapter 5) or due to electric field stressing will influence the efficiency of lateral emission. A novel measurement technique is proposed in Section 7.3.4 to investigate this parameter.

2.4.3 *Photoluminescence Measurement*

Photoluminescence (PL) is a characteristic of a phosphor material. When photons of high enough energy excite a phosphor material, luminescence would transpire, hence it is called a photoluminescent process. This characteristic can be used to provide a non-destructive technique for determination of certain impurities in a host material.

The phosphor host material used in this study is Zinc Sulphide (ZnS), which has an energy bandgap of 3.6 eV. By shining this material with photons of higher energy than the bandgap energy, electrons will be excited from the valence band into the conduction band. The recombination process, which is the decay of the excited electrons from the Excited state to the Ground state in the atomic transition of the Manganese (Mn) dopant system could produce a radiative transition. Therefore the efficiency of the phosphor material (a measure of number of radiative centres) could be determined by means of this technique.

A LASER Science inc., VSL-337ND Nitrogen LASER source was used for the excitation. The LASER has an output wavelength, λ of 337nm with 6mW of average power at 400 x 10^{-6} joule energy/pulse. The photon energy can be calculated using Eq. 2.8, given below

$$\mathbf{E} = \frac{\mathbf{h\,c}}{\lambda} \qquad \text{Eq. 2.8}$$

where h is Planck's constant given by 4.1 x 10^{-15} eV second and c is velocity of light given by 3 x 10^{8} meter/ second. The calculated photon energy for the Laser source is 3.6645 eV.

A schematic diagram of the PL measurement system is shown in Figure 2.17. The spectrum analyser, described in the previous section is used to study the spectrum of the photoluminescence of the excited phosphor.

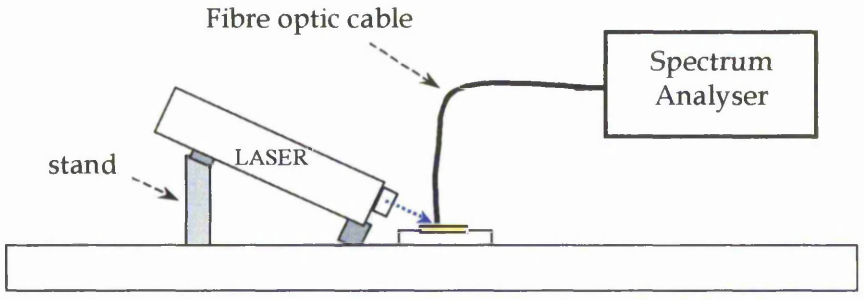


Figure 2.17 Schematic arrangement for Photoluminescent measurement.

The Laser utilised has a pulsed Ultra-Violet (UV) output. The pulsed excitation allows the photoluminescent decay constant (τ_p) to be investigated[14]. It has been found that τ_p has a relationship with the number of luminescent centres in the phosphor[15]. The phosphor material constant, τ_p is determined from the photoluminescence decay profile using a curve fitting routine. The light detector used for this transient measurement is the PMT described in the previous section. The decay constant of interest is only of the peak photoluminescent wavelength. Therefore a 10nm band-pass filter at 580nm light wavelength was used near the fibre optic light pickup. A picture of the arrangement is shown in Figure 2.18.

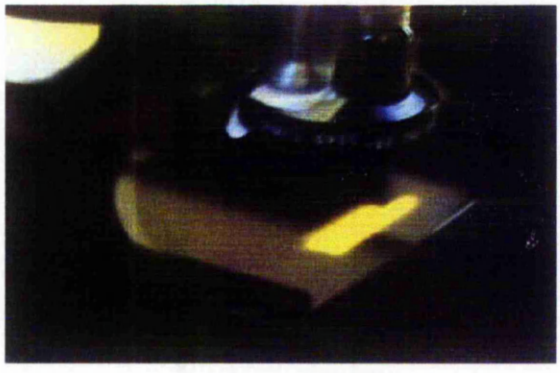


Figure 2.18 A picture of an optical 10nm band-pass filter at 580nm wavelength in the way of the fibre optic cable, used for transient Photoluminescent measurement. The yellow light seen at the centre of the wafer is the photoluminescence of a thin film ZnS:Mn.

2.4.4 *Thermal Imaging*

An Agema Infrared system, Thermovision 880 was used to capture Electro-magnetic energy radiation from the surface of ACTFEL devices. This measurement was performed to investigate the generation of heat from the device during operation. The Thermovision system is a real time thermal imaging system for temperature measurement and analysis of both dynamic and static thermal patterns. The infrared detector is cryogenically cooled with liquid nitrogen. The scanner unit converts infrared radiation emitted by the object into an electrical video signal, which can be analysed by utilising a dedicated computer system. Computer Aided Thermographic Software (CATS) is used to perform the thermal analysis.

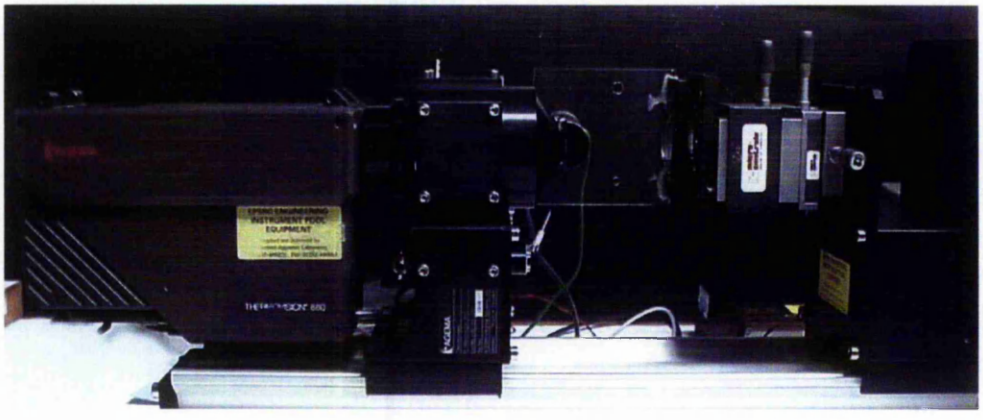


Figure 2.19 Shows a picture of the Infrared thermal imaging system. The system is fitted with microscope lens system to measure 1 mm diameter surface area.

EL arises from the non-thermal generation of light, however during the ACTFEL device operation, the current flow results in appreciable amount of heat[16]. Detail of the processes that generate heat within the device during operation will be discussed in Chapter 6. A picture of the measurement system is shown in Figure 2.19. A microscope attachment is used to image an active area of 1 mm diameter. A close up picture of the microscope is shown in Appendix B. In order to improve the emissivity of the surface, a black non-metallic paint was used to blacken the area under study.

2.5 Vacuum Chamber Characterisation and Ageing Unit

A vacuum chamber has been designed and built to perform lifetime measurements of ACTFEL devices. A LETFEL device has a cleaved emitting facet (phosphor without the protection of Y_2O_3 dielectric layer) exposed to the environment. On the application of high field, the facet has shown degradation after a few tenths of hours. It has been proposed that this degradation could be due to moisture in the air or hydrogen atoms in the environment diffusing into the phosphor resulting degradation. This phenomenon was investigated using this vacuum chamber.

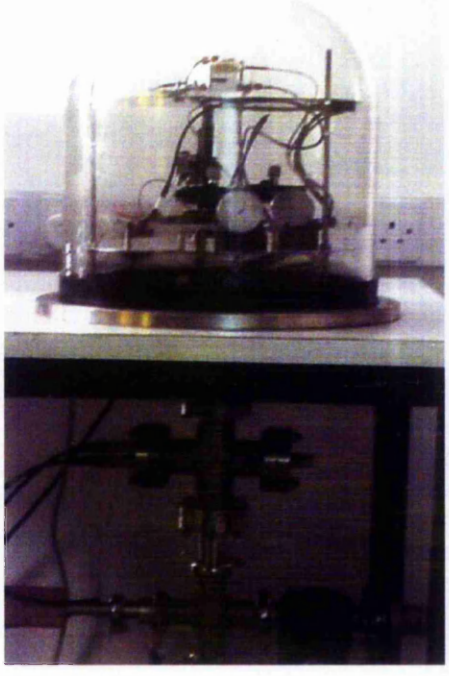


Figure 2.20 Picture of the vacuum chamber utilised to measure luminance degradation of ACTFEL device under vacuum.

The vacuum in the chamber is achieved with a rotary pump, which can pump the chamber pressure to less than 160×10^{-3} mbar. Chamber pressure is monitored using an Edwards Pirani gauge. Luminance from either edge emission or vertical out of an ACTFEL device is coupled via 1 mm fibre to light detectors. A picture of the system is shown in Figure 2.20. A picture of the fibre optic system for vertical out device is shown in Appendix B. The control PC mentioned in Section 2.4.1 monitors the measurements.

2.6 Crystal Structure Characterisation

2.6.1 LASER Raman Spectroscopy

This measurement was performed at the University of Greenwich on NTU thin film samples. The measurement details are as follow:

Raman Spectroscopy was performed using a Labram Raman 1E spectrometer, equipped with an 1800 grooves/mm holographic grating and a Peltier-cooled CCD detector. The spectrometer is configured with an Olympus BX40 microscope, which has good confocality, thereby permitting the examination of thin film thicknesses of the order of micrometers. In addition, an Olympus x100 magnification objective was used. This objective has a high numerical aperture (N.A. 0.95), which is necessary in order to achieve a good axial spatial resolution. The samples were excited with 514.5 nm light from an argon ion laser, which provided 10 mW of power at the sample surface.

2.6.2 X-Ray Diffraction

X-ray diffraction (XRD) measurement was used to investigate the crystallinity of the thin films, utilising a Philips PW 1049/10 XRD system. The system has a standard CuKα emission wavelength, λ of 0.154056 nm. The applied power and angular steps are 40KV x 25mA and 0.01° respectively. XRD measurements were performed at angles 10 to 71°. The observed peaks were used to study the spacing between crystal planes, improvement in crystallinity and the crystallite size. The plane spacing d was calculated using the Bragg equation[17]

$$\lambda = 2d \sin\theta \qquad \text{Eq. 2.9}$$

where θ is half of the XRD measured diffraction angle.

It is also possible to calculate d if the lattice constant, of a particular structure relating to Miller indices, hkl and lattice constant (a) are known[17]. Both Y_2O_3 and ZnS:Mn have cubic structures.

Plane spacing, d for cubic structure could be calculated with the equation below

$$\frac{1}{(d_{hkl})^2} = \frac{h^2 + k^2 + l^2}{a^2} \qquad \text{Eq. 2.10}$$

Broadening of a diffraction line is an indication of polycrystalline materials, especially more pronounced for materials with individual crystals being less than 100nm. Full width angle taken at half the maximum (FWHM) of the diffraction peak is utilised to approximate the average crystallite size[18]. Crystallite size, t could be calculated from the Eq. 2.11, below

$$B = \frac{0.9\,\lambda}{t\cos\theta} \qquad \text{Eq. 2.11}$$

where B is the broadening of diffraction line at half it maximum intensity in radians and t being the diameter of the crystallite size. The peak intensity together with FWHM gives a picture of the crystalline quality of the material.

2.7 References

1 M. R. Craven, Ph.D. Thesis, Nottingham Trent University, U.K. 2000

2 W.M. Cranton, D. M. Spink, R. Stevens and C. B. Thomas, Thin Solid Films 226 1992 Pg. 159

3 Y. Nakanishi, S. Mori, T. Nakamura, H. Tatsuoka, H. Kuwabara & Y. Hatanaka, Mat. Chem. & Phys., 43 1996 Pg. 292

4 A.N. Krasnov, Thin Solid Films 347 1999 Pg. 1

5 R.A. Serway, Physics for Sciencetist and Engineers with Modern Physics, 5th ED, Sunder College Publishing, 2000 Pg. 1198

6 D.H. Smith, Journal of Luminescence 23, 1981. Pg.209

7 A.N. Krasnov & P.G. Hofstra, Progress in Crystal Growth Characterization of Materials, 2001 Pg. 65

8 P.J. Harrop, Dielectrics, Butterworth Publishers, 4, 1972

9 J.J. O'Dwyer, The Theory of Electrical Conduction and Breakdown in Solid Dielectrics, Clarendon Press, 1973

10 R. Stevens, C.B. Thomas & W.M. Cranton, IEEE Elec. Dev. Lett. 15 (3) 1994, Pg. 97

11 C.B. Thomas, W.M. Cranton, I.P. Mc Clean, M.R. Craven & A.H. Abdullah SID Int. Symp. 1995 Pg. 887

12 R. Stevens, C.B. Thomas & W.M. Cranton, Appl. Phy. Lett. 63 1993 Pg. 3119

13 Y.A. Ono, World Scientific Publishing Co. Pte. Ltd. 1995

14 R.C. Ropp, Luminescence and the Solid State, Elsevier 1991

15 W.M. Cranton, Ph.D. thesis, University of Bradford 1995.

16 A.N. Krasnov, Thin Solid Film (Review article), 347, 1999 Pg. 1

17 D.B. Cullity, Elements of x-ray diffraction, Addison-Wesley, Reading, MA, 2nd Ed, 86 1978

18 C. Hammond, The basics of crystallography & diffraction, Oxford Science Publications, 146 1997

CHAPTER 3

PROPERTIES OF Y_2O_3 THIN FILM

3.1 Introduction

Yttrium Oxide (Y_2O_3) (also known as *Yttria*) was initially proposed in 1974 as the dielectric of choice for use in ACTFEL devices by Sharp[1], one of the major Electroluminescent Flat Panel display manufacturers of the 80's and 90's. This is due to its classification as a high-κ material for its high value of dielectric constant, Charge Storage Capacity (CSC) and low leakage current. However, Y_2O_3 has poor reproducibility and was recently superseded by silicon-based dielectrics, e.g. SiON. Even so Y_2O_3 is still used in many research laboratories because of its merits and is of interest for commercial applications such as Integrated Circuits[2,3,4,5]. Hence there is a need for more detailed studies to be carried out to improve the quality and growth of this transition-metal oxide. Therefore this chapter deals with thin film Y_2O_3 dielectric properties as a function of thickness, growth and processing parameters. A comparative study was carried out to appreciate how this insulator contributed to the characteristics of the ACTFEL device in relation to SiON based insulator device, which is presented in chapter 6. (Y_2O_3 constants for pure crystal are given in Appendix C)

3.2 Growth Parameters

Y_2O_3 was deposited using the system described in Section 2.2. The thin film Y_2O_3 grown by this method has a measured refractive index n of 1.91, which is in good agreement with the reported pure crystal refractive index of 1.93[6]. Using Eq. 2.1, it can be shown that each cycle on the thickness monitor represents a growth of approximately 170nm thick of Y_2O_3 thin film. Therefore, with certain tolerance the number of cycles on the thickness monitor can be used to obtain a measure of target surface sputtered. Utilising this measure, films grown at various stages of the target lifetime were characterised, as shown in Figure 3.1. It was found that at the early stages of the target's life, the thin films had a lower relative dielectric constant, ε_r (calculated using Eq. 2.4). This stage is described as the "Pre-Stable" region, which is consistent with changes in the crystalline structure shown in Figure 3.1.

Y_2O_3 in powder form has three main diffraction peaks, corresponding to the (222), (400) and (440) planes, located at angles of 29.52°, 33.78° and 48.53° respectively[7], characteristic of its cubic nature. However, in most samples sputtered on Si, only the XRD peak corresponding to the (222) plane showed significant intensity, hence it becomes the focus of this study. Analysing the peak corresponding to (222) plane, films grown during the Pre-Stable period were of low crystalline quality. This is apparent from the XRD peak intensity and plane spacing (d-space), shown in Figure 3.1. Also the crystallite size indicates an increase from 15nm during the Pre-Stable to 20nm after this region for samples annealed at 500 °C (calculated using Eq. 2.11).

The edge of this region accounts for almost a third of the target sputtering life. The films produced after the Pre-Stable region increase in dielectric constant until stabilisation is reached referred to as the "Stable" region. In this region it was identified that Y_2O_3 thin films were of more reproducible quality.

This phenomenon is believed to be due to the difference in sputtering yield of Yttrium (Y) and Oxygen (O) atoms during the course of the target's lifetime. On the basis of Sigmund's expression, the sputtering yield is proportional to the Energy transfer function between the sputtering ion and the target atom[8]. It can be shown that the Energy Transfer in Binary Collision for Y and O with Argon ion are almost the same. However O being a lighter atom would be preferentially ejected in the direction normal to target surface relative to heavier Y atoms[9]. This would cause a depletion of O atoms from the surface. This is consistent with observation of a black layer existing on the surface of a used target, which is believed to be Y rich, as shown in Figure 3.2

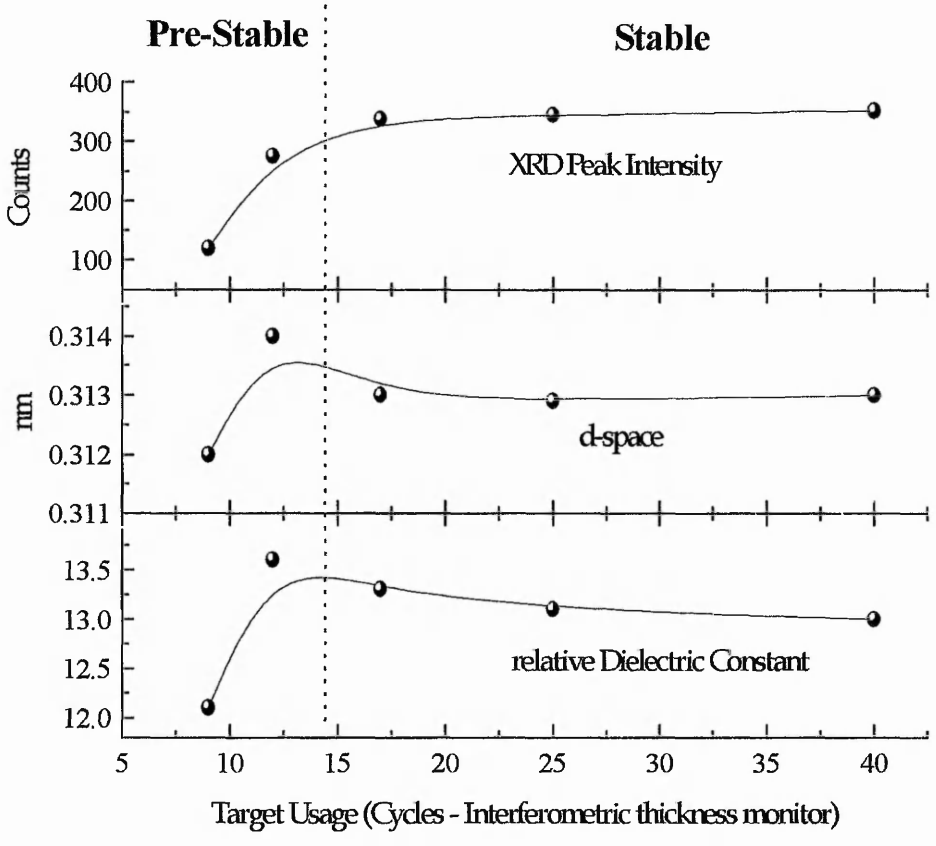


Figure 3.1 Shows XRD structural analysis and relative dielectric constant of thin film Y_2O_3 as a function of target usage lifetime. It indicates the Pre-Stable region in the course of the thin film grown during a target lifetime. Each cycle on the thickness monitor represents 170 nm of Y_2O_3 grown on the substrate wafer. The samples were of standard 300 nm thick.

This is a plausible explanation for the poorer quality of the thin films fabricated during the Pre-Stable period. After this phase, the effect of sputtering yield difference between Y and O will take place. Therefore due to the difference in depletion rate from the target surface and the difference in surface concentration of the two species, the sputtering yield will eventually balance out between these two types of atoms and form a better stoichiometrical structure. This region is believed to be the Stable period according to the quality of the thin film produced. The growth rate over the sputtering lifetime of the target remained stable at 14 Å/min ±5%.

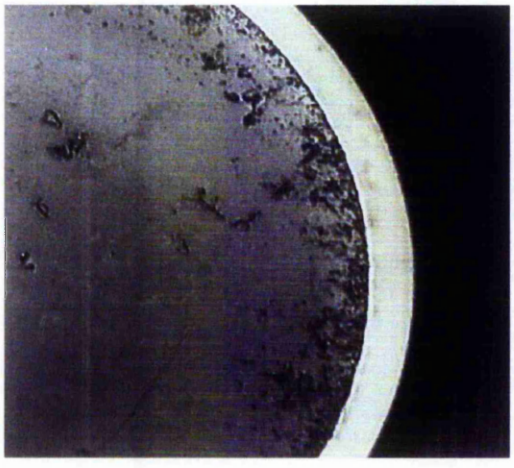


Figure 3.2 Picture of a used 7.5 cm Y_2O_3 target showing the surface of the active region to be blackened believed to be Yttrium rich.

The Y_2O_3 thin film samples were annealed for different time spans at 500 °C. The ε_r versus annealing period characteristic showed no change. However a minimum of one hour of annealing was required to reduce leakage current by an order of magnitude, from 6.5 x 10^{-9} for non-annealed sample to 7 x 10^{-10} A/cm^2. Annealing the sample for extended periods beyond one hour worsened the leakage current. On the basis of overall evaluation, one hour of annealing was used in all samples under study.

3.3 Structural and Dielectric Properties

The crystallinity of an annealed sample is greatly improved as indicated by measured XRD data as shown in Figure 3.3. The XRD data show a clear increase in plane (222) peak intensity and shift of the peak to a higher diffraction angle with annealing temperature. Analysis of the XRD is summarised in Figure 3.4.

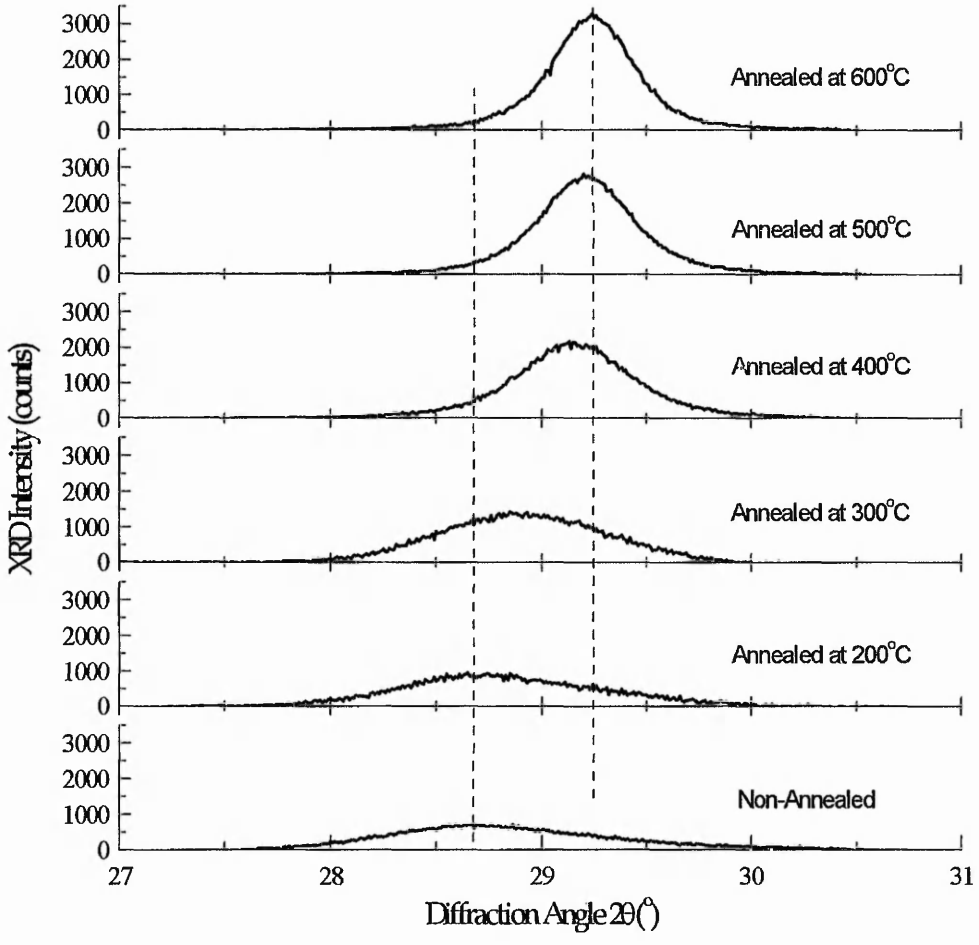


Figure 3.3 XRD pattern of 300nm thick Y_2O_3 thin films, showing the improvement in crystalline quality due to post-deposition annealing (222 peak shown). The thin films were grown at 190 °C.

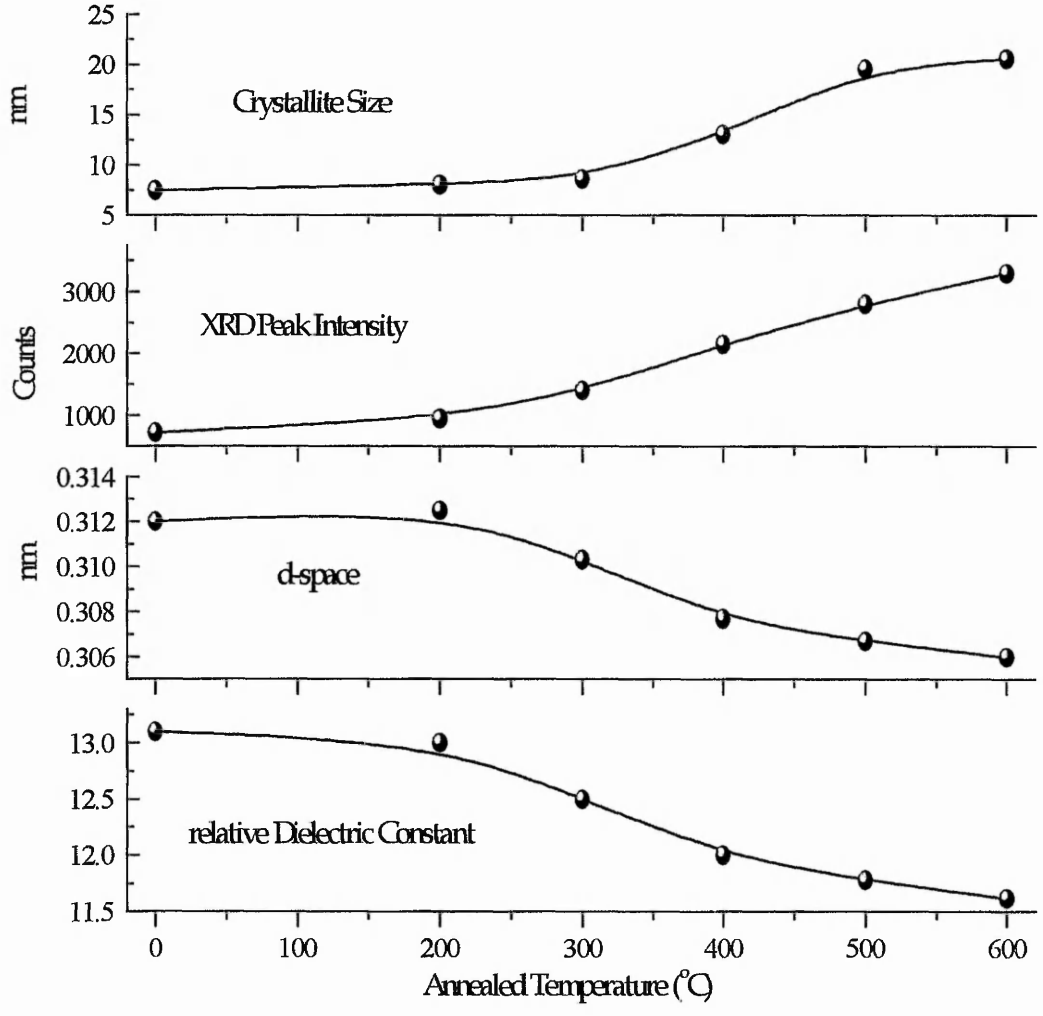


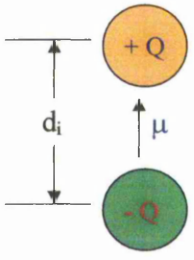
Figure 3.4 XRD structural analysis and relative dielectric constant for 300 nm thick Y_2O_3 films grown on silicon (100) as a function of sample annealing temperature. It demonstrates a large improvement in the crystallinity of 300nm thick thin film polycrystalline Y_2O_3 on Silicon (100) substrate with annealing temperature. Also illustrates the strong relationship between crystal d-spacing and ε_r.

The average measured d-space for non-annealed and annealed samples at 600 °C are 0.312 and 0.306 nm respectively. This suggests that annealing introduces a rearrangement within the Y_2O_3 crystallites, promoting crystal lattice structure, with d-spacing of 0.306 nm (calculated using Eq 2.10 considered for (222) plane from a unit cell length of 1.0604nm[10]). The peak intensity for this plane also increases with annealing

temperature. This is attributed to crystallites orientating themselves to reinstate order within the structure. Additionally the average crystallite size improved from 7nm for non-annealed samples to 21nm for samples annealed at 600 °C. In all considerations for the annealing temperatures studied, the samples showed more improvement in structural properties at heat treatment higher than 300 °C.

Coincidental with this observed structural transformation due to annealing, is a decrease in average ε_r from 13.0 to 11.6 ±0.2. Measurements indicate ε_r to be highly dependent on d-space. In Figure 3.4 the characteristics of ε_r and the measured d-space as a function of annealing temperature are also shown.

A hypothesis for this observation can be explained as:



Y_2O_3 has a body-centered cubic C-type structure with six oxygen ions surrounding each yttrium ion[11]. The d-spacing is the distance between planes of the crystal structure consisting of these molecular ions. Therefore these cation and anion, which behave as electric charges ±Q of opposite polarity, create dipoles, as shown in the figure on the left.

Changes in d-space would in turn vary the distance between these charges, d_i influencing the molecular dipole moment, μ when an electric field is applied. The dipole moment is given to be

$$\mu = Qd_i \qquad \text{Eq. 3.1}$$

The dielectric polarisation, P is equivalent to the average value of the electric dipole moment per unit volume[12], which carries a dimension as *charge per unit area*. In relation to P, the dielectric constant is defined as[13]

$$\varepsilon = \frac{\textbf{Charge per unit area}}{\textbf{Force per unit charge}} \qquad \text{Eq. 3.2}$$

Therefore it is proposed that small ε_r changes observed in the Y_2O_3 samples due to annealing in vacuum, is attributed mainly to the atomic rearrangement of the crystal structure, by encouraging reduction in the distance between planes and the improved ordering of the crystallites. This relationship is also demonstrated in a temperature independent experiment, shown in Figure 3.1.

This samples show only cubic characteristics determined from Raman spectrum measurement. Raman spectra were obtained for thin film Y_2O_3 samples on Silicon (100) substrate annealed at different temperatures. The samples investigated were annealed at 400, 500 and 600 °C and non-annealed. Even when focusing on the surface of the Y_2O_3 film, the Raman spectra from all four wafers show a very strong band at 520 cm^{-1}, which is the zero order phonon band of silicon. Additional bands at 302 and 960 cm^{-1} found were also due to silicon. The latter band is very broad and is the first order phonon band of silicon. On expanding the spectra in the 400 cm^{-1} region, a weak band is seen at 375 cm^{-1} in the spectra of the annealed samples but it is absent in the spectrum of the non-annealed. This band is the strongest Raman phonon band of cubic Y_2O_3[14,15,16]. Furthermore, it can be seen from Figure 3.5 that the 375 cm^{-1} band of cubic Y_2O_3 increases in intensity with annealing temperature over the range 0 – 600 °C, confirming the XRD measurement.

It is proposed that the increase in the crystal quality leads to a reduction in the density of bulk traps, associated with grain boundaries and interstitial defects of polycrystalline films. Assuming conductivity is primarily by hopping, this results in a longer hopping distance for electrons between traps, hence lowering the electron mobility. This was demonstrated as a reduction in the measured average leakage current from 2×10^{-11} A for non-annealed to 1×10^{-12} A for annealed samples of 300 nm thick, 1mm diameter diodes at 1MV/cm. IV curves for Y_2O_3 samples annealed at different temperature are shown in Figure 3.6.

Samples with different thickness were fabricated to investigate the polycrystalline film properties as a function of thickness. XRD analysis revealed that d-space did not vary

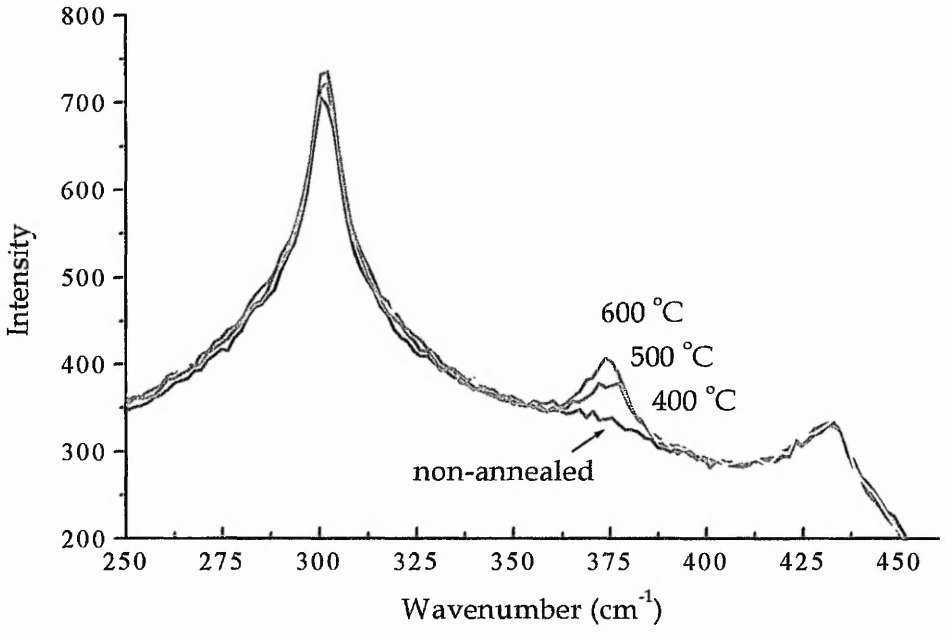


Figure 3.5 Raman Spectrum for Y_2O_3 thin films grown on Silicon (100) substrate, indicating an improvement in cubic nature of the crystallites with annealing temperature.

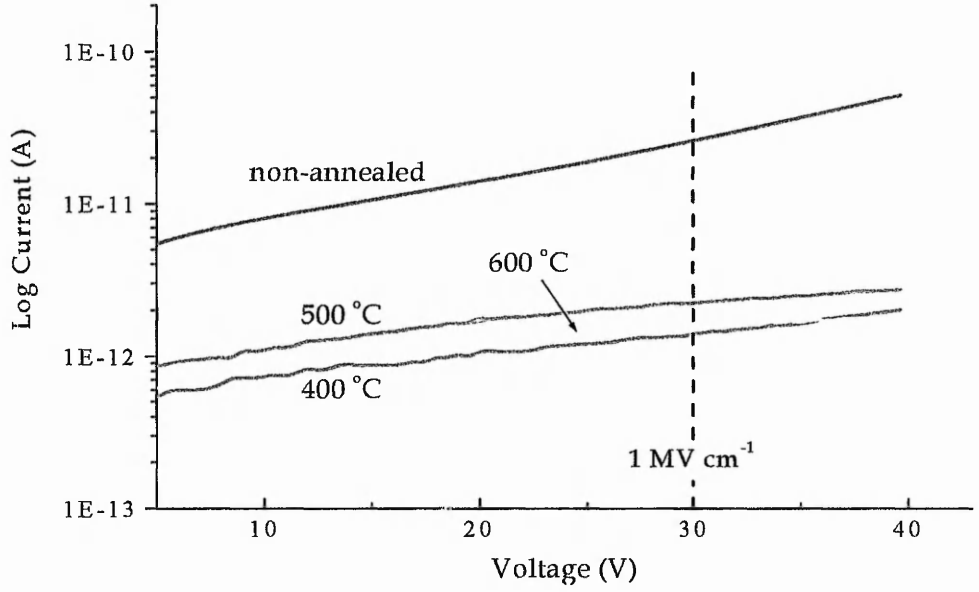


Figure 3.6 Current-Voltage curves for Y_2O_3 samples of 300nm thick, 1mm diameter diodes, indicating the improvement in leakage current after the samples have been annealed.

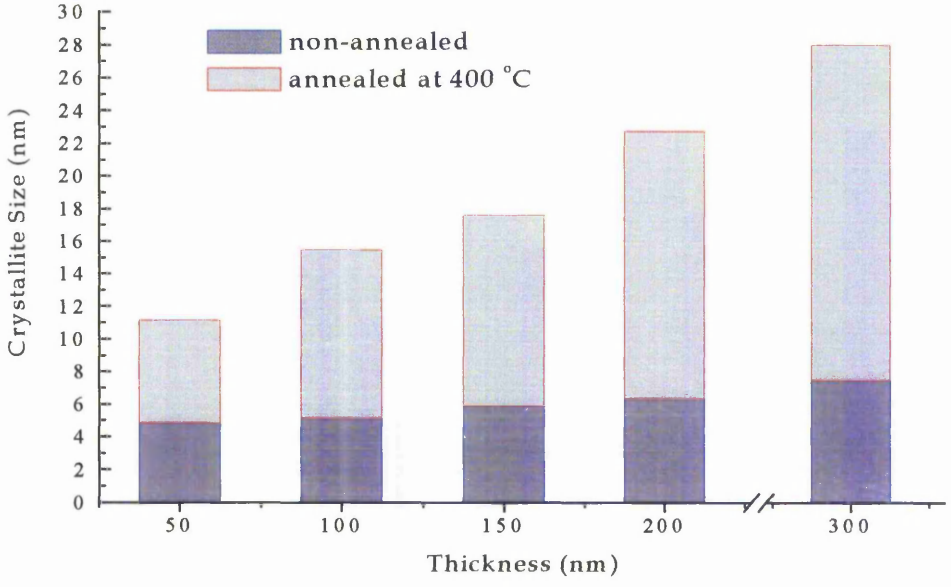


Figure 3.7 Shows the increase in crystallite size with increase in Y_2O_3 thin film thickness. Also indicated by these results is that, annealing does more improvement in thicker films.

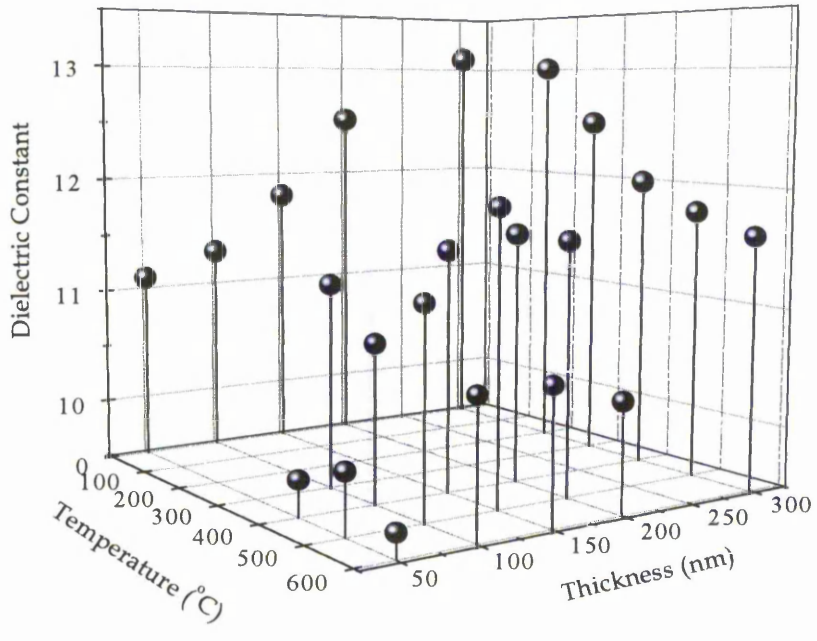


Figure 3.8 Summary of the average measured relative dielectric constant (± %5) for thin film Y_2O_3 as a function of sample thickness and annealing temperature.

with increasing thickness in both non-annealed and annealed samples. However the crystallites became larger as shown in Figure 3.7. In other words, the crystallinity of the material closer to the interface of the silicon is of lower quality and it improves as the thickness increases.

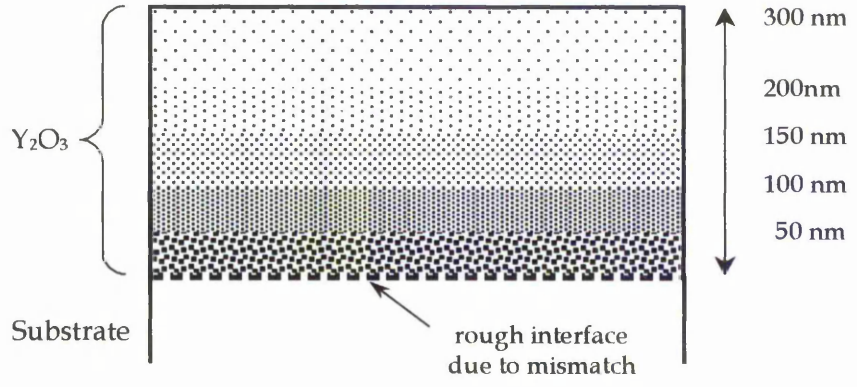


Figure 3.9 Pictorial crystalline defect thickness model of sputtered Y_2O_3 thin film on Silicon (100) substrate, showing the region closer to the interface is more defective.

Thin film Y_2O_3 has a measured lattice constant of approximately 1.06nm whereas Silicon is at 0.5431nm[17] and even at 2 multiples (1.0862nm) is not a perfect match. Hence the lattice mismatch between silicon and Y_2O_3 would cause the interface region to be disordered. However as the crystallites grow away from the interface they would preferentially arrange themselves to the natural crystal structure, to form larger crystallites. CV analysis discussed in Chapter 4 strengthens the hypothesis that the thin film material closer to the interface of the silicon contains a higher density of bulk traps, with the trap density improving as the thickness increases. This could explain the increase in ε_r with increasing sample thickness, as shown in Figure 3.8. It is believed that this increase arise from the reduction of isolated charges. The proposed model of the crystallite's microstructure for various thickness stages is shown in Figure 3.9. Annealing proved to be more effective in thicker films showing more improvement in crystal quality, as shown in Figure 3.7. This would be expected, because the crystallite would have more freedom to rearrange itself having lesser influence from the substrate.

3.4 Oxygen Annealing

Annealing thin film Y_2O_3 in an Oxygen (O_2), environment is thought to improve the dielectric properties[3,18,19,20,21]. However, a limited amount of free oxygen ions are believed to diffuse into the Si during annealing, contributing to the growth of an interfacial silicon-based oxide layer. In the samples studied, annealing was performed in high vacuum, hence this interfacial layer would not be expected. A good argument is given in reference [22] for the expectation, which says; during the annealing stage, thermodynamics dictate that due to its higher enthalpy of formation, Y_2O_3 will reduce interfacial SiO_x, filling oxygen vacancies in the epilayer. Recently, depth profiling done by *Busch et al.* in samples annealed in O_2 and vacuum revealed that this is the case[23].

The formation of the interfacial layer by oxygen annealing would reduce the overall effective capacitance and the calculated ε_r. However, to investigate the possible improvement that O_2 annealing could do for this oxide without the risk of this interfacial layer being formed, some 300nm thick samples were annealed in low-pressure oxygen ambience instead of in vacuum. The samples were annealed in 20mTorr of 20% oxygen to Argon concentration at 500 °C. A 5.6% increase was measured for the dielectric constant in comparison to the value obtained for annealing in vacuum. This small increase could be due to available oxygen in perfecting oxygen deficient sites that may exist in the bulk material. Therefore by annealing the Y_2O_3 samples in low pressure O_2 environment, the growth of the interfacial layer has been avoided or minimised to a negligible level. However no change in structural (XRD measurement) or breakdown strength is observed.

3.5 Electrical Stressing

Y_2O_3 MIS diodes were electrically stressed. CV measurements were performed before and after stressing. No change in dielectric constant was observed both for DC and AC stressing at electric field of 2MV/cm for up to 50 hours. However the MIS system showed some shifts in its CV behaviour, which will be discussed in the next chapter.

3.6 Breakdown Strength

More than 55% increase in breakdown strength was achieved by annealing the thin films at 400 °C. However, at higher annealing temperatures, the characteristics of dielectric breakdown field strength E_{bd} (calculated using Eq. 2.5) show a decreasing value as listed in Table 3.1. These values are on the higher band of the typical range seen for Y_2O_3 utilising different types of deposition techniques[7,24,25,26].

Breakdown Technique	Average Breakdown Strength (MV/cm)			
	Non-annealed	400°C	500°C	600°C
AC	5.6	6.5	6.3	6.0
DC	3.2	5.0	4.5	3.7

Table 3.1 Summary of the average breakdown strength (±10%) for thin film Y_2O_3 using AC and DC electrical breakdown technique for 300nm thick samples. The measurement is repeated on two wafers and each value is averaged from 12 diodes.

Overall electric field strength utilising the AC method showed a slightly higher strength than in comparison to using DC. Insulator figure-of-merit, CSC exhibit values over $5\mu C/cm^2$ (calculated using Eq. 2.6). Howard has shown that CSC at breakdown should be at least three times that of the active layer[27]. The CSC value for thin film ZnS:Mn is $1\mu C/cm^2$ (Chapter 5). Hence the measured values are well above the required use in ACTFEL device.

No significant variation in breakdown strength was found for sample thickness of 100nm and above, however the 50nm thick sample has a DC breakdown strength of 2.2MV/cm ±20% for non-annealed and 2.4MV/cm ±25% for annealed samples. The more defective initial layer could be the reason for this lower value.

3.7 Summary and Conclusions

Y_2O_3 thin film dielectric properties as a function of growth and processing parameters were investigated. It was found that at the early stages of the target's life, the thin films grown had a dielectric constant of lower value. Also, the thin film crystallinity produced during the early stages was of lower quality, which improves after the "Pre-Stable" period of the target usage lifetime. The reason for this is believed to be the sputtering yield difference of Y and O atoms at the target surface during the course of its lifetime.

Annealing significantly improved the crystallinity of the samples by introducing rearrangement within the Y_2O_3 crystallites, promoting the single crystal lattice structure and reinstating order within the structure. The average crystallite size increases with annealing temperature. In all considerations, the samples showed more pronounced improvement in structural properties at annealing treatment higher than 300 °C.

The dielectric constants of the thin films were found to be highly dependent on plane spacing of the crystallites, which showed a slight decrease at higher annealing temperature. This was explained as influence of dipoles being modified with changes in d-spacing of the most prominent (222) plane of its natural Cubic crystal phase. Raman measurement confirms improvement of this crystal phase with increase in annealing temperature.

Leakage current decreases by more than an order when the samples were annealed at 400 °C. This is due to the increase in the crystal quality, leading to a reduction in the density of bulk traps associated with grain boundaries and interstitial defects of polycrystalline films.

Annealing the thin film at 400 °C also improved the breakdown strength by more than 55%, however at higher annealing temperatures it worsened. Charge Storage Capacity exhibit values over $5\mu C/cm^2$, which are well above the required use in ACTFEL device. No significant variation in breakdown strength was found as a function of sample

thickness however the 50nm thick sample has less than half the strength of thicker samples. The more defective initial layer is believed to be the reason for this lower value.

Annealing in low pressure 20% O_2 environment at 500 °C improved the dielectric constant by 5.6% in comparison to samples annealed in vacuum. It has been demonstrated that annealing the Y_2O_3 samples in low pressure O_2 environment, the growth of the silicon based oxide interfacial layer was avoided or minimised to a negligible level. However this type of treatment showed no change in structural or breakdown strength.

Crystallite size increases with sample thickness. This improved the dielectric constant of the material, which is believed to be by reduction of isolated charges within the thin film structure. It has been demonstrated that the lattice mismatch between silicon and Y_2O_3 produces smaller crystallite closer to the interface. Consequently, annealing proved to be more effective in thicker films showing more improvement in crystal quality.

No change in dielectric constant was observed for both dc and ac stressing at electric field of 2MV/cm for up to 50 hours.

3.8 References

1 T.Inoguchi, M.Takeda, Y.Kakihara, Y.Nakata and M.Yoshida, Proc. of SID digest 1974 Pg. 84

2 L. Manchanda, M. Gurvitch, IEEE Electron Device Lett. 9, 4 1988 Pg. 180

3 A.C. Rastogi & R.N. Sharma, Semicond. Sci. Tech. 16 2001 Pg. 641

4 L.S. Yip, I. Shih, Electronics Lett. 24, 20 1988 Pg. 1287

5 G.D. Wilk, R.M. Wallace & J.M. Anthony, Jour. of Appl. Phys. (Review), 89/10 2001 Pg. 5243

6 Y. Nigara, Japanese J. Appl. Phys., 7 1968 Pg. 404

7 K. Onisawa, M. Fuyama, K. Tamura, K. Taguchi, T. Nakayama, Y.A. Ono, J. Appl. Phys. 68,2 1990 Pg. 719

8 B. Chapman, Glow Discharge Processes, A Wiley-Interscience Publication 180, 1980

9 S.I. Shah, Handbook of Thin Film Process Technology, IOP Publishing A3.0:10, 1995

10 B.H.O'Connor & T.M. Valentine, Acta Cryst. B25 1969 Pg. 2140

11 W.J. Troff and M.E. Thomas, Handbook of optical constant of solids II, Academic Press 1991 Pg. 1079

12 C.Kittel, Introduction to Solid State Physics, 5th Ed, Wiley, 1976, Pg. 401

13 A.V. Hipple, Dielectric Materials and Applications, Artech House, 6 1995

14 J. Silver, M.I.Martinez-Rubio, T.G.Ireland, G. R. Fern and R. Withnall, *J. Phys. Chem B*, 105 2001 Pg. 948

15 J.C. Panitz, J.C. Mayor, B.Grob & W. Durisch, Journal of Alloys and Compounds 303 2000 Pg. 340

16 R.B. Hunt, Jr. and R.G. Pappalardo, J. Luminescence, 34 1985 Pg. 133

17 B.D. Cullity, Elements of X-Ray Diffraction 2nd Ed, Addison Wesley Pg. 507

18 R.N. Sharma, S.T. Lakshmikumar and A.C. Rastogi, Thin Solid Films 199, 1991 Pg. 1

19 R.H. Horng, D.S. Wuu, J.W. Yu, C.Y. Kung, Thin Solid Films, 289 1996 Pg. 234

20 M.E. Hunter, M.J. Reed, N.A. El-Masry, J.C. Roberts and S.M. Bedair, Applied Phys. Letters 1935 2000

21 S.K. Kang, D.H. Ko, E.H. Kim, M.H. Cho and C.N. Whang, Thin Solid Films Letter, 353 1999 Pg. 8

22 A. Dimoulas, G. Vellianitis, A. Travlos, V. Ioannou & A.G. Nassiopoulou, J. Appl. Phys., 92/1 2002 Pg. 426

23 B.W.Busch, O. Pluchery, Y.J. Chabal, D.A. Muller, R.L. Opila, J.R. Kwo & E. Garfunkel, MRS Bulletin, March 2002 Pg. 206

24 V.A. Rozhzov, V.P. Goncharov & A.Y. Trusova, IEEE 5th Int. Conf. On Conduction and Breakdown in Solid Dielectrics 1995 Pg. 552

25 C.H. Ling, J. Bhaskaran & W.K.Choi, Vacuum 43 5 1992 Pg. 753

26 T.S. Kalkur, R.Y. Kwor & C.A. Paz De Araujo, Thin Solid Films 170 1989 Pg. 185

27 W.E Howard, IEEE Trans. on Electron Devices 1977 Pg. 903

CHAPTER 4

CAPACITANCE ANALYSIS OF Y_2O_3 MIS DIODE

4.1 Introduction

Capacitance-Voltage (CV) measurements were carried out on sputtered thin film Y_2O_3 MIS diodes. As much as the study of MIS diodes is useful in understanding the semiconductor surface, it can also reveal valuable information regarding the nature of the insulator. The techniques used in this study were developed in the past for the characterisation of Si-SiO_2, Metal Oxide Semiconductor (MOS) diodes and they were also utilised in MOSFETs analysis. Terman first employed this diode structure in the study of a thermally oxidized silicon surface[1]. The fundamental theory of this structure was developed during decades of research, and the interested reader can find an extensive analysis of the MIS diodes in references [2] and [3]. The theory is mainly based on the Fermi-Dirac and the S-H-R (Shockley-Hall-Read) statistics that characterise the statistics of trapping and de-trapping of interface and bulk states, and would be applicable for any insulating oxide material, grown on a semiconductor substrate. Here, some of the concepts have been used to characterise the integrity of Y_2O_3 thin film, which is of much importance in the optimised fabrication of this high-κ, material.

4.2 General MIS CV Measurement Theory

A typical Metal Insulator Semiconductor (MIS) structure is shown in Figure 4.1. The steady state capacitance of the diode as a function of gate bias is measured using a two-component voltage waveform. It consists of a small-signal Alternating Current (AC) voltage referred to as the probe signal, superimposed on a Direct Current (DC) bias.

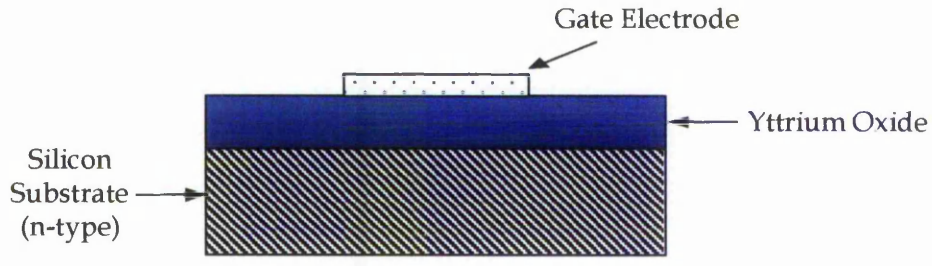


Figure 4.1 Cross section of Y_2O_3 MIS diode.

Utilising this method, the capacitance of the diode can be determined as a function of DC bias. The total capacitance of the diode consists of two capacitances connected in series, which are the insulator layer capacitance, Cins and semiconductor surface region, Cs. This is shown schematically in Figure 4.2.

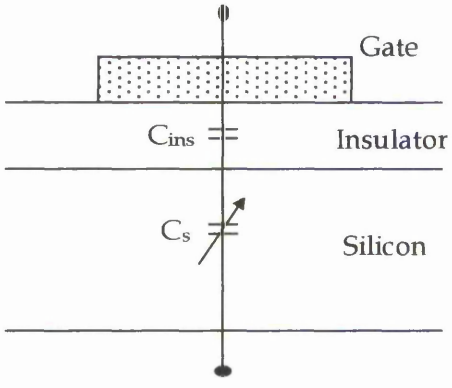


Figure 4.2 Schematic of an MIS diode shown as a simple equivalent circuit.

In Figure 4.2, the capacitor Cs is shown as a variable to denote that it is bias dependent.

The measured capacitance, C_m is related to these components as given in Eq. 4.1

$$C_m = \frac{C_{ins}\, C_s}{C_{ins} + C_s} \qquad \text{Eq. 4.1}$$

A potential-band diagram of such structure, in the ideal case, is shown in Figure 4.3. The ideal case is based on the following assumptions:

- At zero applied bias, the work function difference (ϕ_{ms}), between the metal (ϕ_m), and the semiconductor (ϕ_s), is zero.
- The only charges that exist in the structure under any biasing condition are those in the semiconductor. Therefore the gate voltage (V_G), would be equal to the flatband voltage (V_{FB}), while the bands in the semiconductor and in the oxide are flat. This means no oxide or interface charges exist to offset the system.

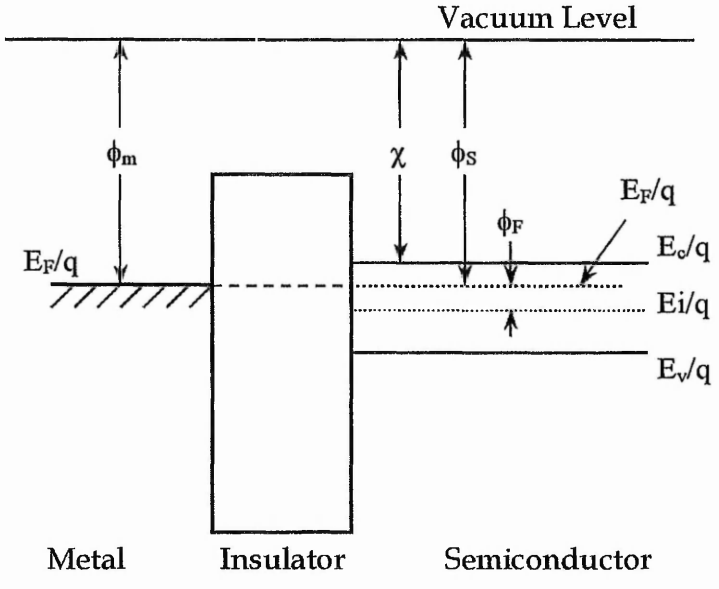


Figure 4.3 Potential band diagram of a MIS structure with an n-type semiconductor at flatband. ϕ_F is the potential difference between the Fermi level, E_F/q and intrinsic Fermi level, E_i/q. χ is the electron affinity of the semiconductor.

Hence the applied V_G, is partially dropped across the insulator and partially across the semiconductor surface, as given by Eq 4.2.

$$V_G = V_{FB} + V_{ins} + \psi_S \qquad \text{Eq. 4.2}$$

where V_{FB} is the flatband voltage which is defined as the offset voltage when $V_G = 0$. While in the ideal case $V_{FB} = 0$ in practice $V_{FB} \neq 0$ due to presence of bulk charges and interface state charges. V_{ins} is the voltage drop across the insulator and ψ_S is the semiconductor surface potential.

During the CV measurement when the diode is biased with positive or negative voltages, the semiconductor surface capacitance varies. The band bending of the semiconductor surface reflects these variations as shown in Figure 4.4. The three regions shown in the ideal case can also be pointed out on a measured CV curve of a typical MIS structure as in Figure 2.9. These regions are named accumulation, depletion and inversion. The measurements in this study were performed using medium-high frequency (1 MHz) probe signal, on n-type silicon.

When a positive voltage is applied to the metal gate, the system goes into the accumulation region. The measured capacitance is due to the dominating Cins, as Cs would be very small. This is simply because the positive gate bias would attract electrons to the interface, causing an accumulation of majority carriers at the silicon surface. This would bend the conduction band downwards, closer to the Fermi level, as is shown in Figure 4.4a. The large electron density at the silicon surface will contribute to a very large capacitance that is Cs >> Cins. Utilising equation Eq. 4.1, the much smaller Cins would dominate, hence measured capacitance, C = Cins.

When a small negative bias is applied to the gate, the system will go into depletion. The bias would cause a layer near the silicon surface to be depleted of majority carriers and thus the immobile, positively charged donor ions would dominate. The semiconductor band would bend upwards as shown in Figure 4.4b. The depletion layer width

increases, as the gate is made more positive, making the depletion capacitance, Cd smaller. The depletion layer in series with the insulator layer reduces the total capacitance.

When a larger negative bias is applied to the gate, the diode goes into inversion. The band bends upward even more to the extent that the intrinsic Fermi level crosses over the Fermi level as shown in Figure 4.4c. At this point the minority carrier density would be bigger than the majority carrier density, screening the depletion layer at the interface. At the measuring frequency, minority carriers in the silicon would not be able to respond to the fast variation of the probe signal. Generally, all minority carriers only respond to frequencies well below 1 kHz in device-graded silicon[2,4]. At high frequency in effect the carrier-inverted layer has no response to the AC signal, and contribute no charge to this effect apart from the spatial redistribution effect[5,†]. Therefore the measured capacitance varies continuously and reaches a minimum value, C_{inv} that is determined by the series capacitance of the maximum depletion layer capacitance and the insulator capacitance.

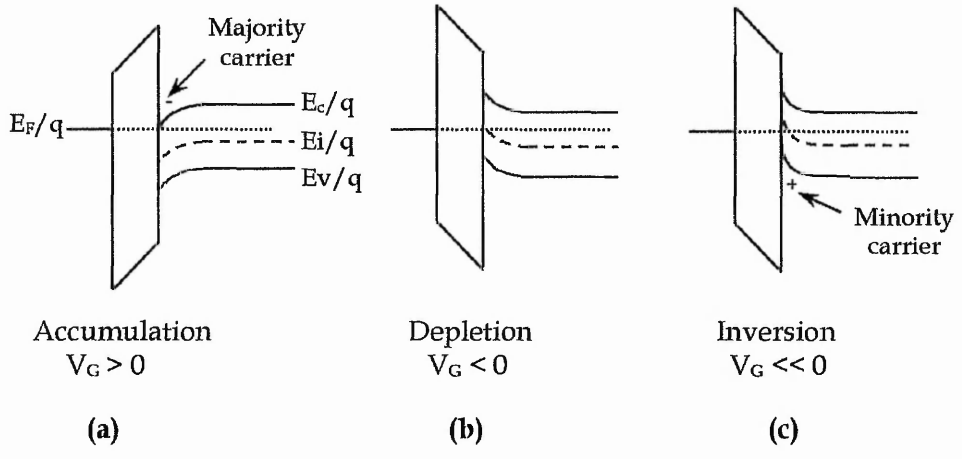


Figure 4.4 Illustrates the operation of a MIS system, showing the band bending at the three regions described in text in the ideal case and when n-type semiconductor is used.

† *In accumulation and depletion, minority carrier response to the AC gate voltage is unimportant because minority carrier density is negligible compared to majority carrier density at the silicon surface*

4.3 Flatband Voltage Determination

In the CV curve of an ideal MIS diode, V_{FB} is zero. However this voltage point could be shifted with the introduction of work function difference, ϕ_{ms} and various types of insulator charges[6], which exist in practice. The introduction of charge into the system induces an image charge on the silicon surface. Therefore a gate bias would be required to compensate the image charge produced to create a flatband condition at a non zero applied gate bias. One way of measuring the density of charge is to infer it from the voltage shift of a CV curve from its theoretical position. A reliable experimental method to obtain V_{FB} is given in reference [7], and is discussed briefly below. By converting a CV curve to $1/(C/C_{ins})^2$ versus V_G, a curve such as shown in Figure 4.5 would be obtained. The lower knee of this curve occurs at $V_G = V_{FB}$.

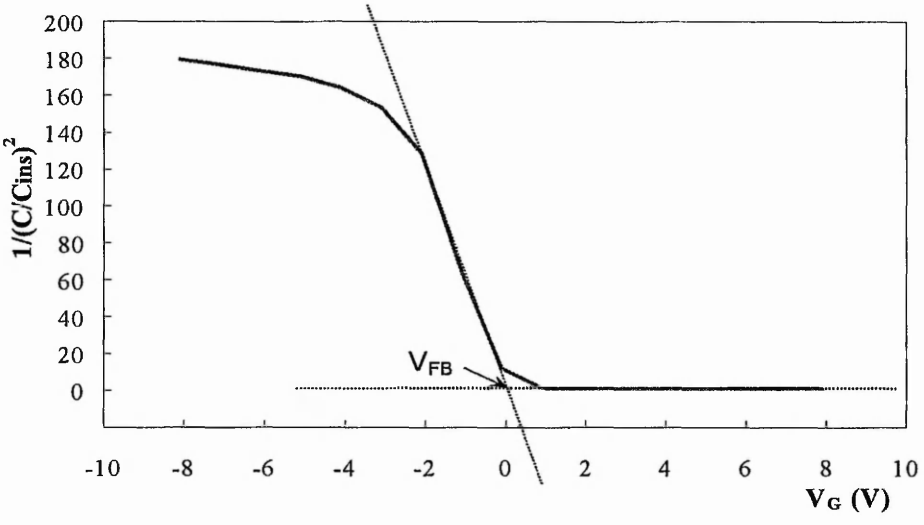


Figure 4.5 Diagram illustrating $1/(C/C_{ins})^2$ as a function of gate voltage. This curve corresponds to the data in Figure 2.9, with a slight shift in voltage scale in order to coincide V_{FB} to be zero.

In addition to this method, the V_{FB} values obtained are compared with the value calculated for flatband voltage capacitance (C_{FB}). The theoretical C_{FB} value would help ensure that the working region is correct. To facilitate the calculation of C_{FB}, Eq. 4.11 is employed which will be discussed in Section 4.5.

4.4 Charges in a Non-Ideal MIS System

There are various types of charges that may exist in an oxide-semiconductor system. Utilising the standardised oxide charge terminology used by Deal[8] the four main types are; fixed oxide charge (Q_f), mobile charge (Q_m), oxide trapped charge (Q_{ot}), and interface trapped charge (Q_{it}). A cross section of a MIS structure, with the various charges and their possible location is shown in Figure 4.6.

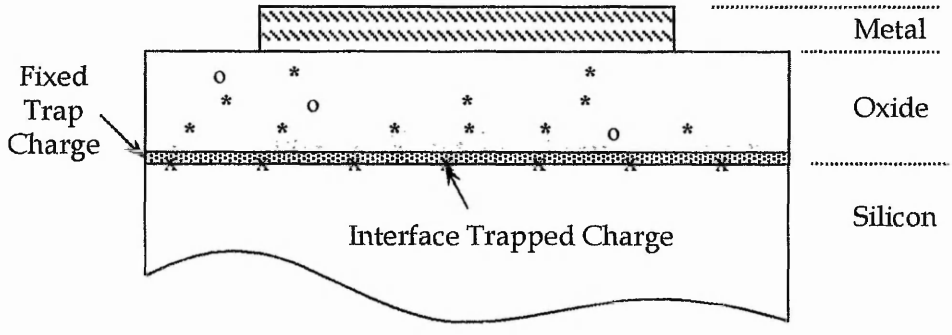


Figure 4.6 Illustration of a MIS structure with charges and their possible locations, generalised for oxides. " * " being oxide charge, "o" for mobile charge and "x" indicates interface trapped charge.

Interface state charges, (Q_{it}) are either positive or negative charges created due to structural defects at the interface. These defects are created because of lattice mismatch that may exist at the interface between the oxide and silicon, metal impurities or due to some bond breaking processes. Traps associated with these charges exist mainly in 2-dimensions at the interface of silicon and insulator. However in some occasions they can be distributed in a thin interface layer of 10nm in thickness. Interface traps can be charged or discharged, depending on the surface potential. Charges related to interface trap states would cause stretch-out in the depletion region of a CV curve[2].

Oxide Charges are associated with traps located in the bulk of the oxide insulator. The family of these oxide charges can be divided into three types, which are

- **Oxide Fixed Charge, (Q_f)** mainly existing near the interface of the silicon and are related to structural defects or remnants after interface trap charge is annealed out. It is regarded as a charge sheet, therefore causing a parallel shift of the CV curve along the voltage axis, thus fixing V_{FB} permanently at a different point than the theoretical position.

- **Oxide Trap Charges, (Q_{ot})** may be positive or negative due to holes or electrons, trapped in the bulk of the oxide. They are usually located either at the metal-oxide or oxide-silicon interface. The traps associated with this type of charge are bulk defects that are created during the fabrication process and affect the quality of the material. Electrons injected from the metal or silicon interface at high enough potential can be trapped in the bulk of the insulator, if they acquire enough energy to (overcome) the potential barrier at the interface, otherwise trapping and de-trapping can occur at the vicinity of the interface. In the second case the electrons at the silicon or Al electrode can communicate with the traps in the insulator by tunneling. Unlike fixed charge, oxide trapped charge is general annealed out by low temperature (< 500 °C) treatment, although neutral traps may remain[8]. In this study, it has been observed that not all the charges are de-trapped when the polarity is reversed in some samples. This observation will be discussed in the next section. The occurrence of injected oxide charge can be observed as hysteresis in CV curve. This can be identified while sweeping from accumulation to inversion, the curve would not vary its position, while the back sweep curve from inversion to accumulation would be transposed to more negative voltages. In this situation V_{FB} will be reduced. As the amount of charge injection and trapping would influence Q_{ot}, hysteresis would be dependent on the upper and lower limits of the CV measurement voltage scale.

- **Mobile Ionic Charge, (Q_m)** is commonly attributed to the presence of ionised Alkali metal atoms, which carry a positive charge. The presence of mobile ions causes hysteresis to occur in the CV curves. Hysteresis due to mobile ions is more pronounced at higher temperatures due to the increased mobility of metal ions. The hysteresis is due to the drifting of mobile ions on the application of positive or negative bias by altering the centroid of the mobile ion distribution. If a negative stress voltage is applied, the positively charged ions will move closer to the gate electrode, resulting in a reduction of the negative image charge on the silicon surface. Hence the CV curve will be shifted towards more positive voltages (to the right) creating clockwise hysteresis behaviour.

With the introduction of these charges to the MIS system, the relative position of V_{FB} would be influenced. Generating a relationship between all the factors that may influence V_{FB} would facilitate appreciation of the density of these charges. Considering all the above-mentioned parameters, the flatband voltage is influenced by the metal-semiconductor work function difference, ϕ_{mS} and the various charges[9] as given below

$$V_{FB} = \phi_{mS} - \frac{Q_f}{C_{ins}} - \frac{\gamma Q_m}{C_{ins}} - \frac{\gamma Q_{ot}}{C_{ins}} - \frac{Q_{it}(\psi_S)}{C_{ins}} \qquad \text{Eq. 4.3}$$

Q_{it} is designated as a function of ψ_S because the occupancy of the interface trapped charge depends on the surface potential. γ is a factor introduced to account for the charge distribution throughout the insulator, and defined as

$$\gamma = \frac{\int_0^d (x/d)\ \rho(x)\ dx}{\int_0^d \rho(x)\ dx} \qquad \text{Eq. 4.4}$$

where $\rho(x)$ is the charge per unit volume, d is oxide thickness and x is the position from the gate. This would mean $x = 0$ and $\gamma = 0$ if the charge is located at the oxide gate interface and $x = 1$ and $\gamma = 1$ at the silicon interface. However if an assumption is made

that $\rho(x)$ is constant for a range of thickness, γ would simply become d. With this factor, charge closest to the silicon surface would have the most effect on V_{FB}.

As discussed previously, in a MIS system oxide charges may be introduced by injection of electrons and / or holes either from the substrate or the gate area. The V_{FB} point would shift from its original position when this occurs. Such change in V_{FB} could be determined by the technique described in Section 4.3. Having measured ΔV (the relative shift), the amount of transferred charge may be determined by using the expression

$$Q = - \Delta V \, C_{ins} \qquad \text{Eq. 4.5}$$

However, as mobile ions can also cause CV hysteresis, their involvement must be first ruled out by examining the relative movement of the CV shift (i.e. clockwise or anticlockwise).

4.5 Yttrium Oxide MIS Diode

CV measurements were performed on Yttrium Oxide (Y_2O_3) MIS diodes. Samples were fabricated with different thicknesses in identical conditions thus maintaining the same growth environment. The samples were then annealed in vacuum as described in Chapter 2 between 300 and 600 °C. The Silicon substrates used were from the same batch of n-type with a doping density, N_d of $1x10^{14}$ cm^{-3} of Phosphorus. The measurement AC probe signal frequency and peak-to-peak amplitude are 1 MHz and 5mV respectively.

As discussed in Chapter 3, a non-annealed sample has more defects in its crystal structure. These defects are believed to create traps within the forbidden bandgap of this oxide, which can carry charge. Their existence was observed in the CV curve as it was always shifted from its theoretical position. One of the observations was in non-annealed, virgin 50 and 100 nm thick samples after the diodes were electrically stressed with positive bias.

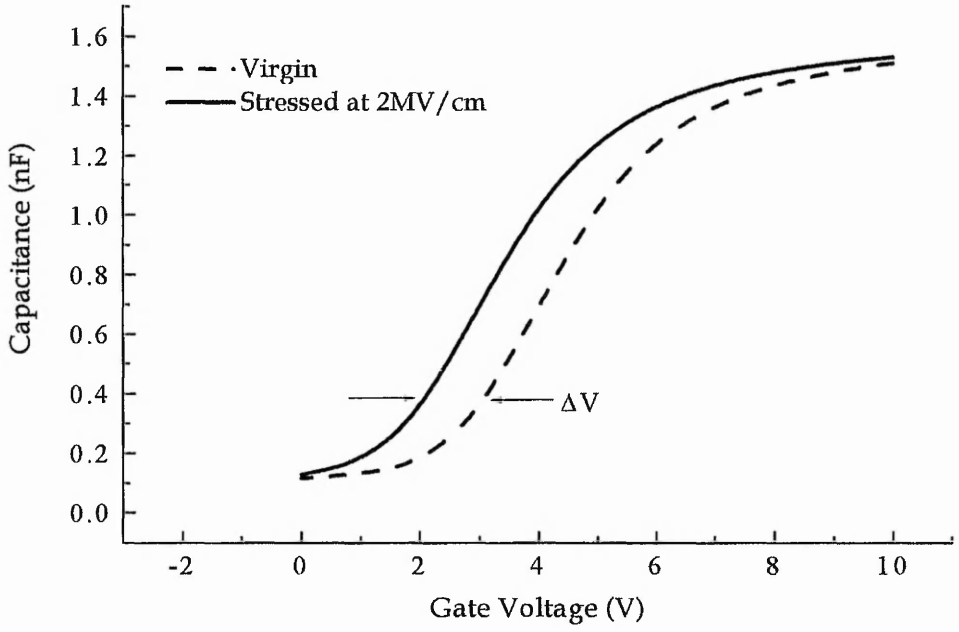


Figure 4.7 Shows the shift in CV curve toward less positive V_G after the application of positive gate voltage. The curves shown above correspond to non-annealed 50nm thick Y_2O_3 sample of 1mm diameter diode.

The V_{FB} shift, which occurred in non-annealed virgin diodes for the first sweep from accumulation to inversion, was permanent, and should not be mistaken for hysteresis. This trapped oxide charge did not get de-trapped when the polarity was reversed. In Figure 4.7, ΔV is 1.1 V and this is caused by stressing at positive 2MV/cm field. The shift was towards a less positive gate bias. Therefore this would mean that in the bulk of the insulator a less negative charge or more positive charge has been established after the application of the positive stressing voltage. It is difficult to determine from CV analysis alone what type of trap is associated with these charges. This is because Donor traps are neutral when filled and positive when empty whereas Acceptor traps are negative when filled and neutral when empty[2]. Therefore only the dominant charge can be determined. However, the following observations concerning Figure 4.7 can be made:

I. In the first instance, the depletion region of the virgin CV curve is on the positive half of the gate voltage scale. Therefore the virgin diode must have in the bulk and/ or interface traps a net negative charge, causing a positive charge image on the silicon surface. Hence, the diode is in inversion at zero applied bias.

II. However when the diode is stressed with positive bias, the CV curve shifts to the left as seen in Figure 4.7. Hence the large positive charge on the silicon surface has reduced which would be due to the reduction of the net negative oxide charge. The likely event is that at the insulator interface electrons are ejected from the bulk to the gate electrode when a positive bias is applied.

III. A forming process also occurs since the absence of hysteresis implies the elimination of traps during positive stress.

The argument for this is as follows:

When a positive stress bias is applied to the gate, the silicon surface is populated with electrons. Two things can happen, either these electrons in the silicon surface are

injected into the oxide traps near the interface with the insulator or electrons can be ejected from the oxide traps near the Al electrode.

In the former case, the injection of electrons from the silicon can either decrease the positive charge by filling donor states or increase the negative charge by filling the acceptor states. In both circumstances the net negative charge will increase and the CV curve will shift to the right. In the latter case, when the electrons are ejected from the oxide at the interface with the Al electrode, the reverse is expected to occur i.e. increase in positive charge. This is due to increase in empty donor states (positive charge) or decrease of negative acceptor states (neutral). In this occasion the CV curve will be shifted to the left.

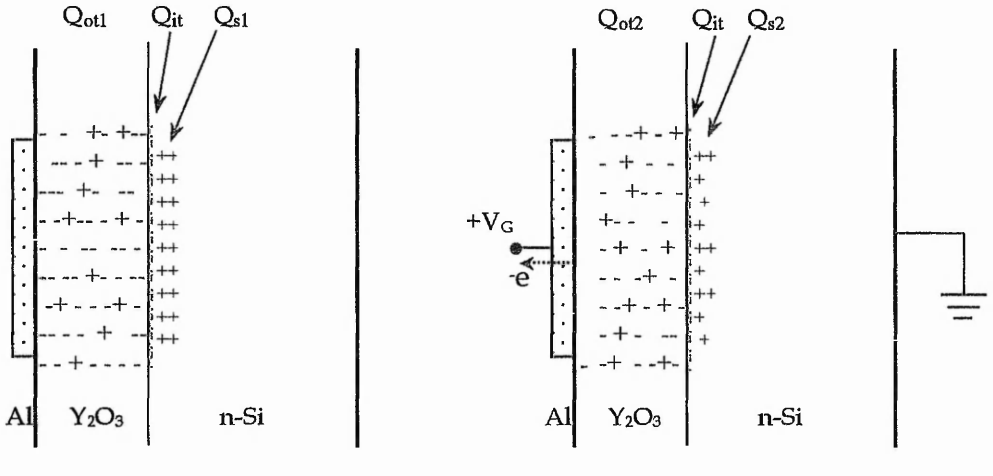


Figure 4.8 Cross-section of Y_2O_3 MIS structure showing that the bulk in a non-annealed sample has net negative charge (LEFT), however when the gate is made positive, some of the negative charge flows out through the gate (RIGHT).

These events are shown schematically in Figure 4.8, where $-Q_{ot1} > -Q_{ot2}$ and $Q_{s1} > Q_{s2}$. Q_s is the image charge appearing on the silicon surface. It was identified in the previous chapter that the thin film material closer to the interface of the silicon had smaller crystallites, and thus consisted of higher bulk traps. The trap density reduces as the thickness increases because crystallisation improves with thickness. This was further

verified because the event described above occurred only in the thinner samples. The transferred charge calculated using Eq.4.5 for 50nm thick samples is **-1.71 nC** whereas for 100nm samples it is **-0.7 nC**. The negative value means negative charge is transferred. In thicker samples, negligible shifting was measured. The decreasing charge value suggests a decreasing trap density at the Al/Insulator interface with increasing Y_2O_3 thickness.

In addition, as the sample thickness increases, the total trapped charge in the bulk of the insulator would also increase. However, the effect of these charges to the silicon surface would be governed by their distribution across the insulator, hence from Eq. 4.4, γ would be significantly influential when considering insulator thickness. ϕ_{mS}, Q_{it} and Q_f are not expected to vary with insulator thickness. Q_f is assumed to exist close to the interface of the silicon. Therefore only the effects of Q_m and Q_{ot} would be detected as variation in V_{FB} with insulator thickness. However the effect of mobile ions were not detected at room temperature. This is because the direction of the hysteresis occurred in the opposite direction to what would be expected if mobile ions were present.

Therefore replacing the sum of ϕ_{mS}, Q_{it}/C_{ins} and Q_f/C_{ins} with a constant K, Eq. 4.3 would become

$$V_{FB} = K - \gamma\,(Q_{ot}/C_{ins}) \qquad \text{Eq. 4.6}$$

assuming $\rho(x)$ is approximately the same for a short range of thickness, hence γ would equal the oxide thickness and the above equation would become

$$V_{FB} = K - d\alpha \qquad \text{Eq. 4.7}$$

where $\alpha = Q_{ot}/C_{ins}$ and Q_{ot} has a negative relation to V_{FB} (Eq. 4.5).

Therefore a plot of V_{FB} as a function of oxide thickness would have a slope Q_{ot}/C_{ins} and intersect the y-axis at K Volt. The measured V_{FB} for non-annealed Y_2O_3 samples as a function of Y_2O_3 thickness is shown in Figure 4.9.

If the charge densities across thickness were the same, the slope would be a straight line because α is proportional to oxide trap charge, Q_{ot}. However, since $\alpha_1 > \alpha_2$ would mean that the bulk charge density in the thinner films is higher than in the thicker films. This evidence further strengthens the model proposed in Figure 3.9. However this graph is not as simple as a straight line, making it impossible to pursue further in this approach to determine the constant K value.

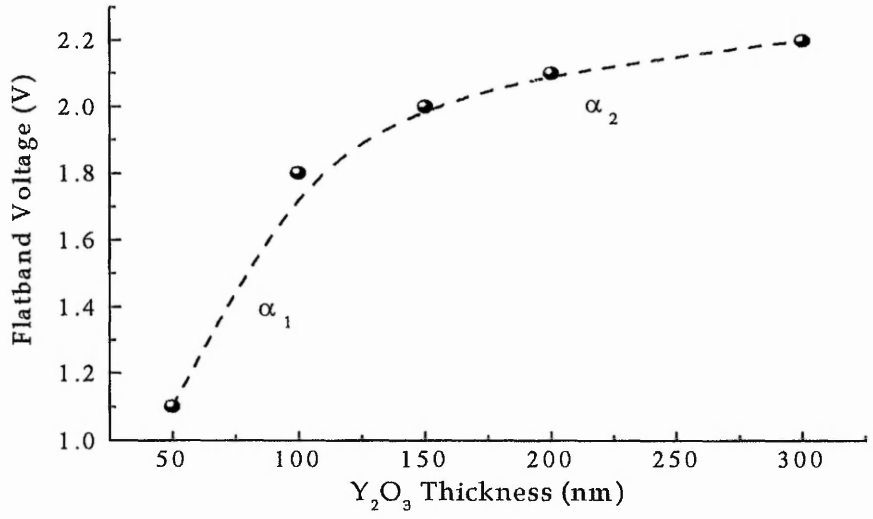


Figure 4.9 Flatband Voltage for non-annealed samples as a function of Y_2O_3 thickness.

However, these samples exhibit hysteresis due to trapping and de-trapping of charge during the CV measurement. The magnitude of hysteresis was dependent on the minimum applied negative voltage in inversion during the CV measurement, as shown in Figure 4.10. By using the difference between the first and second flatband band voltage, the constant K could be discarded. This would bring meaning to Eq. 4.5, therefore in this case making it easier to calculate the injected charge. This is shown in Figure 4.11 for 100nm thick samples annealed at various temperatures. In this case V_{FB} shifted to lower voltages when the diodes were driven more into inversion each time.

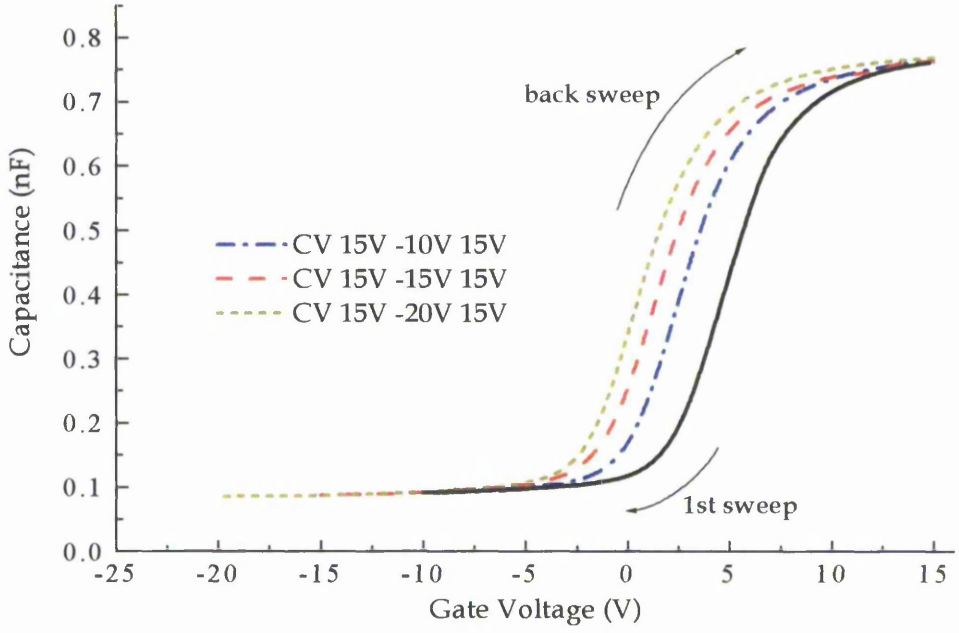


Figure 4.10 CV curves of non-annealed 100 nm thick Y_2O_3 MIS sample with different negative span voltage as detailed in the legend.

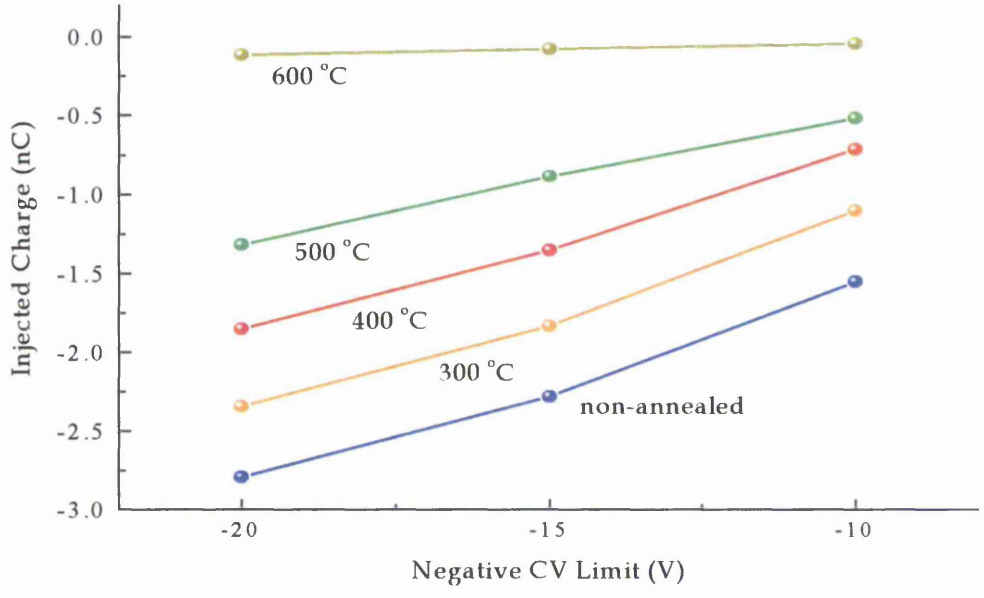


Figure 4.11 Summary of the amount of charge injected as a function of maximum negative voltage bias of CV measurement for 100 nm thick Y_2O_3 MIS diode, annealed at different temperatures. Equation Eq. 4.5 is used to calculate these values.

In accordance with the previous line of argument, application of a negative gate bias during CV measurement will cause inversion (accumulation of holes) in the silicon surface. There are two possibilities, injection of electrons from the Al electrode into the insulator bulk, or ejection of electrons from the insulator bulk to the silicon-inverted surface. In the first case negative charge will dominate (the CV will shift to the right) while in the second case positive charge will dominate (the CV will shift to the left). By considering this argument and the fact that hysteresis is clockwise, the injection must be occurring from the silicon surface.

As is seen in Figure 4.11 this mechanism improves with annealing temperature, reducing the amount of charge trapping/de-trapping due to application of bias. It is important to note that at 600 °C annealing, negligible amount of charge is measured. Therefore the trap density has been significantly reduced due to the heat treatment at this temperature.

In Figure 4.12, normalised CV curves for a 100nm thick Y_2O_3 sample, annealed at various temperatures are shown. The curves indicate flatband voltage shifting along the voltage axis, most prominently noticeable between the non-annealed and the annealed samples. This issue will be discussed later, after all the factors governing V_{FB} has been discussed.

In addition to the shifts:

1) The curves in Figure 4.12 also show various amount of stretch-out in the depletion region, signifying that the amount of stretch-out reduces when the annealing temperature is increased. The cause of stretch-out is due to interface traps responding to the slow varying DC applied bias[1]. The charging of an interface trap, which may exist at various energy levels within the silicon bandgap, depends on the surface potential. The surface potential is a function of gate bias, referred to by Eq. 4.2. With the existence of Q_{it}, the gate charge would also need to contribute towards charging the interface traps. Therefore, this would result in a stretch-out of the CV curve along the gate voltage axis, and the amount would depend on the density of these traps.

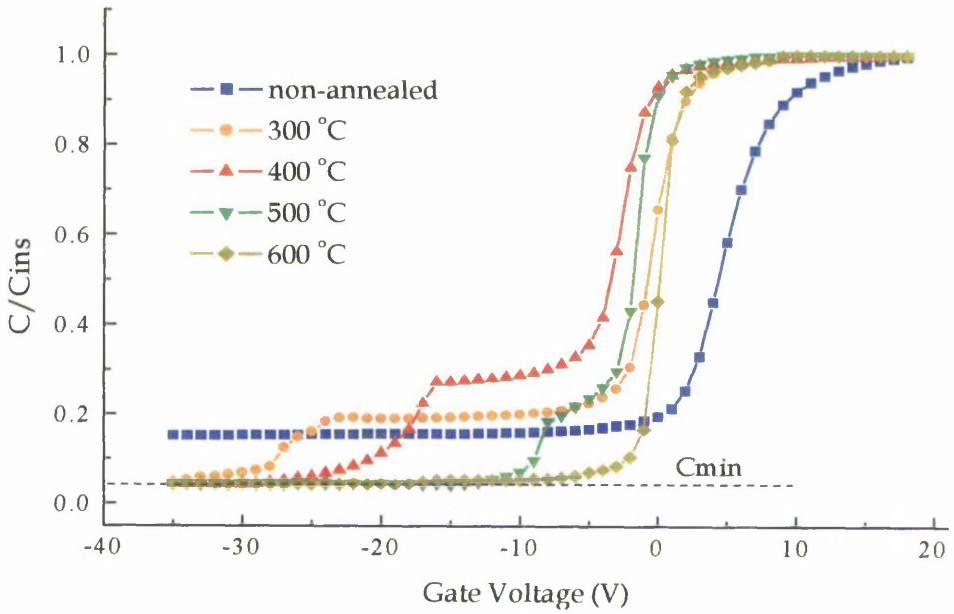


Figure 4.12 Normalised CV curves for 100 nm Y_2O_3 MIS diodes on n-type silicon, annealed at various temperatures. Cmin is the calculated minimum value for these diodes.

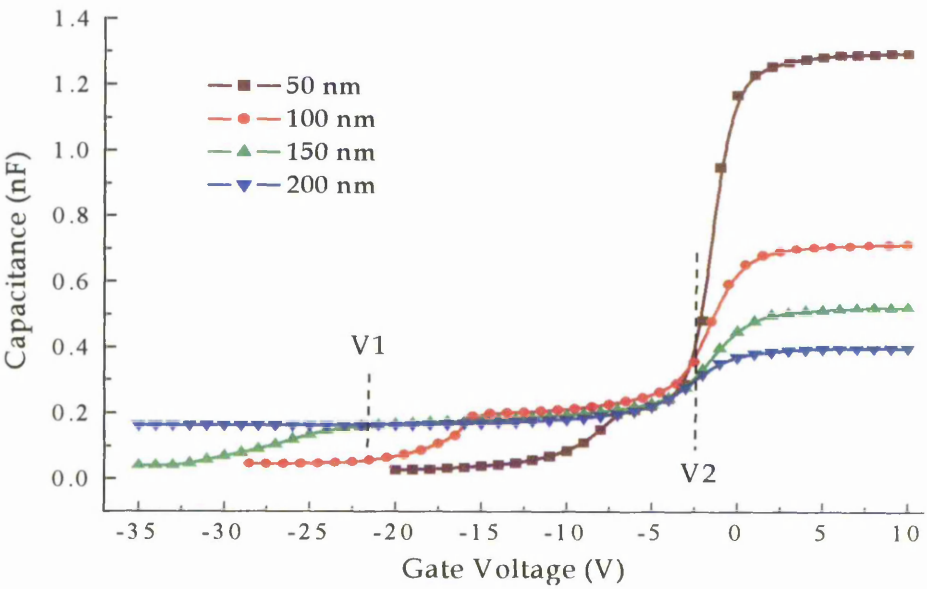


Figure 4.13 CV curves of samples with different thickness annealed at 400 °C. Demonstrates that the pinning voltages span increased for smaller insulator capacitance of thicker films. An example is shown for the 150 nm sample, where the difference of V1 and V2 is the voltage span where C_S is pinned.

2) Only the sample annealed at 600 °C goes into true inversion C_{inv}, for the smallest V_G.

C_{inv} occurs when the maximum depletion width, W_m is reached and is given as[3]

$$W_m = \left[\frac{4 \varepsilon_S kT \ln (N_d/n_i)}{q^2 N_d} \right]^{1/2} \qquad \text{Eq. 4.8}$$

where ε_s is the permittivity of silicon given as 11.9 x ε_o, k being Boltzmann's constant given as 1.4 x 10^{-23} joule/ Kelvin, T is the temperature considered, taken as 300 Kelvin, q being charge of an electron given to be 1.6 x 10^{-19} coulomb and n_i being the intrinsic carrier concentration for silicon given to be 1.45 x 10^{10} cm^{-3}.

C_{inv} per area is given as

$$C_{inv} = \frac{\varepsilon_i}{d + (\varepsilon_i/\varepsilon_S) W_m} \qquad \text{Eq. 4.9}$$

where ε_i is the permittivity of the insulator which is approximately 12 x ε_o and d is the thickness of the insulator which is 100nm. Therefore the calculated value for the normalised C_{inv} equals to 0.047 and is shown in Figure 4.12 as C_{min}.

The non-annealed sample did not go into inversion for the maximum voltage limit of the CV measurement system. However, the other samples annealed at 300, 400 and 500 °C went into inversion at gate voltages -22, -12 and -6 V respectively. These values are much easier to infer from Figure 4.15. This phenomenon is due to the existence of a large number of interface states. This was observed before in Semi-Insulating Polycrystalline Silicon diodes[10]. As these states would require charging, the capacitance is pinned for certain span of voltages. Figure 4.13 demonstrates this, which shows CV curves of samples with different thickness annealed at 400 °C. The voltage span is an indication of the density of interface states. It must be noted that for this reason and the fact that the measured values for the diodes go to the theoretical inversion capacitance value eventually at higher negative voltage, this is not a case of deep depletion.

The charge trapped at a certain band bending can be calculated for the different insulator thickness. This can be done using Eq. 4.10 given below

$$Q_{it}(\psi s) = |V1 - V2|\ C_{ins} \qquad \text{Eq. 4.10}$$

Q_{it} is expected to be the same for all the insulator thickness. As can be seen from Figure 4.13, as the insulator capacitance decreases (insulator thickness increases), the voltage span, $|V1 - V2|$ increases considerably in order to charge the interface states fully. Eventually when the states get filled up the diode would start to approach inversion. The gate voltage at which the C_S begins to be pinned would be the point where the trap states exist in the silicon bandgap.

By comparing the measured CV curves that includes contribution to the capacitance from the interface traps and an ideal MIS diode response, the position of these traps within the bandgap could be determined. Also, the density of interface traps (D_{it}), could be approximated. This would require generation of the ideal Capacitance versus silicon band bending, ψ_s, graph. This method originates from the High Frequency Capacitance technique developed by Terman[1], described comprehensively by Nicollian and Brews in reference [2], Section 8.2.4.

In these samples, bulk charges and ϕ_{ms} contribute an additional voltage shift to the V_{FB} value. Hence the measured CV curves are shifted parallel along the voltage axis. In order to compensate for this effect, the measured curves should be translated accordingly, so the V_{FB} of the measured value will coincide with the $\psi_s = 0$ point of the theoretical graph.

The method is tedious, however an appreciative representation can be obtained. The ultimate objective is to relate the values of ψ_s of the theoretical MIS diode and the gate voltages of the measured CV graphs for common capacitance values. To acquire D_{it} the derivative $dV_G/d\psi_S$ must be found.

The ideal capacitance is the series capacitances of the Insulator layer, C_{ins} and the Silicon Surface capacitance, C_S and is given by Eq. 4.1 and repeated here again

$$C_{ideal} = \frac{C_{ins}\, C_S}{C_{ins} + C_S}$$

The Silicon Surface capacitance, Cs as denoted previously, is a function of ψ_s and is given below for the different regions[2]

- At flatband, $\psi_s = 0$

$$C_S = C_{FBS} = \frac{A\,\varepsilon_s}{\lambda_n} \qquad \text{Eq. 4.11}$$

- Strong Accumulation, $\psi_s > 0$

$$C_S = \frac{C_{FBS}}{\sqrt{2}} \exp\left[\frac{v_S}{2}\right] \qquad \text{Eq. 4.12}$$

- Depletion and weak inversion, $\psi_s < 0$

$$C_S = \left[\frac{C_{FBS}}{\sqrt{2}}\right] \frac{[\exp(v_S) - 1]}{[-(v_S + 1) + \exp(v_S)]^{1/2}} \qquad \text{Eq.4.13}$$

where A is the diode area, v_S is ψ_s x q/kT , and λ_n is the Debye length defined as a measure of the distance over which a charge imbalance is neutralised by majority carriers under equilibrium condition and is given by

$$\lambda_n = (\varepsilon_s k\, T/q^2\, N_d)^{1/2} \qquad \text{Eq. 4.14}$$

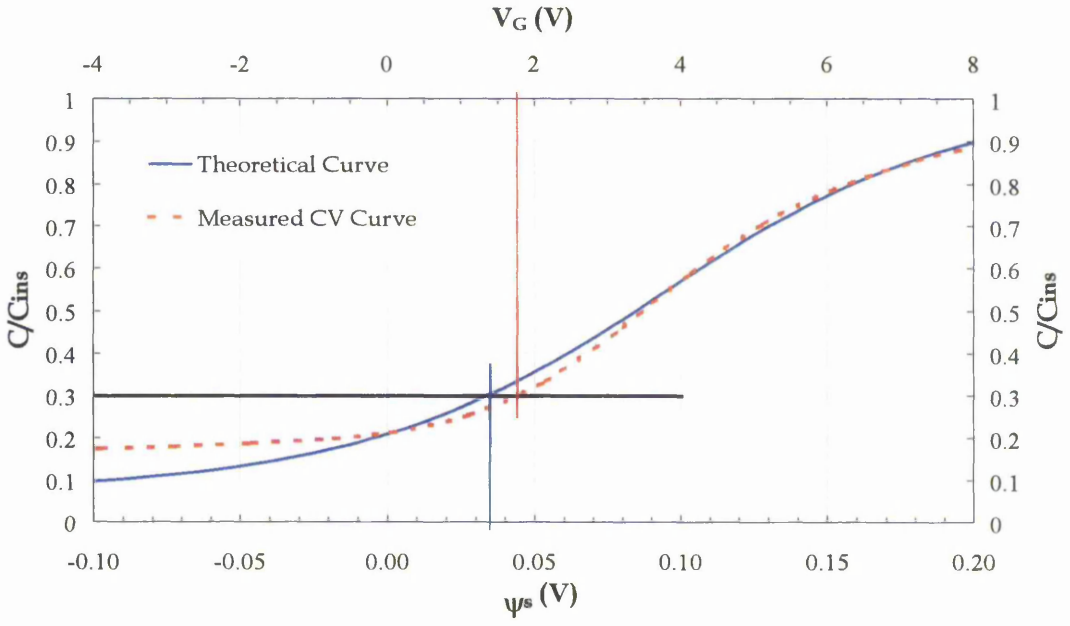


Figure 4.14 A theoretical high frequency capacitance versus ψ_s graph compared with a measured CV curve, of a non-annealed MIS sample with 100nm thick Y_2O_3. An examples, at V_G = 1.75 V corresponds to capacitance ratio determined from the curve, C/Cins = 0.3. This point corresponds to band bending of ψ_s = 0.035 V shown as straight dark lines. In the actual graphical comparison to obtain the data points, the graph is focused in at least 5 times.

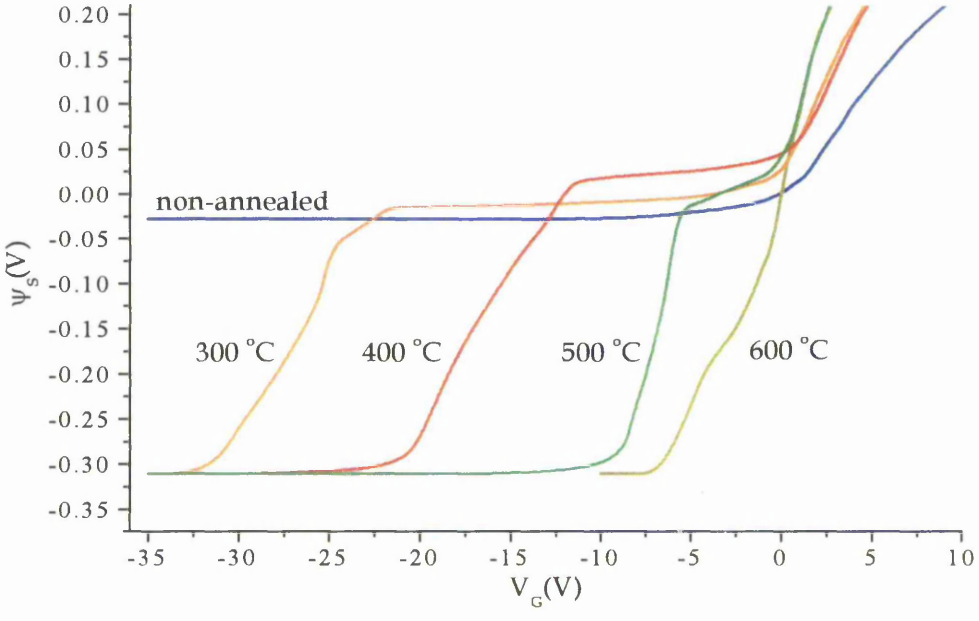


Figure 4.15 Plot of ψ_s versus V_G for data from Figure 4.12.

A Matlab program was written to generate the theoretical curve. By graphically comparing the theoretical graph and the measured CV curve a relation between ψ_s and V_G was found. This is shown in Figure 4.14, for the non-annealed sample data from Figure 4.12, translated along the voltage axis so that V_{FB} relates to ψ_s at zero. Plots for ψ_s versus V_G for samples annealed at different temperatures are shown in Figure 4.15.

The interface trap density is given by

$$D_{it}(\phi_s) = \frac{1}{qA}\left[C_{ins}\left[\frac{dV_G}{d\psi_S} - 1 \right] - C_s(\psi_s) \right] \qquad \text{Eq. 4.15}$$

However when large state causes pinning, the derivative $dV_G/d\psi_S$ would go to infinity. Therefore to approximate D_{it} of such state, Eq. 4.16 is used and the value added to the value from Eq. 4.15 just before the pinning.

$$D_{it} = \frac{Q_{it}(\psi_s)}{q\,A} \qquad \text{Eq. 4.16}$$

In Figure 4.16 the calculated density of interface states as a function of the silicon bandgap energy is shown. It reveals that the peak density decreases with annealing temperature. This peak is responsible for the pinning effect in the CV measurement. Also demonstrated is that annealing causes reduction of interface states of Y_2O_3 MIS structure. As more ordering of the interface occurs with increase of annealing temperature the interface charge properties improves. This could serve as an explanation for the reduction in the amount of hysteresis seen with annealing temperature, shown in Figure 4.11.

The interface charge would also contribute towards V_{FB} governed by Eq. 4.3. Therefore as the density of states, (Q_{it}) decreases with annealing temperature, V_{FB} will be less influenced by the smaller Q_{it} of samples annealed at higher temperatures. However only a qualitative picture may be obtained, as the interface charge could not be calculated using this method. This is because the technique relies on shifting the CV curve to compensate for any charges.

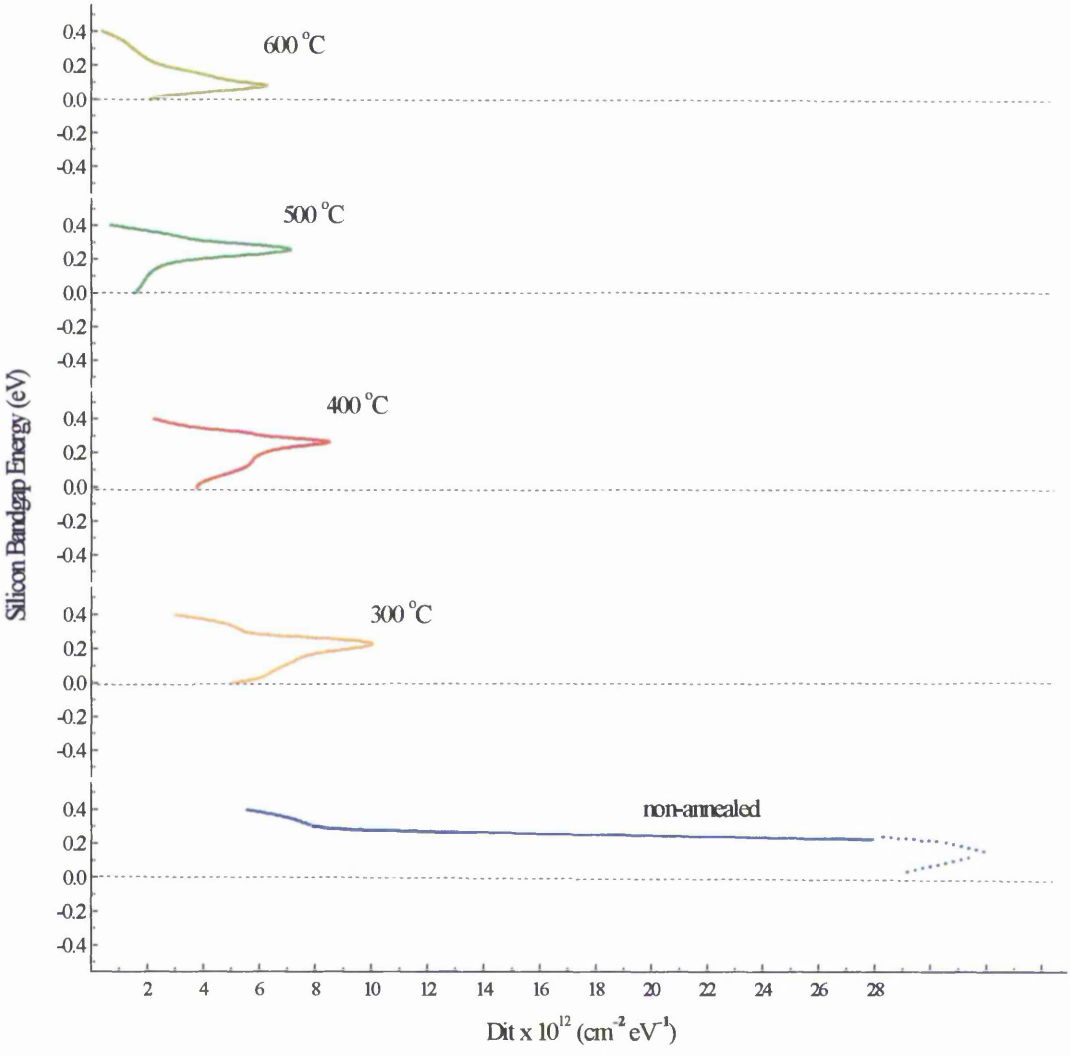


Figure 4.16 Calculated density of interface state versus silicon bandgap for Y_2O_3 MIS diodes, annealed at different temperatures. Dashed lines indicate the silicon mid-gap (intrinsic Fermi level). These data corresponds to CV data from Figure 4.12. The figure clearly demonstrates that the density of the large discrete state reduces with annealing temperature.

The net charge associated with insulator bulk alone has been found to be positive by various groups working on thin film Y_2O_3 MIS diodes grown by R.F. Sputtering and other deposition techniques[11,12,13,14,15,16,17]. This would mean that the flatband voltage would be in the negative half of the gate voltage scale. All these groups have also reported that annealing causes the flatband voltage to move closer to zero volts by reducing the positive charge.

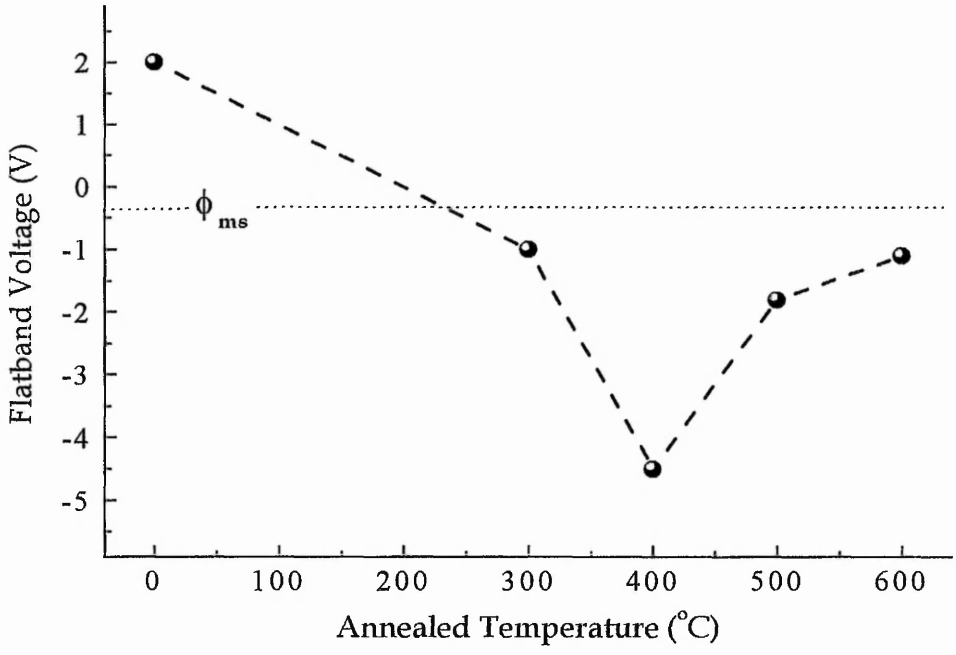


Figure 4.17 Measured V_{FB} for 100 nm thick Y_2O_3 MIS samples as a function of annealed temperature. The dashed line indicated by ϕ_{ms} is the potential due to work function difference between Al and Si with a doping density of 1×10^{-14} cm^{-3}.

In Figure 4.17 the measured V_{FB} for Y_2O_3 MIS samples as a function of annealed temperature is shown. On another independent experiment, IV measurements were performed on 300nm thick Y_2O_3 samples of which the curves are shown in Figure 4.18. The lowest current point on the IV curve corresponds to the flatband voltage of the MIS system where no net current is flowing through the device. These points seem to

indicate the same pattern to the V_{FB} obtained from CV curves as shown in Figure 4.17, confirming the position of these values on the voltage scale.

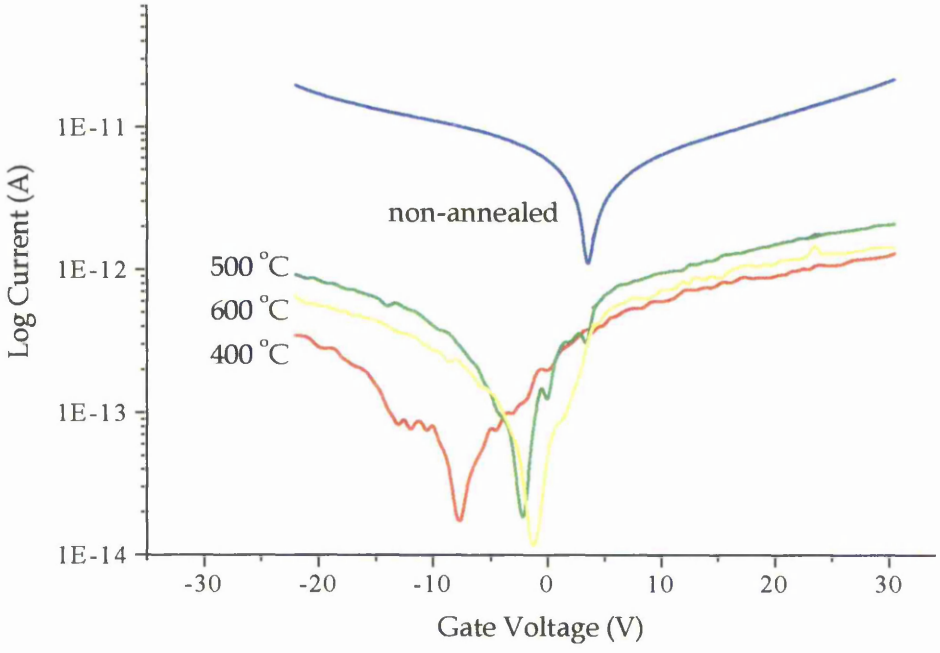


Figure 4.18 IV curves for 300 nm thick Y_2O_3 MIS with 1mm diameter diodes, annealed at different temperatures. The lowest current point is an indication of flatband voltage.

As noted previously, the work function difference between the Aluminium gate and the Silicon substrate, ϕ_{ms} would also cause the V_{FB} to shift. The value given in literature[2] for ϕ_{ms} between Aluminium and silicon with doping density of 1×10^{14} cm^{-3}, is -0.4V. A straight line is drawn across the graph in Figure 4.17 to mark the position of V_{FB} of a MIS diode without any charges present.

In Chapter 3, it was concluded that the bulk of the insulator showed a more prominent improvement in crystal quality at annealing temperatures higher than 300 °C. This relates to improvement in the trap density associated with defects. The defects are believed to be mainly due to oxygen vacancies and broken bonds. These defects are trap centres, which can hold charge. However annealing reduced these positive charges in the bulk, which is clearly seen between annealing temperatures 400 and 600 °C in Figure 4.17. Therefore at above 400 °C annealing temperature a decrease in oxygen related defects takes place hence restoring compositional homogeneity of the Y_2O_3 thin film material.

Concomitant with bulk charge reduction, the interface state density is also reduced significantly with annealing temperature, as shown in Figure 4.16. Since acceptor traps were found to be present at the silicon/insulator interface in the hysteresis experiment, it is reasonable to assume that the large density of interface states detected with the Terman analysis is also attributed to the dominance of acceptor ions. Therefore a negative charge exists at the interface due to these states. Since it is also plausible that large quantity of positive charge is present in the diode annealed up to 300 °C, a balance of charges is achieved. As the annealing temperature is increased the interface state density is reduced at higher rate than the positive charge. At 400 °C with the interface density having been reduced considerably, the flatband voltage reaches its lowest negative value indicating the existence of a dominant positive charge. Further increase of the annealing temperature up to 600 °C reduces the difference of positive and negative charges. However the positive charge is still prevailing at 600 °C and hence the flatband voltage is slightly negative.

4.6 Summary and Conclusions

The oxide integrity of Y_2O_3 thin film was investigated as a function of thickness and annealing temperature. Charges related to defects were characterised and the improvement that annealing causes to the MIS system is depicted.

It has been demonstrated that the thin film material closer to the interface of the silicon consists of higher bulk traps and the trap density improved as the thickness increases. Evidence obtained from the CV analysis in this study, strengthen the crystalline defect thickness model proposed in Chapter 3 (Figure 3.9).

These samples exhibit hysteresis in CV measurement due to trapping and de-trapping near the interface of the silicon. However, it has been shown that the amount of hysteresis, reduces with annealing temperature. Sample annealed at 600 °C, showed negligible amount of hysteresis causing charge.

It is concluded that the deposition temperature is high enough for the energetic species to create considerable damage at the Si/Y_2O_3 interface. This creates large interface trap states. The existence of large interface states caused pinning of the Fermi level at the depletion region. Terman's[1] method was used to study this phenomenon, which reveals existence of a large density discrete state. This state had value as high as 10^{13} cm^{-2} eV^{-1} for samples annealed at lower temperature. This prevented the MIS system to move to the inversion region for a certain span of voltages during CV measurement. As the samples were annealed at higher temperatures the pinning voltage span became smaller. The non-annealed sample did not go into inversion and was pinned for the maximum voltage range of the CV measurement system. It has been demonstrated that a decrease in the density of interface states with increase in annealing temperature explains this observation. The reduction in Q_{it} is also believed to be the reason for the reduction in hysteresis seen with annealing temperature.

The measured V_{FB} for Y_2O_3 MIS samples shows a positive value for the non-annealed samples and negative values for the annealed samples. Samples annealed at 400 °C had the lowest negative V_{FB} value. It is proposed that the effects of negative interface charge and positive bulk charges of the diode cause V_{FB} to be shifted in this fashion as a function of annealing temperature. The complimentary effect of these two charges to the image charge appearing on the silicon surface is given as an explanation.

Presently the bulk and interface properties, such as bulk charges and D_{it} are on the high end for use as an alternative to SiO_2. However thermal treatment of the MIS structure has demonstrated a reduction in parasitic charges. Additionally, the high dielectric constant and low leakage current values of the material does carry a potential for this oxide for use as an alternative gate dielectric.

4.7 References

1 L.M. Terman, Solid-State Electronics, Pergamon Press 1962 5, Pg. 285

2 E.H. Nicollian & J.R.Brews, MOS Physics and Technology, Wiley-Interscience 1982

3 S.M. Sze, Physics of Semiconductor Devices, 2nd Ed, 1981

4 A.S. Grove, E.H. Snow, B.E. Deal & C.T. Sah, J. Appl. Phys., 35, 8 1964 Pg. 2458

5 A. Berman & D.R. Kerr, Solid State Electronics 17 1974 Pg. 735

6 G.D. Wilk, R.M. Wallace & J.M. Anthony, J. Appl. Phys. (Review), 89/10 2001 Pg. 5243

7 R.J. Hillard, J.M. Heddleson, D.A. Zier, P.Rai-Choudhury, & D.K. Schroder in Diagonostic Technique for Semiconductor Materials and Devices, Electrochemical Soc., Pennington 1992, Pg. 261

8 B.E. Deal, IEEE Tran. Electron Devices, Ed. 27, 1980 Pg. 606

9 D.K. Schroder, Semiconductor Material and Device Chracterization, 2nd Ed., Wiley-Interscience 1998

10 K.M. Brunson, Ph.D. Thesis University of Bradford, UK Chracterisation of Semi-Insulating Polycrystalline Silicon 1987.

11 L.A. Ragnarsson, S. Guha, M. Copel, E. Cartier, N.A. Bojarczuk & J. Kransinski, Appl. Phys. Lett. 78, 26 2001 Pg. 4169

12 C.H. Ling, J. Bhaskaran, W.K. Choi & L.K. Ah, J. Appl. Phys., 77, 12 1995 Pg. 6350

13 M.E. Hunter, M.J. Reed, N.A. El-Masry, J.C. Roberts and S.M. Bedair, Applied Phys. Lett. 1935 2000

14 L. Manchanda, M. Gurvitch, IEEE Electron Device Lett. 9, 4 1988 Pg 180

15 C.H. Ling, J. Bhaskaran & W.K.Choi, Vacuum 43 5 1992 Pg. 753

16 A.C. Rastogi & R.N. Sharma, Semicond. Sci. Tech. 16 2001 Pg. 641

17 K. Kakuno, D. Ito, N. Fujimura, T. Matsui, T. Ito Article in Press, J. of Crystal Growth 2002

CHAPTER 5

PROPERTIES OF ZnS:Mn PHOSPHOR

5.1 Introduction

The word Phosphor means, "light bearer" in Greek. An important property of a phosphor material is its luminescence[1]. Luminescence is defined as the generation of non-thermal electromagnetic radiation when a substance is given energy by some means of excitation process. The electromagnetic radiation emitted by a luminescent material is usually in the visible range, but can also be in other spectral regions, such as the ultraviolet or infrared. Zinc Sulphide doped with Manganese, (ZnS:Mn) is a luminescent material. The II-VI compound doped with the transition-metal emits light in the visible range, with a peak wavelength centered at ~585nm and a typical spectral bandwidth of ~50nm. This material is the core of an ACTFEL device, and is defined as the active layer. As it is the source of the light generation in the device, it plays an important role in its efficiency. Hence, the light generation properties of this material are vital to be known for optimum tuning of the ACTFEL device. This chapter consequently deals with an investigation of the electrical, structural and phosphor efficiency of ZnS:Mn as a function of growth parameters.

5.2 Structural Properties

X-Ray Diffraction (XRD) measurements were carried out on the ZnS:Mn powder source material used for the sputtering target. It was found that the powder consists of crystals from only the hexagonal phase of ZnS. A XRD graph of the ZnS:Mn powder material is shown in Figure 5.1. For reference, in Table 5.1 all the XRD diffraction planes found previously for cubic and hexagonal phase of ZnS:Mn are given.

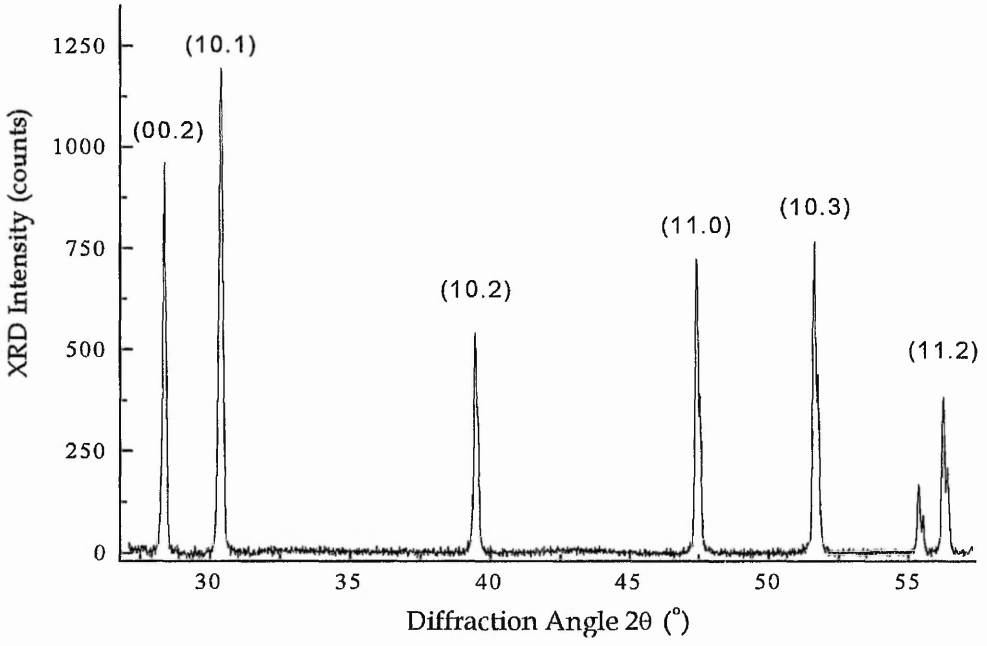


Figure 5.1 XRD pattern of ZnS:Mn powder source material used in sputtering target.

Cubic	**(hkl)**	111	200	220	311		
	2 θ (°)	28.56	33.09	47.50	56.36		
Hexagonal	**(hkl)**	00.2	10.1	10.2	11.0	10.3	11.2
	2 θ (°)	28.49	30.52	39.59	47.53	51.74	56.36

Table 5.1 The expected diffraction lines in XRD patterns of ZnS:Mn. (hkl) are the Miller Indices and 2θ is the XRD diffraction angle[2,3,4].

Thin film samples of 800nm thick ZnS:Mn were grown at different substrate temperature on 300nm thick Y_2O_3 thin film on Silicon (100) wafers using the deposition system described in Section 2.2.1. XRD measurement carried out on the non-annealed samples shows a predominantly cubic phase based on the diffraction peaks listed in Table 5.1, and only a single plane (10.1) of the hexagonal phase, in its polycrystalline structure. The preferred orientation of the ZnS:Mn thin films was indicated by the cubic (111) plane showing the highest intensity[5,6,7]. XRD patterns of the measurements are shown in Figure 5.2.

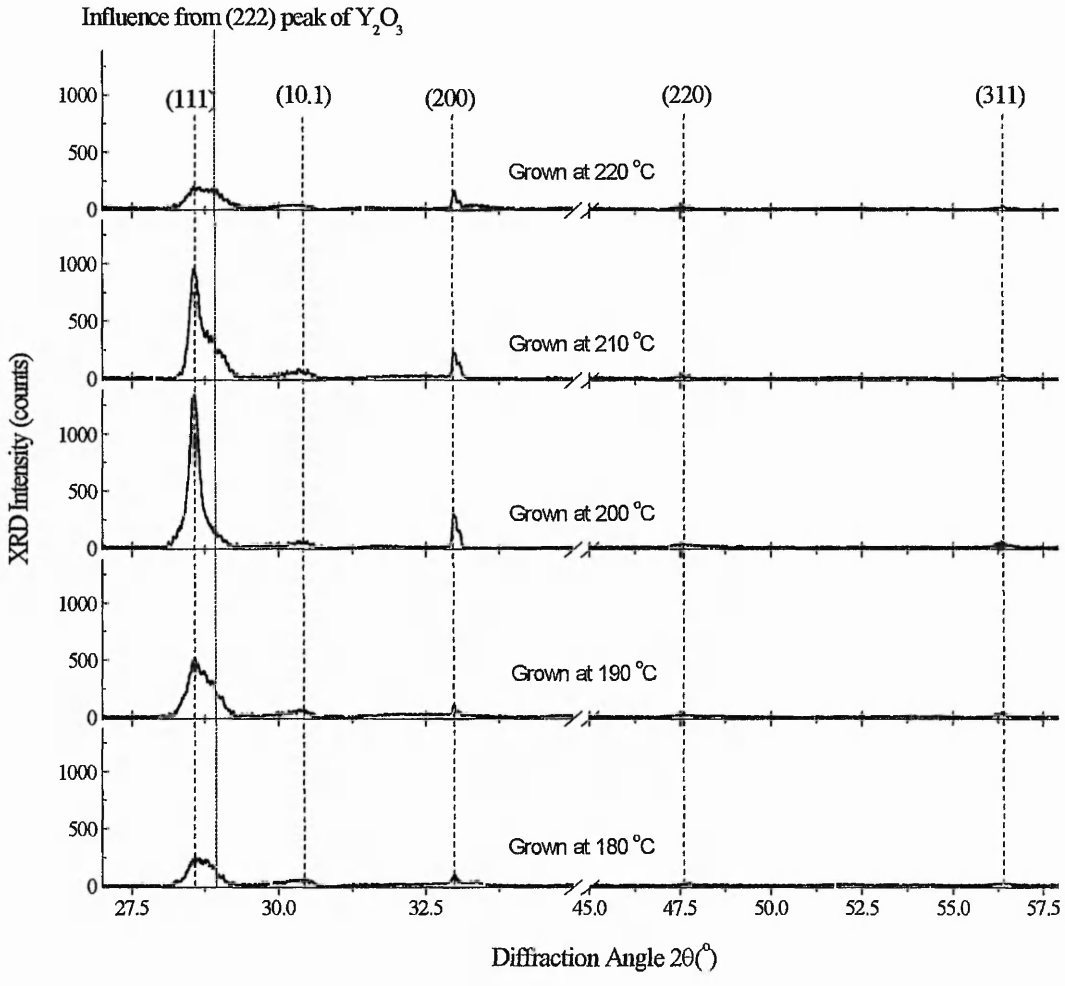


Figure 5.2 XRD patterns of non-annealed thin film ZnS:Mn grown at different substrate temperature fabricated on Y_2O_3 thin film on Silicon (100) substrate.

The XRD peak intensities corresponding to plane peaks (220) and (311) were very small. However it can be clearly seen from the XRD pattern that the sample grown at 200 °C has the best cubic crystalline properties. It has the highest peak intensity for all its cubic phase planes and is least influenced by the underlying Y_2O_3 thin film (222) plane.

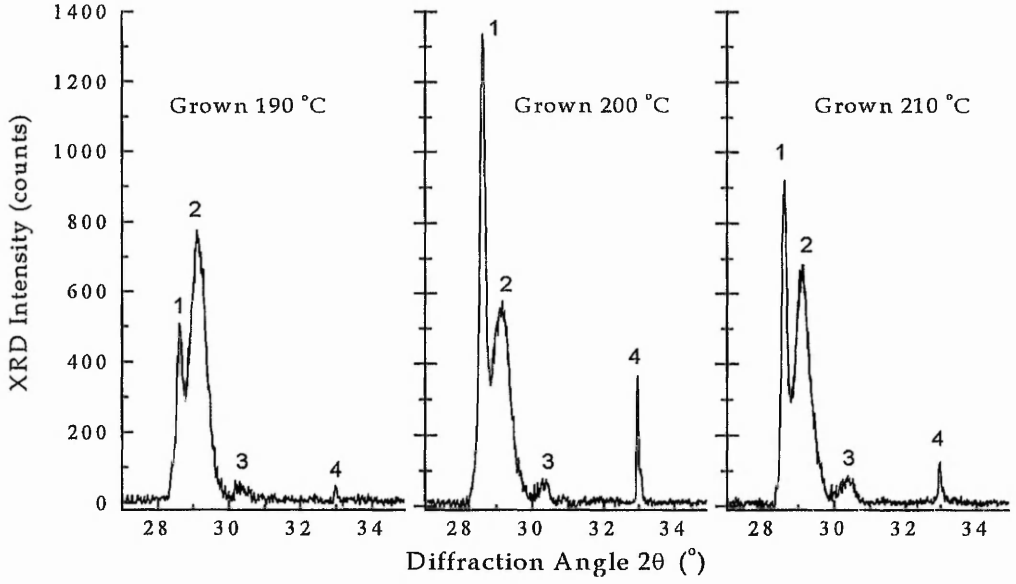


Figure 5.3 XRD patterns of thin film ZnS:Mn grown at different substrate temperatures on Y_2O_3 thin film on Silicon (100) substrate and annealed at 500 °C. Labels "1" corresponds to plane (111), "3" is (10.1) and "4" is (220) of ZnS thin film and label "2" is for plane (222) of Y_2O_3.

These samples were then annealed at 500 °C for 1 hour and XRD measurements were performed again of which patterns are shown in Figure 5.3. Samples grown at 200 °C show more pronounced crystalline quality than the samples grown at other temperatures studied. This effect has also been observed elsewhere[7,8]. The patterns also show a clearer separation between the (111) plane of the ZnS:Mn and constructive interference of Y_2O_3 (222) plane. Again, on the annealed samples the influence of the underlying Y_2O_3 has a reduced effect on ZnS:Mn thin film grown at 200 °C. It is apparent that the ZnS:Mn thin film grown on Y_2O_3 thin film at 200 °C promotes the growth of cubic structure crystallites. Other researchers have utilised ~200 °C as the deposition temperature for ZnS:Mn thin film[8,910,11], which was found to be optimum to

produce good structural properties. However no reason has yet been given for this optimum temperature. A plausible explanation could be that at 200 °C substrate temperature the Zn and S species may have the optimal thermal energy needed to recombine at the surface of the substrate for fabricating a superior thin film cubic crystal structure.

However this was not the case when the samples were directly grown on silicon (100). No changes in the XRD plane peaks were observed for all growth temperatures. This strongly suggests that the silicon (100) has a pronounced effect on the growth structure of the ZnS:Mn crystallites. In Figure 5.4, XRD patterns of ZnS:Mn grown at 200 °C and annealed at 500 °C fabricated directly on Silicon (100) and Y_2O_3 thin film are shown.

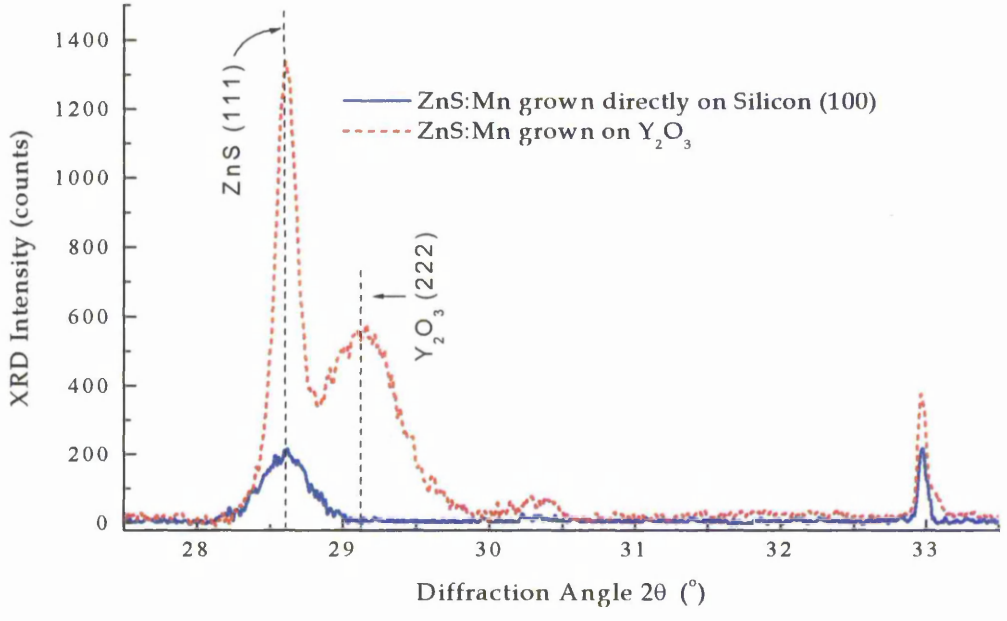


Figure 5.4 XRD patterns of thin film ZnS:Mn grown on Y_2O_3 thin film and on Silicon (100) substrate are shown. These samples were grown at 200 °C and annealed at 500 °C.

The peak intensity of the ZnS:Mn (111) plane grown on Silicon (100) is much lower compared to the thin film grown on Y_2O_3, as seen in Figure 5.4. Additionally, the measured average crystallite size calculated from plane (111) of ZnS:Mn grown on Silicon (100) is 22 ***nm*** whereas the one grown on Y_2O_3 thin film is ***46 nm*** (calculated using

Eq. 2.11). Therefore this result suggests that the <222> oriented Y_2O_3 encourages the same direction <111> orientated ZnS:Mn crystal growth. The fabrication rate of ZnS:Mn thin film on silicon is 40 Å/min whereas on Y_2O_3 it is 71 Å/min. The faster fabrication rate on Y_2O_3 surface also suggests that the surface promotes the crystal growth. Raman spectrum measurements were performed on both types of samples. The spectra obtained are shown in Figure 5.5. The band in the region of ~ 350cm^{-1} represents the cubic phase of ZnS thin film[12,13]. The higher intensity of the peak for the ZnS:Mn thin film grown on Y_2O_3 confirms that the cubic crystal structure is of higher quality. This is clear evidence that Y_2O_3 thin film insulator has good interfacial properties to produce ZnS:Mn phosphor of superior crystalline cubic phase structure.

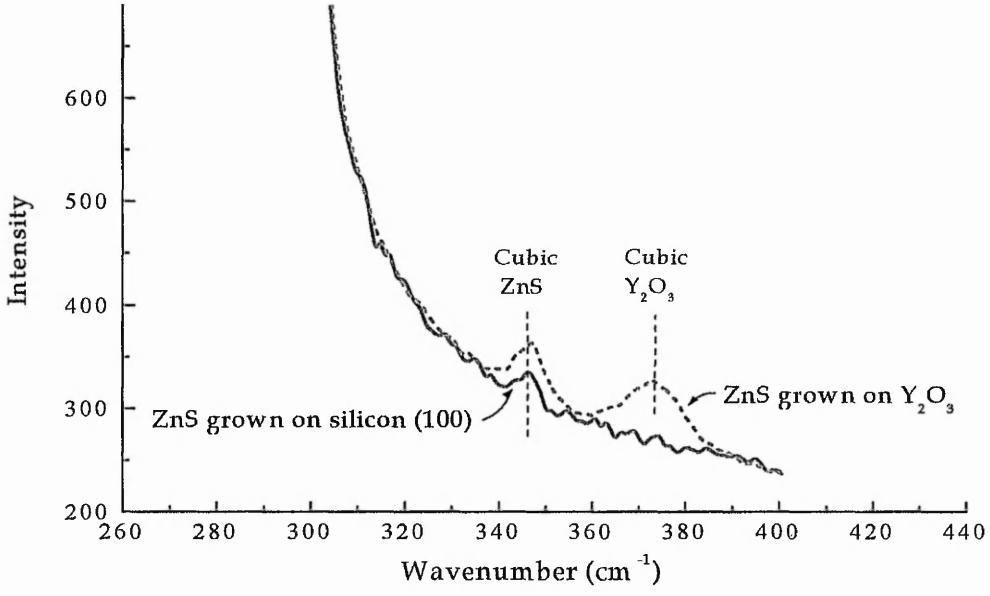


Figure 5.5 Raman Spectrum for ZnS:Mn thin film grown on Y_2O_3 thin film and on Silicon (100) substrate. These samples were grown at 200 °C and annealed at 500 °C.

The bi-layer samples with Y_2O_3 and ZnS:Mn thin film presents a complication when considered for electrical and photoluminescent measurements. The capacitive coupling between the layers makes it difficult to isolate the electrical properties of the ZnS:Mn layer. In photoluminescent measurement, the thin film Y_2O_3 with a lower refractive index than ZnS:Mn as mentioned in Section 2.4.2 causes light confinement in the

phosphor layer. Additionally, some light is transmitted into the Y_2O_3 layer, which travels through the layer and is back reflected at the mirror like surface of the silicon interface. The returning light rays below the critical angle re-enter the ZnS layer causing selective interference in the light wavelength, which is a function of the Y_2O_3 layer thickness. These effects make the spectrum measurement unfit for quantitative characterisation.

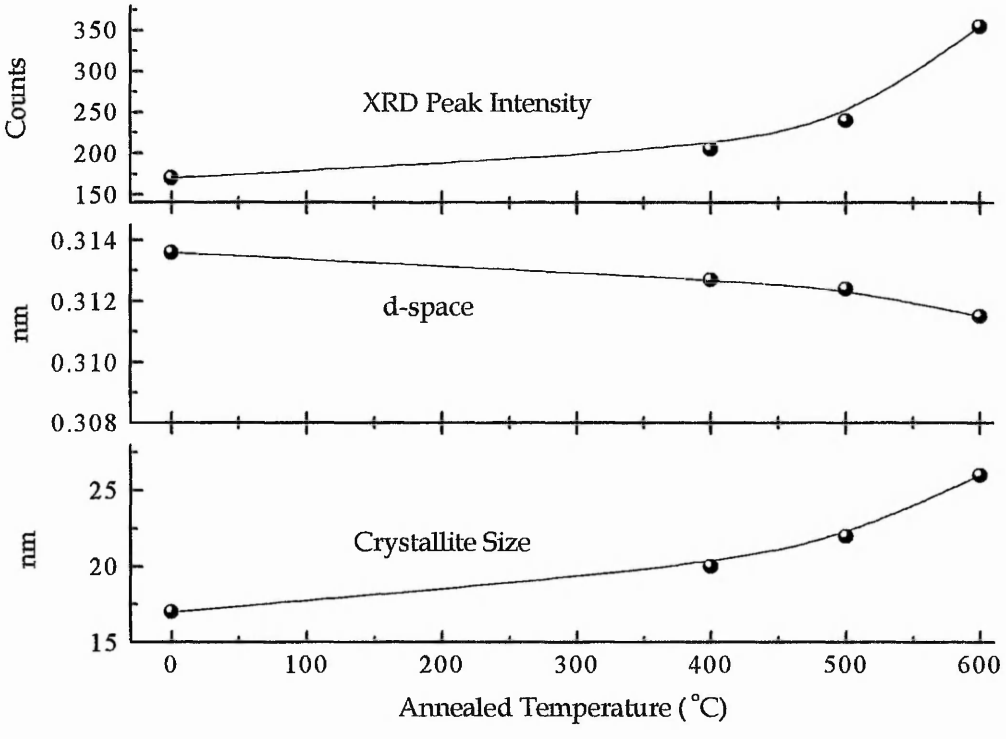


Figure 5.6 XRD structural analysis for thin film ZnS:Mn grown on silicon (100) at 200 °C as a function of sample annealed temperature. The data corresponds to the main plane peak (111).

Taking these factors into account, the electrical and photoluminescent measurements were only carried out on thin film ZnS:Mn samples grown directly on silicon substrate. Though it has been demonstrated that the interfacial properties have influences on the structural properties of the thin film grown, however it is sensible to assume that the bulk properties of the material grown on silicon and Y_2O_3 would be improved when annealed. On the basis of this assumption, further studies on ZnS:Mn thin films are

performed on the type grown directly on silicon substrate. Structural analysis of XRD measurement for samples of ZnS:Mn grown on silicon at 200 °C, annealed at different temperatures are given in Figure 5.6.

The analysis shows that the average crystallite size increases with annealing temperature as seen in Figure 5.6. It also demonstrates a slight improvement in the ordering of the structure in the <111> direction with increase in annealing temperature. However the d-space did not vary extensively for the annealing temperatures studied, which other groups have also reported[8]. It must be noted that thermally treating this phosphor material does not influence the crystalline quality as much as it does on Y_2O_3 thin films, detailed in Chapter 3.

5.3 Photoluminescence

Photoluminescence (PL), spectra were taken of samples of ZnS:Mn thin films grown at 200 °C and annealed at various temperatures. The peak intensity of the PL spectrum significantly improved with annealing temperature as shown in Figure 5.7.

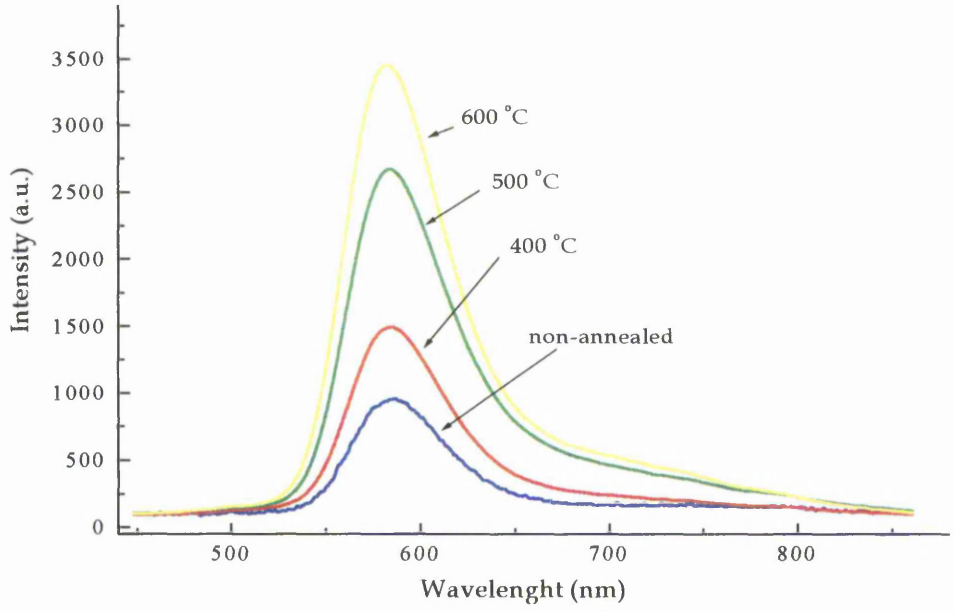


Figure 5.7 PL spectra for ZnS:Mn thin film annealed at various temperatures.

The peak wavelength at 580nm and FWHM spectrum bandwidth of 67nm did not vary for the annealing temperatures studied. In this phosphor material, Mn^{2+} sits as an isoelectronic substitute on a Zn site in the lattice[14]. The Mn substituted on a Zn site will behave as a deep electron trap[15]. The crystal field of the host material on these sites influences the emission wavelength[16,17]. It could be shown utilising Eq. 2.8, that the energy transition responsible for emission at the measured wavelength is equal to 2.12eV. Therefore, annealing the samples at these temperatures did not alter the transition energy level due to Mn ions within the ZnS host material. This is consistent with practically no change observed in the lattice constant (d-space) of the ZnS structure with annealing temperature.

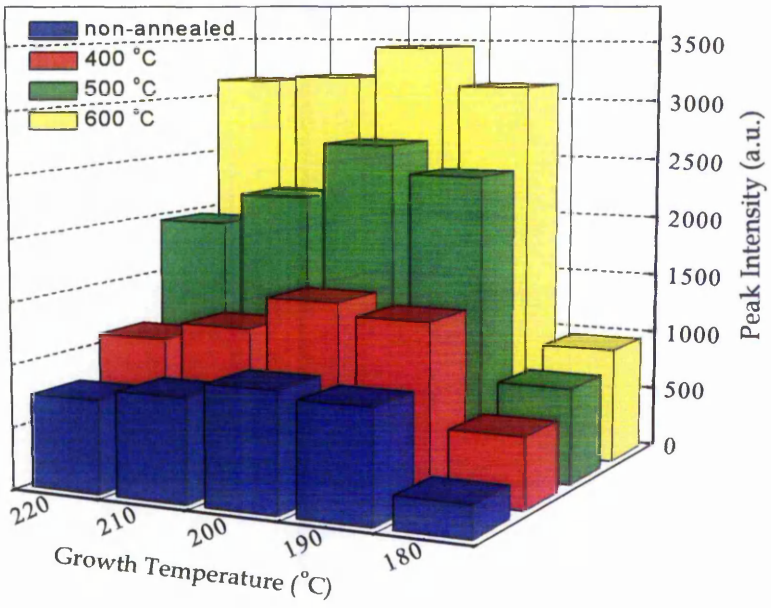


Figure 5.8 Summary of the peak PL intensity for ZnS:Mn thin film grown on silicon substrate as a function of sample fabricated and annealed temperature.

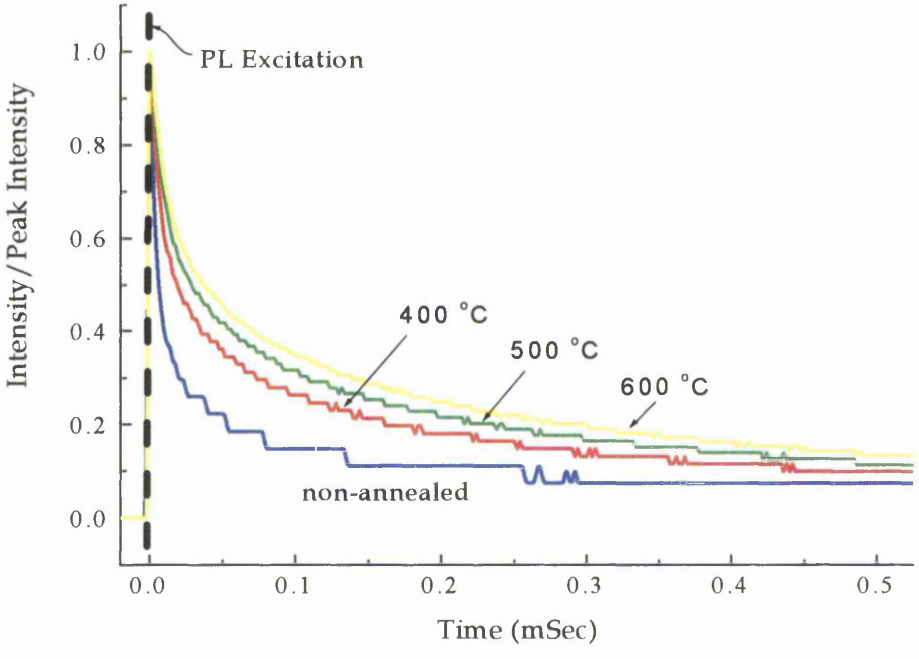


Figure 5.9 Normalised transient emission decay of PL from ZnS:Mn thin films grown on silicon at 200 °C and annealed at various temperatures.

The peak intensity of the PL spectrum for thin film ZnS:Mn samples as a function of the growth and anneal temperature are given in Figure 5.8. The figure clearly indicates that the brightest PL measurement occurs for samples fabricated at 200 °C. Therefore it is apparent that the better cubic crystals grown at this temperature has a part to play in the improved efficiency of the phosphor. However annealing the phosphor shows much more improvement in PL intensity, which is not all due to increase in crystalline quality concluded from structural analysis in the previous section. The following results and discussion will explain the factor governing the improvement in PL intensity.

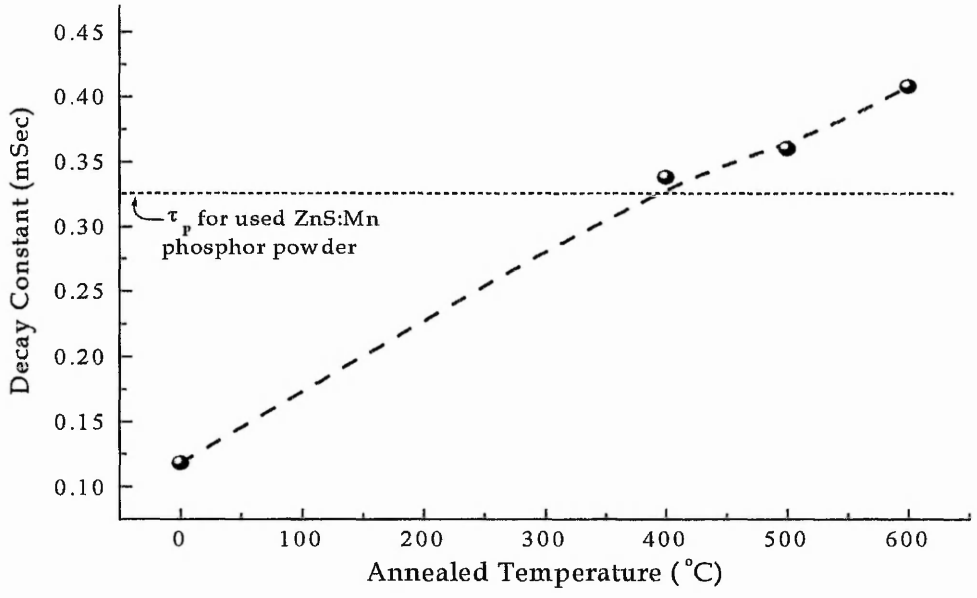


Figure 5.10 Transient PL decay constant for ZnS:Mn thin film as a function of sample anneal temperature. The short dashed line indicated the value of τ_p extracted for used ZnS:Mn phosphor powder.

By applying an excitation LASER pulse, the decay profile of the transient photoluminescence of ZnS:Mn thin films were obtained for samples annealed at various temperatures. A 10nm band pass filter, centred at 580nm is used to isolate the exponential PL decay relating to the peak wavelength alone from the superposition of multiple exponentials in the profile, as described in Section 2.4.3. The normalised transient photoluminescence for the various samples are shown in Figure 5.9.

Photoluminescence decay constant (τ_p) was extracted from these profiles[18] and plotted as a function of sample anneal temperature in Figure 5.10. It shows that the value τ_p increases linearly with annealing temperature. This means the after-glow period, when the excitation has ceased becomes longer when the samples are annealed at higher temperature. As this period is only a fraction of milliseconds, the after-glow by definition is fluorescence[19].

In Figure 5.10 a line is drawn across the graph to indicate the value obtained of fluorescence τ_p for used ZnS:Mn powder utilised in the target. Using this line as a reference, the non-annealed sample has a very short photoluminescence lifetime. However when the samples are annealed at 400 °C and above, τ_p becomes longer than for the material used to sputter grow the thin film. This observation will be discussed later. The longer decay times of the annealed thin film phosphor samples would appear brighter due to the persistence.

These samples were taken from quarters of the same wafer, which was grown at 200 °C from a ZnS:Mn target material with 0.43wt% of Mn concentration. Therefore the concentration of Mn atoms in these quartered samples would be expected to be the same as they are from the same substrate. However annealing the samples increased the PL luminance, which is thought to be by movements of the Mn ions to more favourable positions to become luminescent centres. It is likely that a large number of Mn sites are initially associated with heavily sputter-damaged portions of the lattice and therefore are not luminescent. Annealing reduces the number of these damaged regions and therefore enhances the number of luminescent centres. The increase in luminescent centres would have an additive effect thus increasing the PL intensity as observed.

It has also been shown previously that annealing increases the number of slow and fast decay centres and increases the decay time constant of the luminescence due to reduced probability of non-radiative recombination[20,21]. Therefore in a less efficient phosphor material, having a high density of non-radiative Mn sites, the luminescence decay would

be faster compared to a material having lower density of non-radiative sites. The reason is quantum-mechanical transfer of excitation energy within the dopant system, accelerating the decay by non-radiative processes[22]. Hence, with the increase in PL intensity and luminescence decay time after annealing the phosphor material, it may be inferred that more radiative sites could have been created from non-radiative sites.

The shorter τ_p measured for the target compared to the annealed thin film samples indicates that the powder material has a higher density of non-radiative sites. Therefore the effectiveness of the preparation method utilised by the phosphor manufacturer, which involves mixing of the ZnS compound and Mn followed by firing at a high temperature, is questionable !

5.4 Electrical Properties

5.4.1 Dielectric Constant

Relative dielectric constant (ε_r), was measured for thin film ZnS:Mn of 280 nm thick samples grown at various temperature on silicon substrates. The relationship between ε_r for non-annealed samples grown at different temperatures is shown in Figure 5.11. The values measured for these samples are slightly higher than reported elsewhere[23].

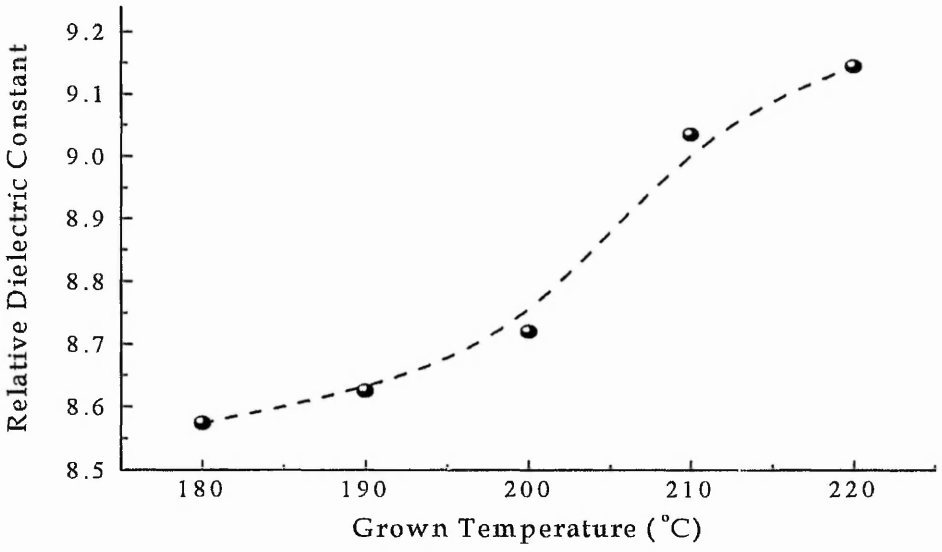


Figure 5.11 Dielectric constant of non-annealed 280 nm thick ZnS:Mn thin film grown on silicon substrate as a function of sample grown temperature.

A continuous increase in ε_r was measured with increase in sample growth temperature. The ε_r increased more drastically for samples grown at temperatures higher than 200 °C. Coincidently with the preference of structural and photoluminescence properties of sample grown at 200 °C, the ε_r value for this sample is also advantageously lower. This is because, in an ACTFEL device the phosphor layer should have ideally the lowest possible ε_r for maximum voltage drop across it, for the device to have the minimum threshold voltage. The ZnS:Mn thin film samples exhibited only a small variation in ε_r (±2.5%) for annealing temperatures between 400 and 600 °C.

5.4.2 *Electrical Stressing*

ZnS:Mn MIS diodes were electrically stressed below breakdown field and capacitance of the thin film was continuously measured during the stressing period. An increase in capacitance was measured for the first 200 minutes and then stabilisation was reached. The initial formation period for the MIS samples was observed to occur within 200 minutes ±10% time frame. In Figure 5.12 the measured capacitance in accumulation as a function of time when a ZnS:Mn diode was stressed at 0.5MV/cm with the Al electrode made negative is shown. However no change was observed when the diodes were stressed with the Al electrode made positive.

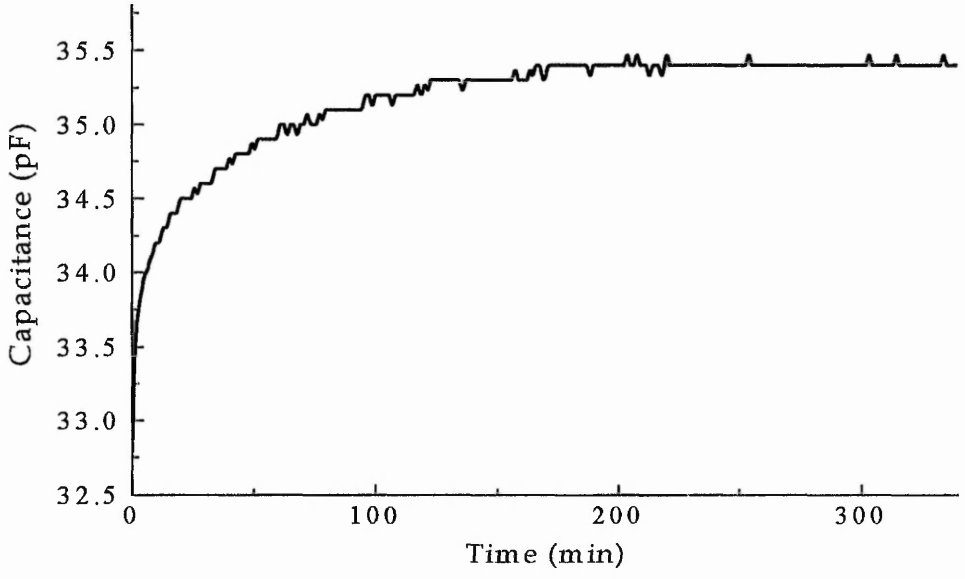


Figure 5.12 The increase in capacitance for ZnS:Mn thin film grown on silicon at 200 °C during an initial formation phase on the application of 0.5 MV/cm electric field across the diode is shown.

This increase is believed to be an effect of space charge modification in the bulk due to impact ionisation of vacancies present in the phosphor layer[24] or charge injection by field emission[25]. The most plausible reason here would be electron injection from the Al electrode, deduced from the polarity of the stressing voltage.

A hypothesis for the increase in capacitance can be explained as:

The injected electrons would neutralise possible existence of positively charged sulphur vacancies in this material (see Chapter 1, Sections 1.3.1 and 1.3.2). These vacancies in the bulk could behave as charge sheets. The existence of charge sheets will divide the bulk into a series of capacitors, hence lowering the net thin film capacitance is in a non-stressed diode. By neutralising these charge sheets the net thin film capacitance would increase.

A consequence of the increase in capacitance for the ZnS:Mn thin film layer when electrically stressed will have an effect on the electrical characteristics of the ACTFEL device during operation, which will be discussed in Chapter 6.

In this chapter, only the electrical parameters were investigated as a function of electrical stressing. On the other hand, the optical properties of ZnS:Mn thin film may also be altered. The EL efficiency relating to this subject is given in Chapter 6. Additionally, a measurement technique is proposed in Section 7.3.4 to investigate if any changes occur to the optical guiding property of this material due to stressing or on the application of high field.

5.4.3 *Breakdown and Leakage Current*

The characteristics of measured breakdown field strength and leakage current at 1MV/cm as a function of anneal temperature is shown in Figure 5.13. The breakdown field strength peaks at 400 °C in comparison to the other annealing temperatures. The breakdown measurement involves increasing the applied voltage across the diode till catastrophic current flows through. Therefore the measurement system is designed to be able to provide enough current required for thin film breakdown.

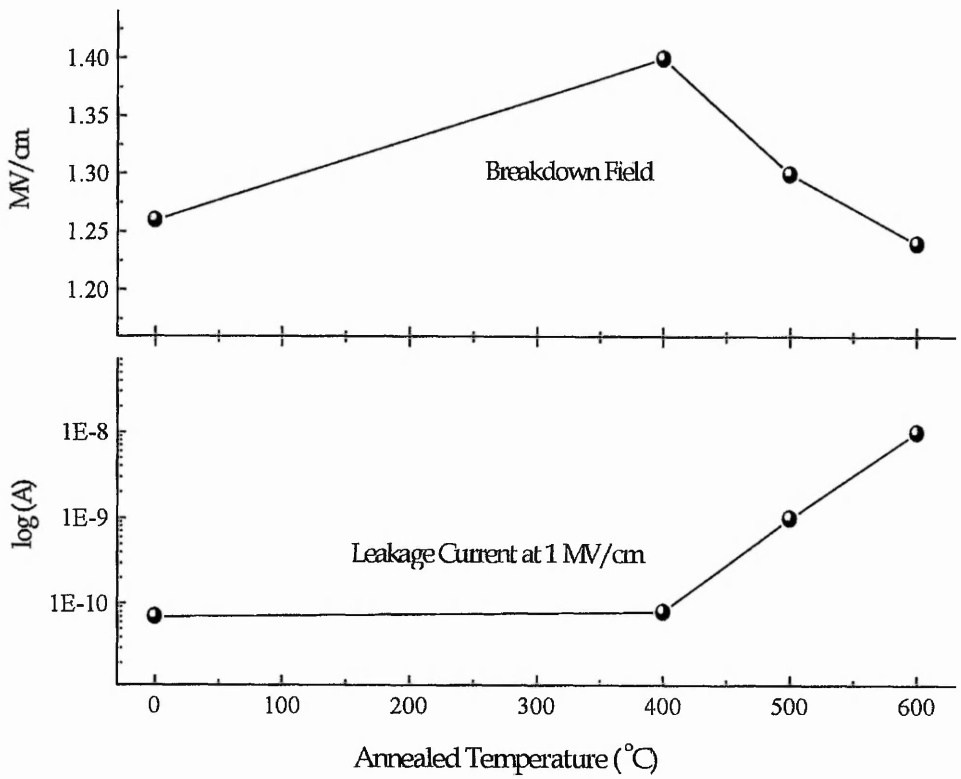


Figure 5.13 Characteristics of breakdown field strength and leakage current taken at 1MV/cm of applied electric field as a function of anneal temperature for 0.5 mm diameter thin film ZnS:Mn diode of 420 nm thick samples grown on silicon at 200 °C.

During the voltage ramp dark crater-like spots appears on the Al electrode surface, randomly. The rate of dark spot appearance increased with applied voltage. As more dots appear the current flowing through the device slowly increased. Importantly, the

appearance of dark spots increased with annealing temperature. Figure 5.14 shows picture of the dark spots of a broken down diode clearly indicating the eye of the craters.

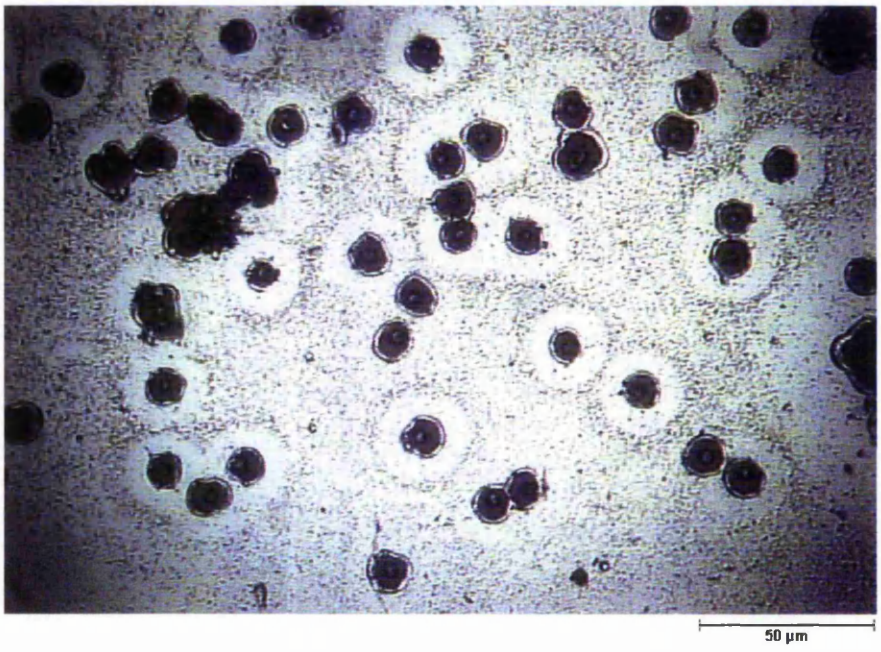


Figure 5.14 A multiple focussed and integrated picture of spots on ZnS:Mn thin film on silicon, broken down diode. The picture indicates that the eye of the crater leads to a deeper depth into the ZnS:Mn layer.

The observation possibly indicates that conducting channels were forming through the film. Therefore it seems likely that the ZnS:Mn films were breaking down locally[26,27]. This Localised Destructive Breakdown (LDB), leads to the destruction of a region of the sample. During LDB, current must rise locally to form a filament of high current density and was found that the LDB filament formation was likely to be triggered near the cathode[28]. This was consistent with the observation of a higher probability of spot occurring when the Al electrode was made negative with respect to the substrate.

It is believed that the preferred paths are caused by inhomogeneities in the phosphor layer and by irregularities at the interfaces that cause high field regions where electrons are preferentially emitted[29].

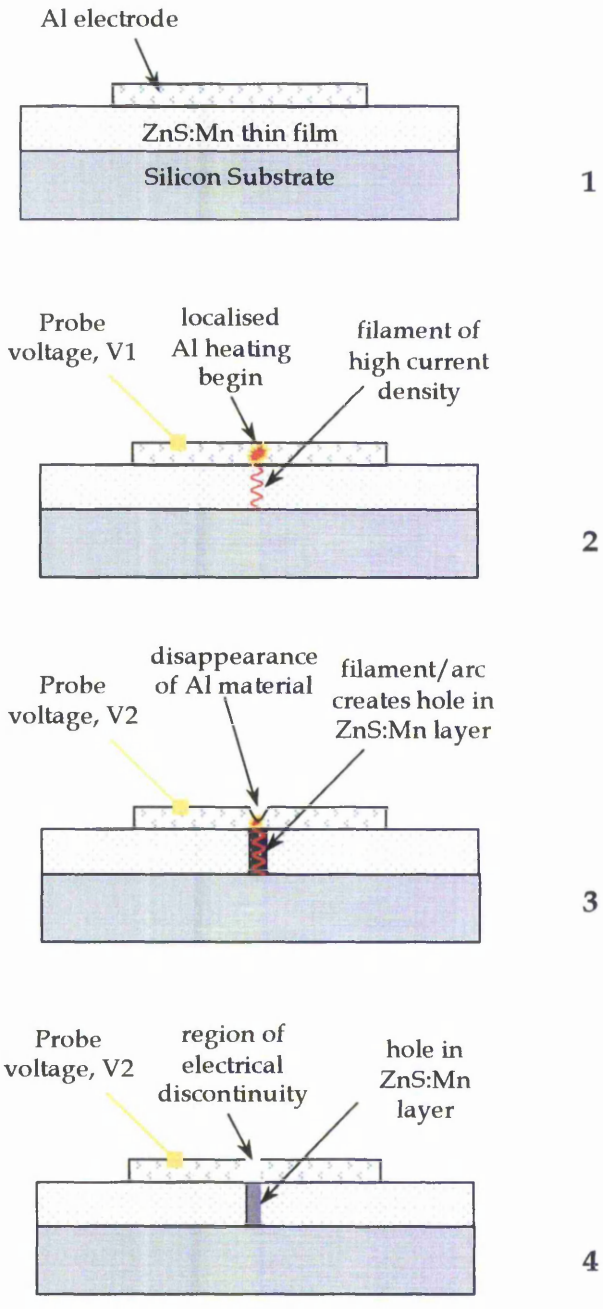


Figure 5.15 Illustrates the processes which creates LDB in ZnS:Mn thin film. *(1)* shows the diode structure. *(2)* shows that on the application of Voltage, V1 to the Al electrode, a hot spot appear in the ZnS:Mn layer causing the temperature of the Al material on the top region to raise. *(3)* shows that when the applied voltage is increased to V2, the current density increases hence enabling the filament to create a hole in the thin film and at this point the temperature is raised high enough to evaporate or melt the Al material. *(4)* shows a region of electrical discontinuity is created which cools down once again.

The LDB formation begins with current entering a region of thermal runaway due to applied field in excess of 1MV/cm. It has been estimated elsewhere, that this type of filament current density exceeds 1 A/cm^2, which elevates the local temperature due to Joule heating[28]. This is consistent with the observation of arcing in the active region. It is believed that the temperature on the surface is raised high enough to cause meltdown or evaporation of the Al. In the case where the temperature is only raised to melt the Al, the molten metal could flow into the hole created by the filament. Therefore, melting or evaporation would cause the electrode material to disappear away from the surface, resulting electrical contact with the region to be broken. This would cease current from flowing in the region. Hence the region cools down. These processes are believed to create the crater like structure. A model illustration of these events is given in Figure 5.15.

The use of Al for the top contact encourages self-healing in the event of a LDB, whereby electrical isolation may take place at the heat-affected zone[28]. However, such localised breakdown in this phosphor material has been found to reduce its electroluminescent efficiency[29]. This is because preferential electron path will excite and exhaust the Mn radiative sites along the route thus reducing the efficiency of the phosphor film.

The non-annealed and 400 °C annealed samples showed the lowest leakage current, which however increases at higher annealing temperatures as can be seen in Figure 5.13. Concomitant with lowest breakdown strength for samples annealed at 600 °C relative to the other samples, the samples also had the highest leakage current.

Charge Storage Capacity (CSC), for these thin film ZnS:Mn samples is approximately 1μC/cm^2.

5.5 Summary and Conclusions

The structural, photoluminescence and electrical properties of ZnS:Mn thin films were characterised as a function of growth and processing parameters. Good correlation between the structural and photoluminescence properties was found.

XRD measurement revealed that the ZnS:Mn powder material used in the sputtering target was made of pure crystals from the hexagonal phase only. However the ZnS:Mn thin film was made of polycrystalline, crystallites of predominantly cubic structure, with the preferred orientation of the (111) plane.

ZnS:Mn thin film samples grown directly on silicon (100) substrate had poorer crystalline properties, with only half the crystallites size compared to the ones grown on Y_2O_3 thin films. This demonstrates that Y_2O_3 thin film has better interfacial properties to produce ZnS:Mn phosphor of superior crystalline cubic structure.

Annealing ZnS:Mn thin film samples on silicon (100) substrate introduces some improvement in its crystallinity and increase in crystallite size, however, the improvement in crystallinity by means of thermal treatment was not as pronounced in ZnS:Mn thin film compared to Y_2O_3. The peak wavelength at 580 nm and FWHM of the PL spectrum did not change for sample annealed between 400 and 600 °C. In the contrary, PL intensity improved significantly with increase in annealing temperature. Also, a linear increase in radiative fluorescence decay constant, (τ_p) with annealing temperature was measured. These observations were used to demonstrate that annealing the phosphor produces more luminescent centres created from non-radiative sites.

On the other hand, the structural properties of ZnS:Mn grown on Y_2O_3 were highly sensitive to the temperature at which it was grown. It has been demonstrated that depositing this material at 200 °C substrate temperature produced the best crystallinity among all the temperature studied, for as deposited and annealed samples. This was

consistent with the brightest PL was found to be from samples grown at 200°C for all annealing temperatures studied. Therefore, the better cubic crystals grown at this temperature has a part to play in the improved efficiency of the phosphor. However annealing the samples showed much more improvement in PL intensity, which did not improve the crystalline quality a great deal. Hence, it is concluded that only by annealing the material, the true potential of the phosphor could be achieved

The ZnS:Mn thin film samples grown on silicon substrates exhibits a slight increase in dielectric constant with growth temperature. Samples grown at 200 °C and lower temperatures had a relatively low ε_r value. The reason for this variation in ε_r is unclear however could be related to the thin film structural properties. Moreover, annealing the samples between 400 and 600 °C did not vary ε_r, which is consistent with only a small variation in crystalline quality.

Electrically stressing ZnS:Mn MIS diodes at 0.5 MV/cm with Al electrode made negative increased the thin film capacitance within the first 200 minutes. After this formation period capacitance stabilised. The increase is believed to be an effect of positive space charge in the bulk being neutralised by electron injected from the Al electrode by high field emission. The existence of space charges in the bulk could be due to sulphur deficient ZnS:Mn thin film.

The primary cause for breakdown in ZnS:Mn thin film is due to LDB, which became prominent in samples annealed at higher temperatures. This is consistent with breakdown field strength being highest for samples annealed at 400 °C at 1.4MV/cm that reduces at higher annealing temperatures. The cause for the LDB is given as inhomogeneities in the phosphor layer and by irregularities at the interface where high field region encourages electrons to be preferentially be emitted.

Leakage current was lowest for non-annealed and 400 °C annealed samples, however increased drastically for higher annealing temperatures, which indicates a rise in conductivity. It is highly possible that some sulphur from the bulk material could be lost

due to heat treatment in vacuum, leaving behind sulphur vacancies. This type of vacancies would give rise to donor traps close to the conduction band edge acting as electron hoping centres, increasing the material conductivity[30].

The CSC for the ZnS:Mn thin films is measured to be $1\mu C/cm^2$, which would make a good engineering match with Y_2O_3 thin film CSC for design of ACTFEL devices[31].

Hence it is suggested that to produce high brightness ZnS:Mn thin film phosphor, the thin film has to be deposited at 200 °C substrate temperature and annealed at the highest possible temperature. However the conventional thermal treatment utilised for this study causes increase in LDB and leakage current at higher temperatures. Therefore the annealing temperature should be selected to comprise between device brightness and stability. The effects of the annealing temperature to the characteristics of ACTFEL device utilising ZnS:Mn thin film is presented in Chapter 6.

5.5 References

1 H.W. Leverenz, Introduction to Luminescence of Solids, Dover Publications, Inc. 1968

2 E. A. Mastio, M.R. Craven, W.M. Cranton, C.B. Thomas, M. Robino & E. Fogarassy, J. Appl. Phys., 86,5,1 1999 Pg. 2562

3 J.C. Jamieson & H.H. Demarest Jr., J. Phys. Chem Solids. 41 1980 Pg. 963

4 R.R. Reeber & G.W. Powell J. Appl. Phys., 38, 4 1967 Pg. 1531

5 S. Kiyota, K. Terai, N. Kikuchi, T. Kojima, N.S. Takahashi & S. Kurita, J. Vac. Sci. Tech A 8, 1 1990 Pg. 43

6 D. Adachi, S. Hasui, T. Toyama & H. Okamoto, Appl. Phys. Lett., 77, 9 2000 Pg. 1301

7 J.M. Blackmore & A.G. Cullis, Thin Solid Films 199, 1990 Pg. 321

8 T. Matsuoka, J. Kuwata, M. Nishikawa, Y. Fujita, T. Tohda & A. Abe Jap. J. Appl. Phys., 27, 4 1988 Pg. 592

9 T.H. Yeom, Y.H. Lee, T.S. Hahn & M.H. Oh, J. Appl. Phys. 79 1996 Pg. 1004

10 A.N. Krasnov, P.G. Hofstra & M.T. McCullough, J. Vac. Sci. Tech. A 18/2 2000 Pg. 671

11 Y.Nakanishi, Y. Fukuda, Y. Hatanaka & G. Shimaoka, Appl. Surface Sci. 48/49 1991 Pg. 297

12 R. Baserman, M.A. Nusimovici & M. Balkanski, Phys. Stat. Sol. 34 1969 Pg. 309

13 M. Zigone & K. Kunc, Proc. of Int. Conf. On Lattice Dynamics, 5/9 1977 Pg. 405

14 P.M. Alt, Proceedings of the SID, 25/2 1984

15 A.N. Krasnov, R.C. Bajcar & P.G. Hofstra, J. Vac. Sci. Tech. A 16/2 1997 Pg. 906

16 G. Blasse & B.C. Grabmaier, Luminescent Material, Springer-Verlag Berlin Heidelberg 1994

17 W. Chen, R.Sammynaiken, Y. Huang, J.O. Malm, R. Wallenberg & et al, J. Appl. Phys. 89,2 2000 Pg. 1120

18 R.C. Ropp, Luminescence and the Solid State, Elsevier 1991

19 S. Shionoya & W.M. Yen, Phosphor Handbook, CRC Press 1999

20 N.A Vlansenko, S.A. Zynio & Y.V. Kopytko, Phys. Stat. Sol., (a) 29 1975, Pg. 671

21 A.F. Cattell & A.G. Cullis, Thin Solid Films, 92 1982 Pg. 211

22 P. Benalloul, J. Benoit, R. Mach, G.O. Muller & G.U. Reinsperger, J. of Crystal Growth, 101 1990 Pg. 989

23 Y.A. Ono, Electroluminescent Displays, World Scientific Publishing, 1995

24 S. Shih, P.D. Keir & J.F. Wager, J. of Appl. Phys., 79/9 1995 Pg. 5775

25 A. Zeinert, C. Barthou, P. Benallou & J. Benoit, Proceedings of 8th Int. Workshop Inorganic and Organic Electroluminescence, 1996, Pg. 65

26 A.P.C. Jones, D.Y. Watts, A.W. Brinkman, J. of Crystal Growth 1986 Pg. 880

27 A.J. Simons, Ph.D. Thesis, University of Bradford 1991.

28 M. Beale, Philosophical Magazine B, 68, 5 1993 Pg. 573

29 S. Gupta, J.C. McClure, V.P. Singh, Thin Solid Films 299, 1997 Pg. 33

30 C. Tsakonas & C.B. Thomas, J. Appl. Phys., 78, 9 1995 Pg. 1

31 W.E Howard, IEEE Trans. on Electron Devices 1977 Pg. 903

CHAPTER 6

CHARACTERISTICS OF ACTFEL DEVICE

6.1 Introduction

The study of ACTFEL devices requires both the electrical and optical properties to be characterised. Based on the physics behind ACTFEL devices and the properties of the individual materials used for the construction of the structure, the important parameters for engineering the characteristics of an ACTFEL device can be summarised as follows:

(1) dielectric coupling of the phosphor and insulator layers
(2) nature of the interface charge states i.e. source of electrons
(3) crystalline quality of the phosphor layer which determines the carrier transport
(4) efficiency of the luminescent centres
(5) stability of the layers in the structure

This chapter details the observations made of ACTFEL devices characteristics during operation with different processing parameters. The devices were probed to facilitate electrical and luminance measurements. These measurements in combination with CCD and thermal imaging of the device surface were used to study the changes occurring to the device. The causes of observed changes were then investigated.

6.2 Experiment Results and Discussions

6.2.1 The Need for Annealing

ACTFEL samples were annealed at 400 °C in vacuum for different lengths of time. The normalised transient EL of these samples is shown in Figure 6.1. As expected, the EL decay becomes longer after the samples were annealed. This is an indication that the density of non-radiative sites has been reduced, and most likely more luminescent centres have been created as shown in Chapter 5. That is, the longer the decay constant, the better the phosphor efficiency[1]. This is consistent with the non-annealed samples having a peak EL luminance of less than 20% of the annealed samples peak luminance value. Additionally, the non-annealed samples were very susceptible to catastrophic breakdown at higher operating voltages. This is evidently due to the poorer quality of Y_2O_3 thin film in the as deposited condition, presented in Chapters 3.

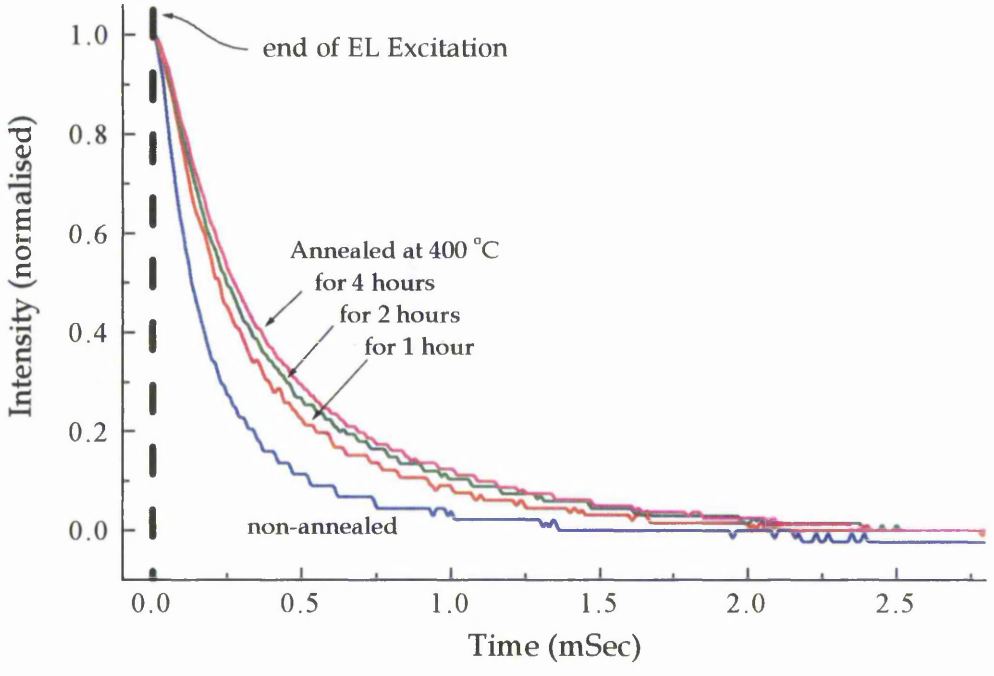


Figure 6.1 Normalised transient emission decay of EL from ACTFEL device for a non-annealed sample and samples annealed at 400 °C for various times.

However, no significant decrease in EL decay was measured for samples annealed for extended lengths of time as shown Figure 6.1.

On the other hand, the EL response to applied voltage was considerably altered for different annealing periods. The changes are shown in Figure 6.2. The threshold applied voltage for EL excitation became lower for longer annealing time. Additionally, the non-annealed sample has a very sharp EL response to applied voltage, which becomes softer with increase in annealing time. These changes are related to electron state distribution at the Y_2O_3/ZnS:Mn interface, which will be discussed in the following sections.

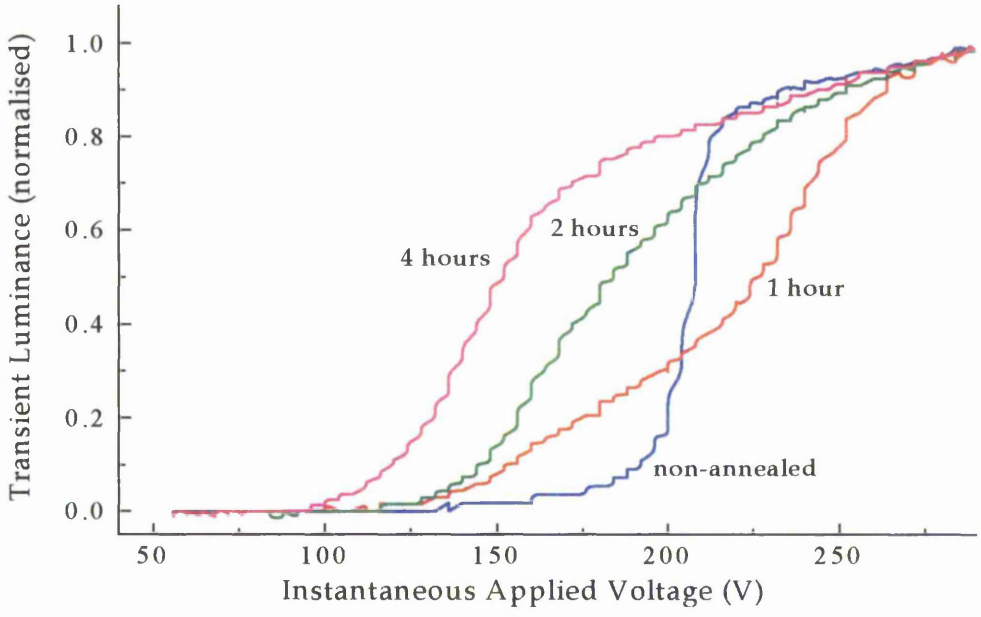


Figure 6.2 Normalised transient EL for ACTFEL device as a function of the instantaneous applied voltage from a non-annealed sample and samples annealed at 400 °C for different lengths of time. The devices were driven with 100 Hz, triangular wave signal.

6.2.2 *Effect of Annealing on Device Characteristics*

Measurements of EL Luminance as a function of applied Voltage (LV) was performed on ACTFEL devices annealed at various temperatures for 1 hour. The samples were of the edge emission type and luminance measurement was performed as described in Section 2.4.2. The measured LV curves for the samples are shown in Figure 6.3.

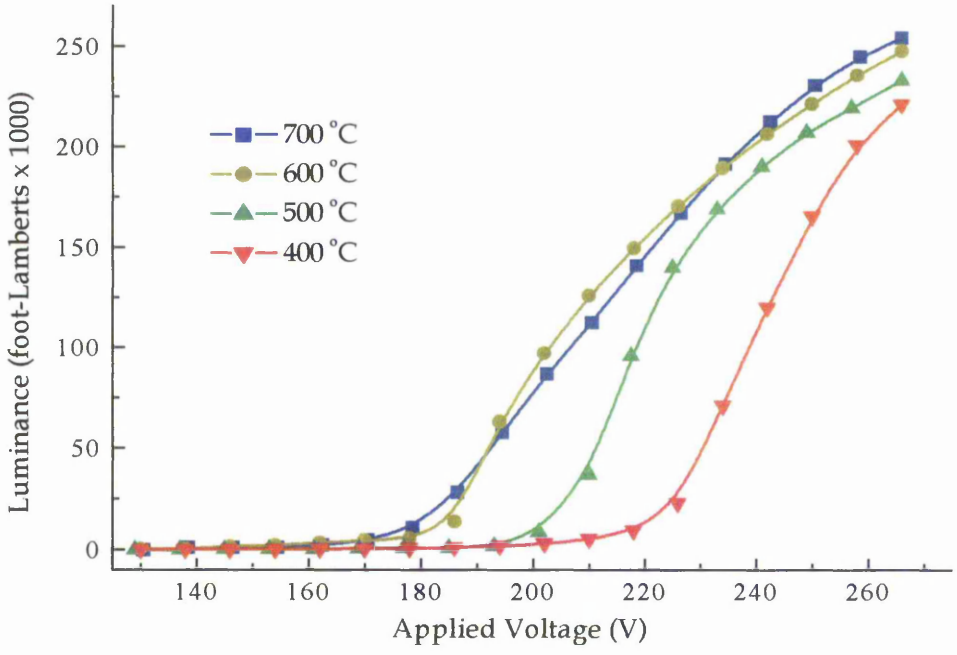


Figure 6.3 LV characteristics for ACTFEL edge-emission type for samples annealed at different temperatures. The devices were driven with 5 kHz sine wave signal.

A slight improvement in EL intensity with increase in annealing temperature was measured for the ACTFEL device. In addition, EL threshold voltage (V_{th}) decreases with annealing temperature, which has also been reported by many other groups[2,3]. The EL V_{th} of an ACTFEL is dependent on the electron state distribution in the area near the insulator-phosphor interface and the breakdown field of the phosphor[4]. A study was carried out on these samples to determine the influence of the two on V_{th}.

Breakdown field strength (E_{bd}) of a thin film phosphor layer is a measure of the non-reversible electrical breakdown due to catastrophic current flow through the layer. However in an ACTFEL device, the insulators will prevent excessive current to flow through the phosphor layer even at electric field much greater than E_{bd} across the phosphor layer. Consequently, in an ACTFEL device it is not a catastrophic breakdown but rather a temporary collapse of the phosphor layer capacitor during charge transfer from one interface to another at electric field higher than E_{bd}. Therefore, E_{bd} values of the phosphor layer may be correlated with the field across the phosphor layer at which EL occurs. As concluded in Chapter 5, E_{bd} of the ZnS:Mn phosphor layer has the highest value for samples annealed at 400 °C and reduces at higher annealing temperatures as shown in Figure 6.4.

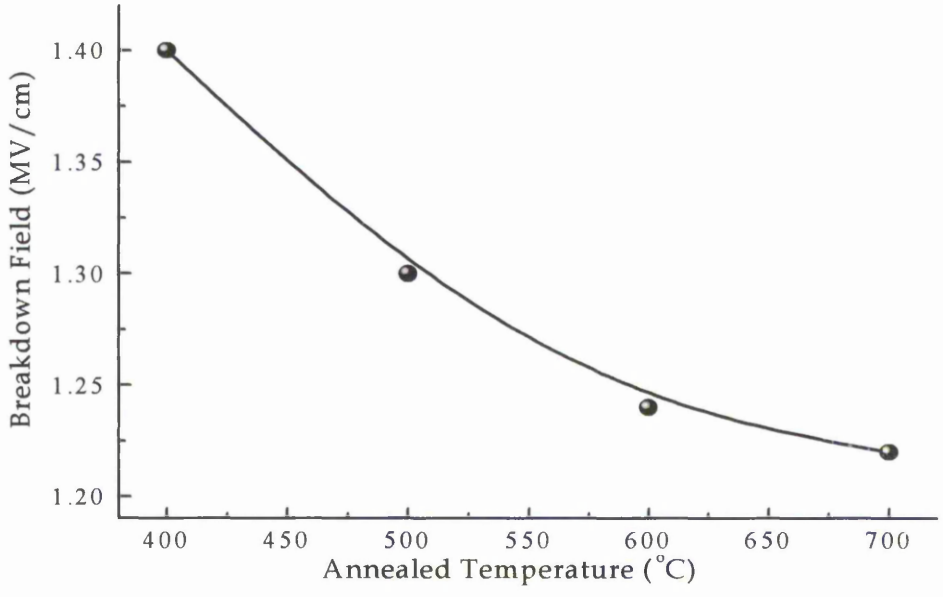


Figure 6.4 Measured breakdown field strength for ZnS:Mn thin film MIS diode as a function of sample annealed temperature.

In order to facilitate the association between E_{bd} and the phosphor layer threshold field (E_{th}) at which EL emission occurs, the voltage axis from Figure 6.3 has to be converted to an equivalent field across the phosphor layer.

The peak phosphor field (F_P) for a given applied voltage is expressed as

$$F_P = \alpha \times \frac{V_{TFEL}}{d_p} \qquad \text{Eq. 6.1}$$

where V_{TFEL} is the peak-voltage applied across the ACTFEL device presented in Section 2.3.2, d_P is the phosphor layer thickness and α is the factor that describes the ratio of the voltage drop across the phosphor layer to the applied device voltage given as[5]

$$\alpha = \frac{C_i}{C_i + C_p} \qquad \text{Eq. 6.2}$$

C_i and C_P are the insulator layers (top and bottom) and phosphor layer capacitances. These values may be determined by differentiating Eq. 2.2 with respect to the instantaneous applied voltage across the device[6]. Hence ACTFEL device capacitance as a function of applied voltage is obtained as shown in Figure 6.5.

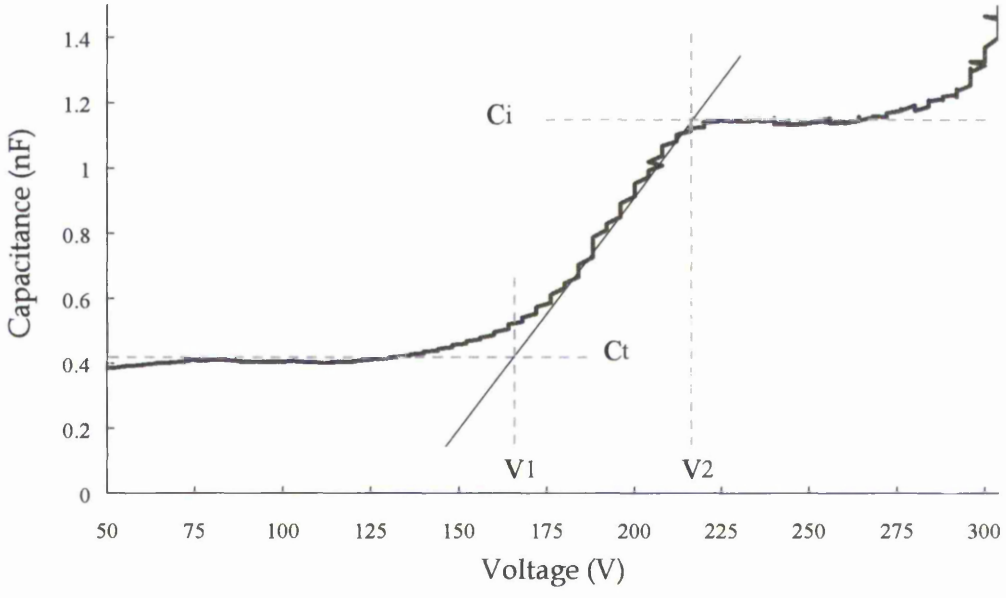


Figure 6.5 Shows a CV curve for an ACTFEL device indicating the plateau at which insulator and total device capacitance values can be obtained.

The CV curve has two plateaus, corresponding to the insulator capacitance, C_i and total device capacitance (C_t). The voltage labelled V1 corresponds to the onset of carrier conduction and V2 to the saturation point of the turn-on period for the ACTFEL device[7,8]. The value of C_P is calculated from C_t and C_i by the relation given by Eq. 6.3.

$$\frac{1}{C_t} = \frac{1}{C_i} + \frac{1}{C_P} \qquad \text{Eq. 6.3}$$

The factor α was calculated from the values of C_i and C_P measured for all the samples. It was found that α was increasing with device annealing temperature. This was due to a combination of increase in C_i and decrease in C_P. Therefore this factor must be taken into account to calculate F_P for individual samples, rather than using the standard relative dielectric constant (ε_r) of the thin films to eliminate the effect of variation in α to the calculated F_P. Utilising Eq. 6.1 to calculate F_P, the LV curves from Figure 6.3 are plotted on a normalised luminance ($L/L_{(F_P=2.1\,MV/cm)}$) versus F_P graph as shown in Figure 6.6.

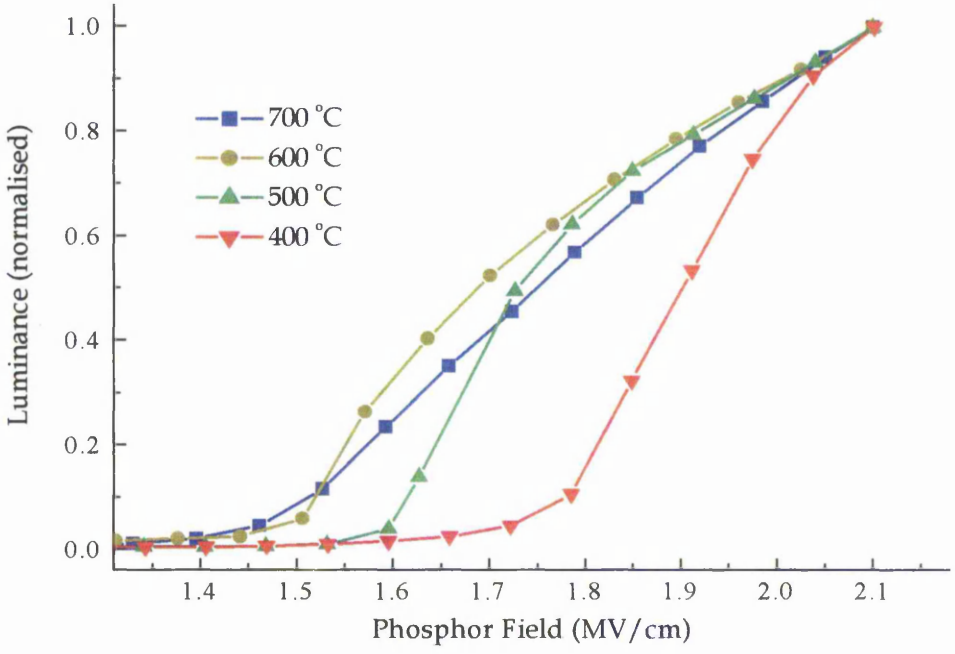


Figure 6.6 Normalised luminance [$L(F_P = 2.1$ MV/cm) = 1] versus phosphor field for ACTFEL devices annealed at different temperatures.

The phosphor field threshold, E_{th} for EL emission to occur (1% of peak intensity) decreases with annealing temperature as shown in Figure 6.6, which has also been seen elsewhere[2]. This is consistent with the reduction of the E_{bd} for ZnS:Mn thin films with increase in annealing temperature. However the effective values of E_{th} for EL are slightly higher than E_{bd}, as can be compared between Figures 6.4 and 6.6. Additionally, the luminance response to the applied field became softer with annealing temperature. These observations will be discussed later.

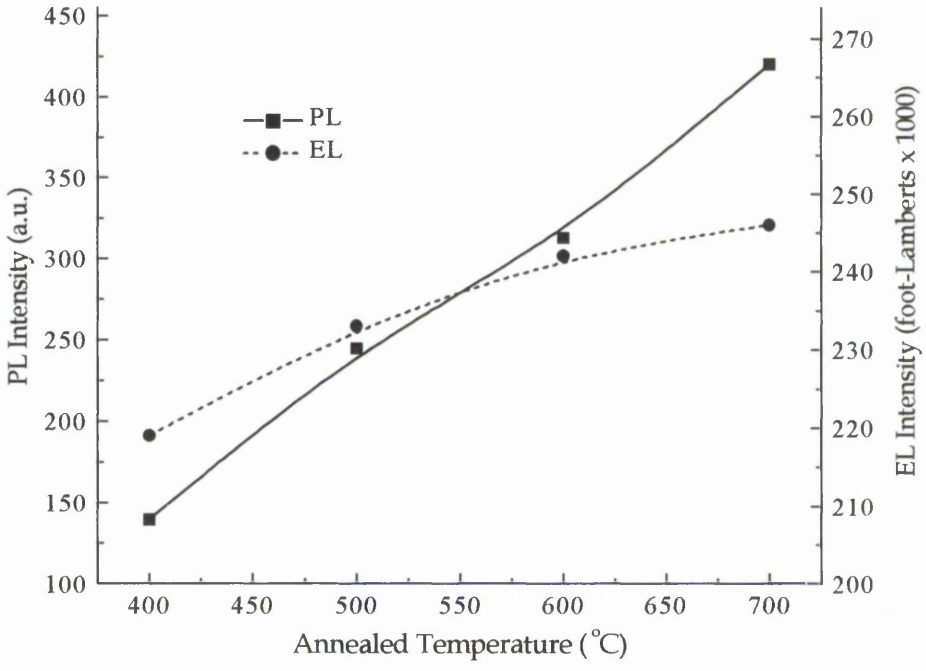


Figure 6.7 A summary of the peak intensity of ZnS:Mn thin film and EL luminance of ACTFEL device at FP = 2.1 MV/cm as a function of annealing temperature.

The ZnS:Mn thin films exhibited an increase in PL intensity with annealing temperature as presented in Chapter 5. However EL intensity of the ACTFEL devices only show a slight improvement with annealing temperature and saturate for treatment higher than 600 °C. Similar results have been seen before[2,9]. A summary of the measured PL and EL intensities are shown in Figure 6.7.

The increase in PL intensity with annealing temperature indicates improvement in the phosphor efficiency, as discussed in Chapter 5. However the saturation in EL intensity for higher annealing temperatures is probably related to a decrease in the number of electrons tunneling out of the interface states, which is the major source of charge in this device for EL to occur. CV analysis is used to quantitatively elucidate this argument.

In order to investigate the interface charge properties the Davison et al[10] technique was used. The method relies on the CV slope of an ACTFEL device during turn-on. Quantitatively the pre-clamping interface state charge (Q_{int}) may be assessed as

$$Q_{int} = \frac{C_i^2}{2}\frac{C_t}{C_P}\left[\frac{\Delta C}{\Delta V}\right]^{-1} \qquad \text{Eq. 6.4}$$

The term in the square bracket is the slope of the CV transition, where $\Delta C = C_i - C_t$ and $\Delta V = V2 - V1$ in relation to Figure 6.5. The calculated values of Q_{int} for different annealing temperatures are given in Table 6.1.

Annealed Temp. (°C)	Q_{int} (coulomb x 10^{-9})
400	36.1
500	34.5
600	32.4
700	30.3

Table 6.1 Details a summary of the calculated pre-clamping interface state charge from measured CV data for ACTFEL device annealed at different temperatures with active area of 0.083 cm^2.

The Q_{int} value of the ACTFEL device reduces with annealing temperature. This explains the saturation in EL, which is due to a combined effect of increase in phosphor efficiency and reduction in Q_{int} of the ACTFEL device with annealing temperature. Similar reduction as in Q_{int} between the insulator and phosphor interface was also measured in the density of interface states between Y_2O_3 and silicon interface with increase in annealing temperature, presented in Chapter 4. However, work done previously has

shown that the lattice misfit between the ZnS:Mn/Y_2O_3 multi-layers becomes bigger after increasing the annealing temperature[11]. Therefore the decrease in Q_{int} is probably not because of improvement in the crystal quality at the interface and may well be attributed to other reasons. A potential reasoning is given below.

In an idealisation of a real ACTFEL device, the interface state density is negligible from the phosphor conduction band minimum to a point approximately 1eV below the conduction band minimum where the density increases abruptly[12,13,14]. The energy depth from the conduction band minimum of which this point occurs in a real device is related to the phosphor field[15,16] at which electron tunneling occurs. *Cranton* has proposed that with increase in annealing temperature the density of interface states at the phosphor-insulator interface behaves less like a heavily populated discrete state, and more like a finite continuum[9]. The model also says that the energy depth from the conduction band minimum at which tunneling begins to occur moves closer to the conduction band, such that tunneling occurs at lower applied field for higher annealing temperatures. The observations made during this work substantiate the proposed model.

With the decrease in E_{th} and the decrease Q_{int} with annealing temperature, it can be deduced that large interface states, which exist at deeper energy levels, are suppressed. This has been demonstrated to also occur on Y_2O_3/Si interface states, presented in Chapter 4. Hence shallower states become dominant when the device is thermally annealed. This would explain the softening of luminance versus F_P slopes for higher annealing temperatures, as shown in Figure 6.6.

Assuming that the primary source of energetic electron are generated from interface states and by considering the Luminance versus Phosphor Field curves for the ACTFEL samples annealed at different temperatures, a possible emission current density profile as a function of phosphor field for samples annealed at lower and higher temperatures is given in Figure 6.8. The model illustrates that electron emission from interface states begins at much lower phosphor field with a softer response as the samples are annealed at higher temperature.

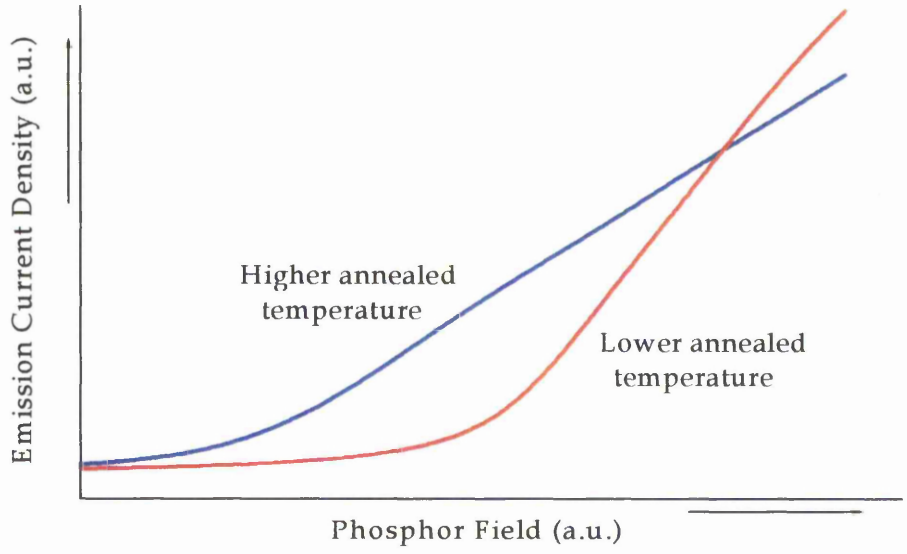


Figure 6.8 A possible emission current density profile from the ZnS:Mn/Y_2O_3 interface as a function of phosphor field for ACTFEL samples annealed at lower (400 °C) and higher (700 °C) temperatures. It indicates that electron emission from interface states begins at much lower phosphor field with a softer response as the samples are annealed at higher temperature.

6.2.3 *Electro-Optical Ageing Behaviour*

6.2.3.1 Vacuum Environment

ACTFEL devices were aged and electro-optical measurements were performed in a vacuum below 0.2 x 10^{-3} mbar. This experiment was performed in vacuum to minimise environmental effects on the performance of the device, hence the effects of electrical stressing alone could be studied. The devices were kept at a peak V_{TFEL} voltage corresponding to F_P = 2.1 MV/cm, according to the different measured α for different annealed temperature.

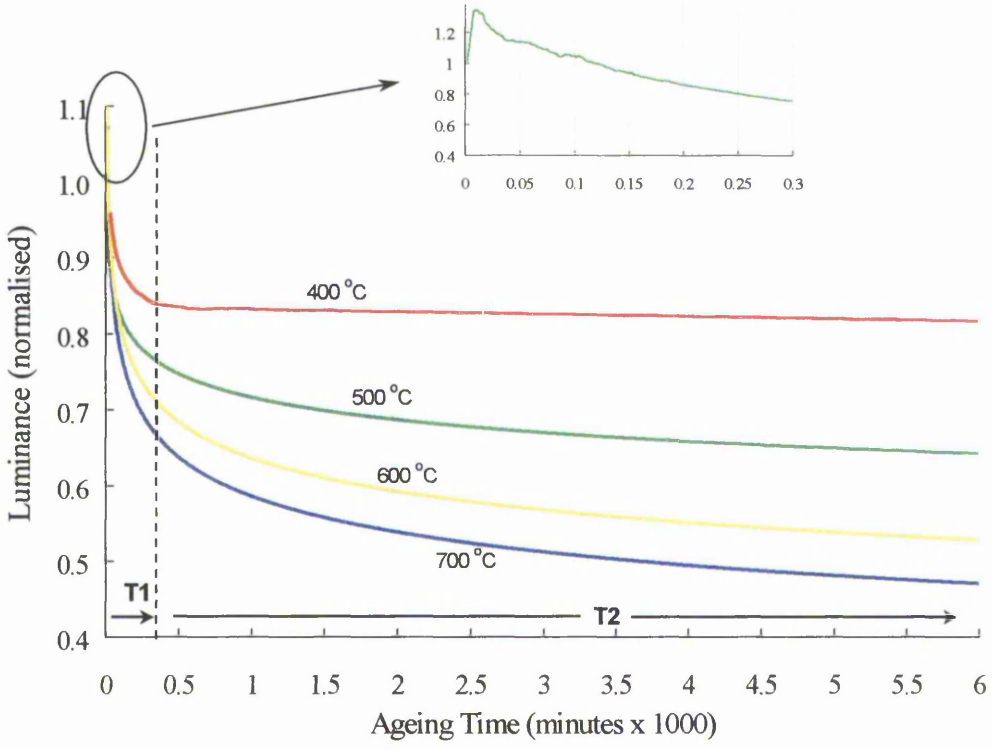


Figure 6.9 Normalised luminance as a function of operation time in vacuum below 0.2x10^{-3} mbar for ACTFEL devices annealed at different temperatures. Each profile is an average of three edge-emitter devices. Smoothing of the curves was performed by averaging the data points by 5, which is approximately 10 minutes. The inset shows the luminance profile of an ACTFEL device annealed at 500 °C during the first 300 minutes of operation.

The devices were operated at different drive frequencies, and it was found that the operating frequency has a strong influence on the ageing characteristic whereby the

higher the frequency the more rapid the device degrades. This was a result of fatigue effect in the device due to the number of operation cycles within a given time. However for this study all the devices were operated with a standard 5 kHz sine wave signal.

In Figure 6.9, EL luminance characteristics as a function of operation time for ACTFEL devices annealed at different temperatures are shown. It was found that samples annealed at 400 °C stabilised in the shortest time and showed the least luminance degradation over time. Whereas the devices annealed at the other temperatures continuously degraded in EL luminance, with the device annealed at higher temperature degrading more. However an initial rapid decrease in luminance could be observed in all the samples, marked as T1 and a gradual decrease in brightness period marked as T2 in Figure 6.9. It was found that the luminance decay profile in the T1 region constitutes multiple exponential functions. The dominant contributing factors in the two regions were investigated and the findings are discussed below.

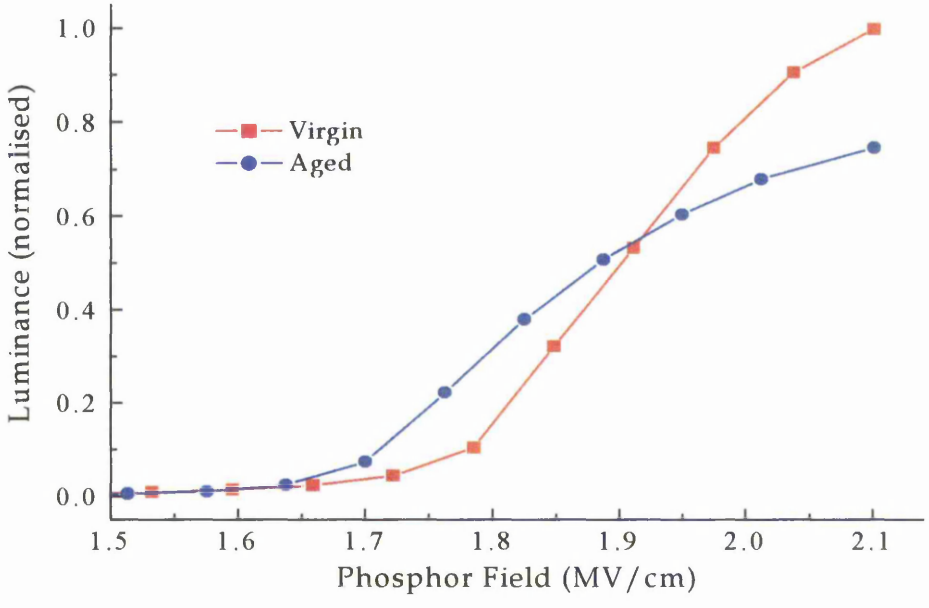


Figure 6.10 Luminance (normalised to initial value in the virgin state) as a function of F_P of an ACTFEL device annealed at 400 °C in its virgin and aged state. The device was aged in vacuum below 0.2 x 10^{-3} mbar with 5 kHz sine wave at 280 V peak voltage for 200 hours.

In Figure 6.10, luminance as a function of phosphor field characteristics for an ACTFEL device in its virgin state and after ageing in vacuum for 200 hours is shown. The device was annealed at 400 °C. It is to be noted that α decreased for the aged sample, and the new value was used to calculate F_P. The aged luminance versus F_P curve shows an increase in EL intensity at fields lower than 1.9 MV/cm and the luminance intensity becomes lower at higher fields in comparison to its virgin state. The increase in EL intensity at lower field indicates that more electrons are injected from shallower interface states as ageing progresses. This is consistent with the softening of the measured CV slope for the aged device at the turn on region[17], as shown in Figure 6.11.

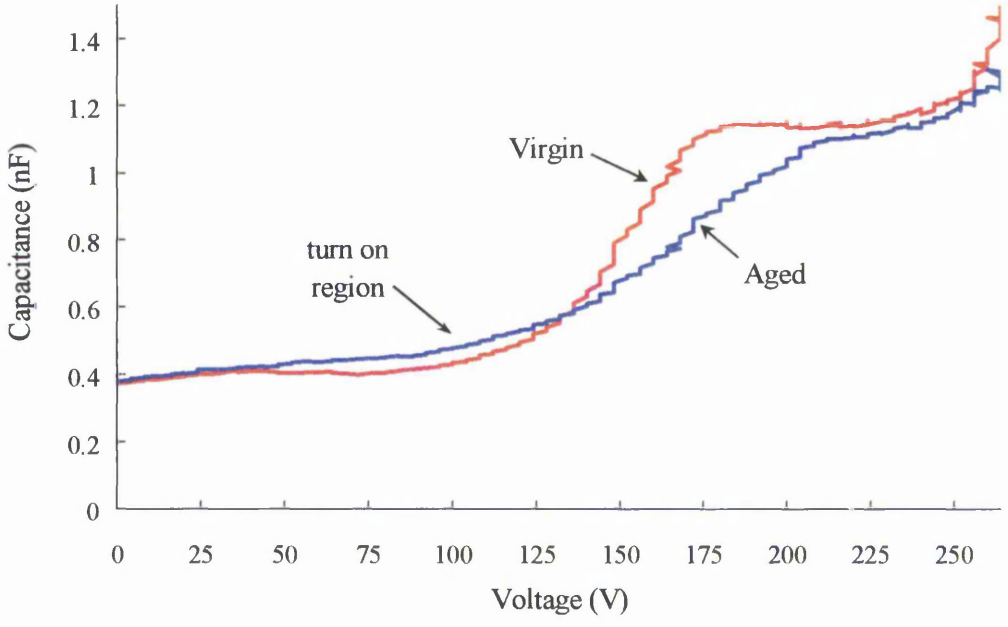


Figure 6.11 CV curves for an ACTFEL device during its virgin state and after ageing.

A plausible explanation for this could be the creation of more shallower interface trap states[18] due to impact of high energetic electron at the insulator-phosphor interface causing structural damage. High current density filaments within the ZnS:Mn layer (Chapter 5) could create sufficient energetic electrons for this to occur. The creation of shallow interface states is believed to take place in the first few minutes when the device is first turned on. This would explain a slight increase in device brightness initially, as

shown in the inset diagram of Figure 6.9. Therefore, these new shallow states should be deep enough for hot electrons to be generated, which is required for EL excitation.

Further evidence to support the argument that the creation of shallow interface states occurs due to ageing is given by the broadening in the transient EL luminance of an aged device for the same applied voltage as shown in Figure 6.12. It can be seen that for the aged device, EL light is observed at lower applied voltage than in its virgin state. The shifting in the peak luminance point to a lower voltage is due to a decrease in factor α. In an α compensated graph the peaks would fall at a point closer in time and voltage scale.

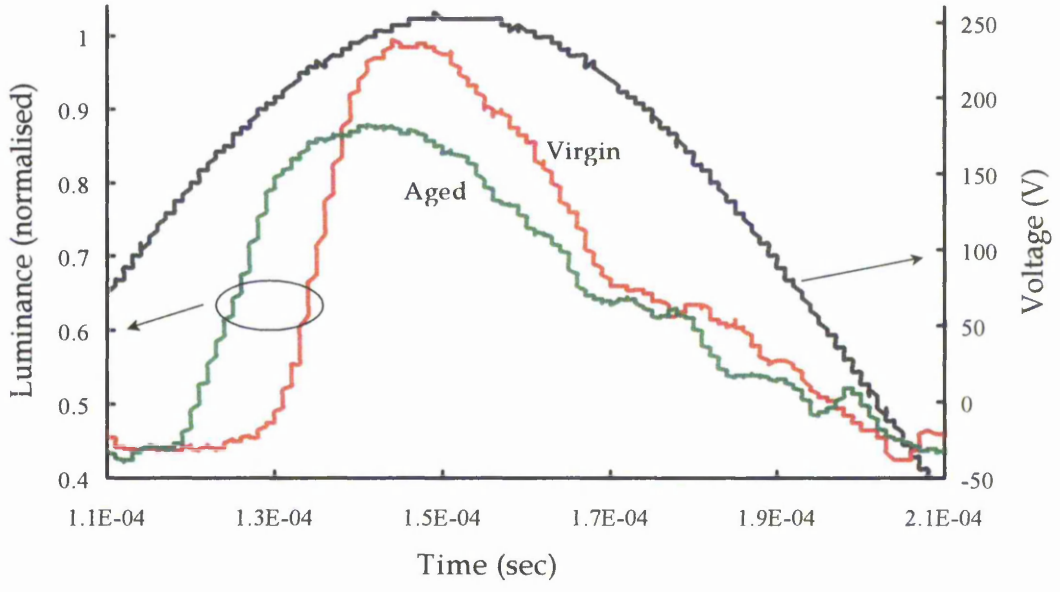


Figure 6.12 Transient EL luminance response to applied device voltage for an ACTFEL device in its virgin state and after ageing in vacuum for 200 hours.

Concomitantly, the bombardment of high energetic electrons at the interface and the non-radiative process during device operation would generate heat within the device. Additionally, during the re-trapping process of hot electrons at the anode interface, a significant amount of thermal heat must be dissipated for it to reach the bottom of the conduction band[19]. The rise in device temperature was observed using the Infrared Microscope system described in Section 2.4.4. In Figure 6.13 thermal images of an ACTFEL device surface in its off and fully turned on conditions are shown.

The figure below clearly shows a small measurable rise in surface temperature. However it is believed that the core temperature of the active region could rise to a significant temperature sufficient for self-annealing to take place. The reason for only measuring a small change in temperature on the surface could be due to heat transferring away from the surface via the metallic electrode by thermal convection to ambient. Also technical issues relating to the emissivity of the surface and poor thermal contact between the device surface and the black paint utilised to improve the emissivity could have affected the measurement.

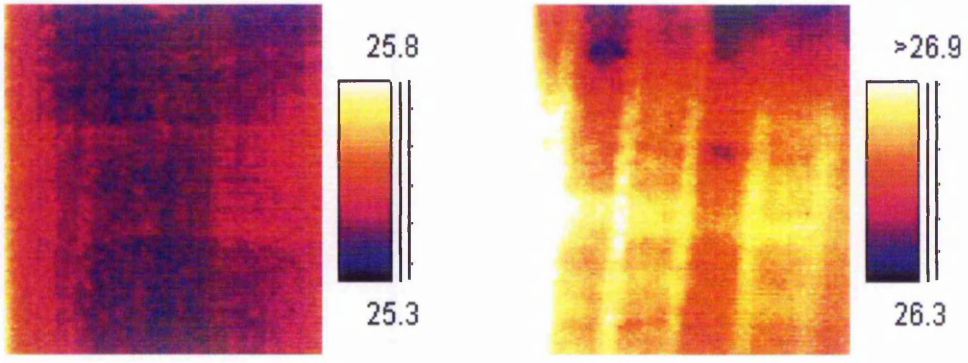


Figure 6.13 Thermal images of an ACTFEL device surface in the off (left) and fully on (right) conditions. The stripes visible in the right picture are the active region. The picture of the device in the on state indicates a measurable rise in surface temperature in comparison to its off state. Values given are in degree Celsius.

The self-annealing process would cause a redistribution of electron charge at the interface, which effectively will reduce the density of states at deep energy levels as discussed in the previous section. This was consistent with a decrease in Q_{int} value by approximately 6%, which took place within the first few hundred minutes of ageing and no further change was measured afterwards. This decrease is a contributing factor to the lower luminance measured at higher fields.

The increase in the number of Localised Destructive Breakdown (LDB) events for ZnS:Mn thin film annealed at high temperatures (Chapter 5) is believed to also have a part to play in the more substantial reduction in EL luminance for devices annealed at

higher temperatures. This is because preferential current paths and reduction in active area associated with LDB would simply reduce the device efficiency. It is reasonable to assume that this process will take place primarily during the initial phase of operation for the same applied voltage. Therefore the reduction in Q_{int} and LDB in the ZnS:Mn thin film that is more prominent at higher anneal temperatures are believed to account for the rapid luminance decrease region, T1 in Figure 6.9.

After the T1 region, it was found that the samples annealed at 500, 600 and 700 °C showed a gradual decrease in α, which was due to the increase in phosphor layer capacitance. As mentioned previously, α determines the field across the phosphor layer. A decrease in α would reduce the phosphor field for a same applied voltage. In Figure 6.14, these variations with operation time for an ACTFEL device annealed at 600 °C are shown. However for the device annealed at 400 °C, the decrease in α was very small.

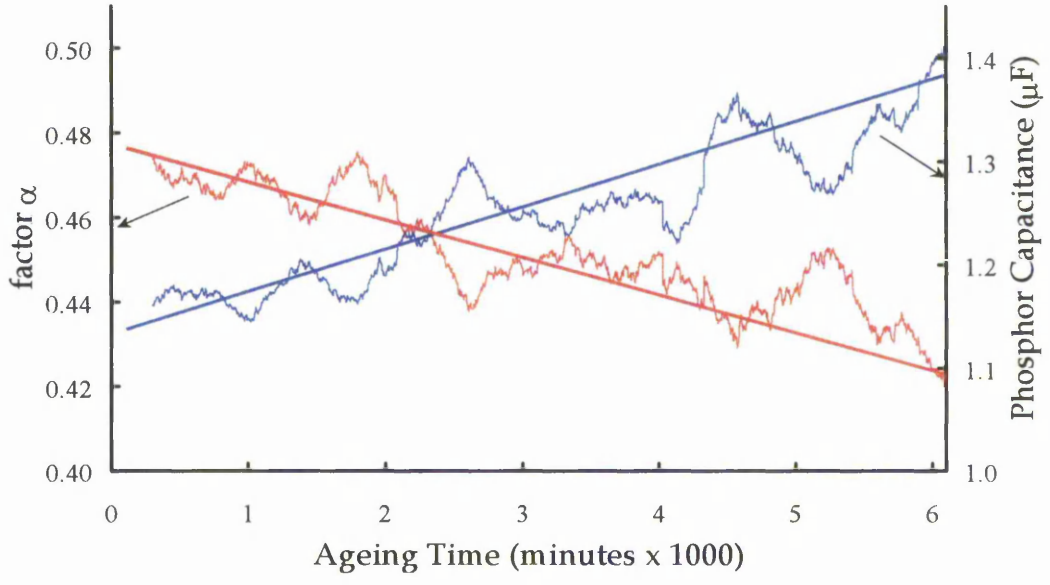


Figure 6.14 Shows the increase in phosphor capacitance, C_P hence reducing the factor α. The data corresponds to an ACTFEL device annealed at 600 °C. The measurement has a noticeable noise level, however a trend line is drawn to indicate the increase in C_P and reduction in α with device operation time.

These variations are related to the increase in phosphor layer capacitance due to electric field stressing, as discussed in Section 5.4.2. It is concluded in Chapter 5 that the increase

in ZnS:Mn thin film capacitance is due to positive space charge neutralisation by injected electrons. In a MIS structure, the amount of electrons available for this process to take place is only limited by the ZnS:Mn thin film leakage current. However, in an ACTFEL device, the insulating layers would also limit the current flowing through the structure. Therefore, in the ACTFEL device the neutralisation process of the space charges would require a longer excitation time to compensate for the limited electrons available in each cycle. This would explain the gradual increase in ZnS:Mn thin film layer capacitance of an ACTFEL device in comparison to the faster increase in capacitance in a MIS structure, which occurred within the first 200 minutes.

Also shown in Chapter 5, the leakage current of the ZnS:Mn thin film significantly increased when annealed above 400 °C, which is believed to be due to increase in sulphur vacancies (Chapter 5), contributing to material capacitance instability. This is consistent with the relatively small change in phosphor capacitance for device annealed at 400 °C as a function of device ageing time. This also explains the higher luminance degradation observed with increase in device anneal temperature in the T2 region of Figure 6.9.

In line with the change in α, the tunneling current was affected. The tunneling current (I_T) is the injection of charge from the interface states at above threshold field, E_{th}. The I_T of the ACTFEL device may be found from the expression below

$$I_{ext} = I_{dis} + \alpha I_T \qquad \text{Eq. 6.5}$$

where I_{ext} is the external measured current during device operation and I_{dis} is the current induced by the device capacitance responding to external applied voltage. However to facilitate the measurement Eq. 6.5 is rewritten as given in Eq. 6.6

$$I_T = \frac{1}{\alpha}\left[\frac{dQ_{ext}}{dt} - C_t\left(\frac{dV_{TFEL}}{dt}\right)\right] \qquad \text{Eq. 6.6}$$

where Q_{ext} is the instantaneous external charge measured to applied device voltage, V_{TFEL}. Q_{ext} is equivalent to the charge described by Eq. 2.2.

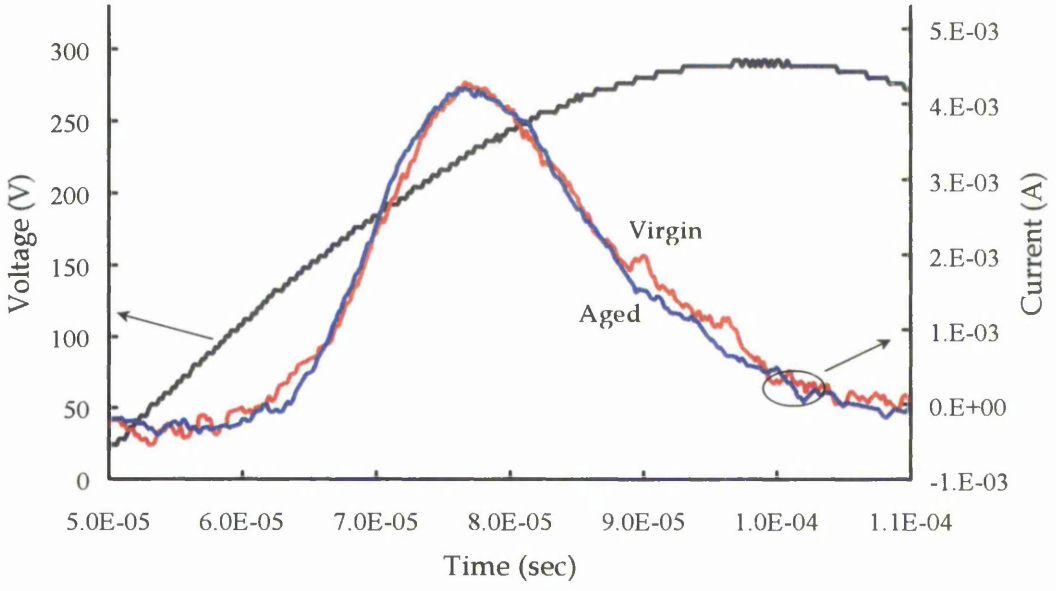


Figure 6.15 Tunneling currents response to applied voltage for an ACTFEL device annealed at 400 °C in its virgin and aged for 200 hours in vacuum.

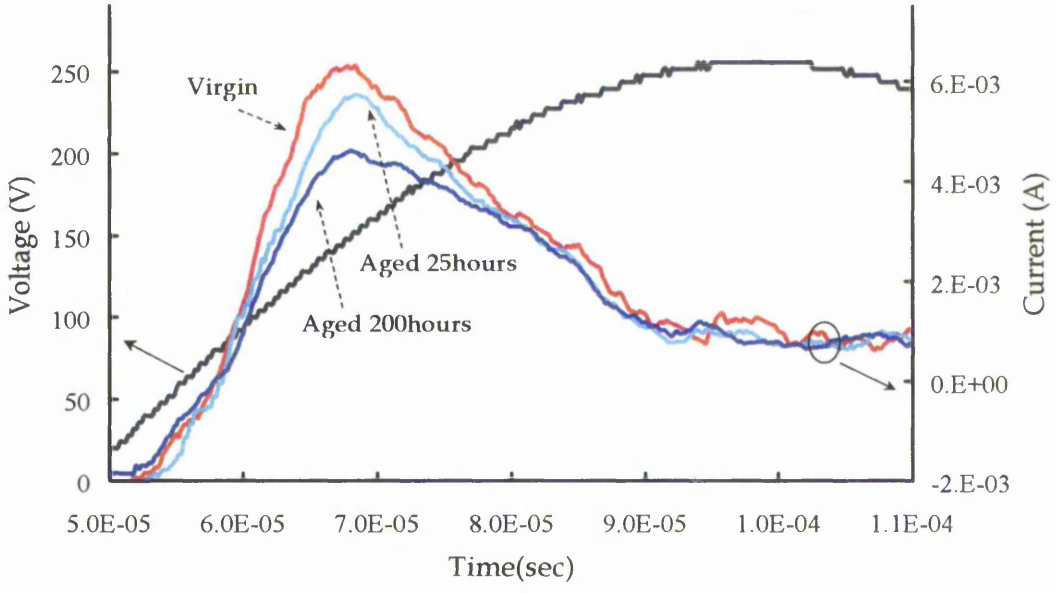


Figure 6.16 Tunneling currents response to applied voltage for an ACTFEL device annealed at 600 °C in its virgin, aged for 25 and 200 hours in vacuum.

I_T for the device annealed at 400 °C only showed a negligible reduction after ageing the device for 200 hours in vacuum as shown in Figure 6.15. However for the other annealing temperatures studied, I_T continuously reduced in response to the decrease in α. These changes are shown in Figure 6.16, where an ACTFEL device annealed at 600 °C showed a decrease in I_T with ageing time. I_T reduces because for the same applied voltage, the field across the phosphor layer has been reduced. As the phosphor field reduces with ageing time, the total number of electrons emitted into the active layer reduces. This statement could be inferred from the emission current density model given in Figure 6.8. The gradual luminance degradation trend of the ACTFEL sample annealed at higher temperature is comparable to the predicted emission current density profile as a function of variation in phosphor field. This strengthens the reasons discussed above for the continuous decrease in EL luminance measured for devices annealed at 500, 600 and 700 °C in the T2 region.

Hence, it may be concluded that the additive effects of decrease in Q_{int} and α along with LDB in the ZnS:Mn thin film were the main reasons for the lowering in EL luminance during device operation in vacuum.

6.2.3.2 Ambient Environment

ACTFEL devices were also operated in a normal ambient environment instead of in vacuum. In Figure 6.17, the luminance profile for two devices operated in normal ambient and one device operated in vacuum below 0.2 x 10^{-3} mbar as a function of ageing time is shown. The samples were of devices annealed at 400 °C, as it is the most stable in vacuum, discussed in previous section. The device in air degraded more rapidly than when operated in vacuum. Samples annealed at the other temperatures also exhibited rapid degradation behaviour when operated in ambient condition. However the device annealed at higher temperatures had much higher luminance loss with ageing time, similar to the vacuum condition.

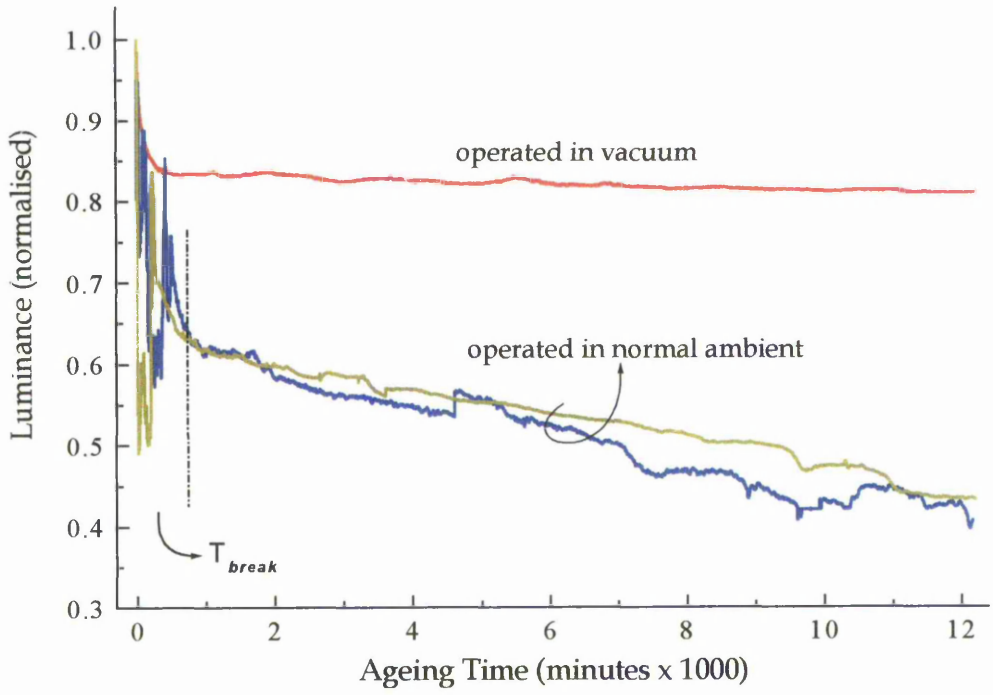


Figure 6.17 Normalised EL luminance as a function of operation time for ACTFEL device annealed at 400 °C. Two devices operated in normal ambient and one device operated in vacuum below 0.2x10^{-3} mbar is plotted. No smoothing was performed on the profiles.

Two devices operated in air are shown in the above figure to illustrate that the EL luminance degradation with time had some aspects of unpredictable behaviour. However there is an initial period that can be identified when the device had an erratic light response, which is labelled as T_{break} in Figure 6.17. The time frame for this period varied from device to device. Dark spots near the light-emitting region appeared during this period. In some cases catastrophic failure occurred. This is believed to be due to moisture in the air causing temporary conducting path between the Al electrode and the silicon substrate in high field regions. This is consistent with observation of sparks near the light-emitting facet in some samples.

After the T_{break} period, the EL luminance continuously degraded significantly with time as shown in Figure 6.17. However no variation in α, tunneling current or Q_{int} occurred after 200 hours of device operation other than the reduction measured for the device operated in vacuum. This interesting observation leads to a speculation that the efficiency or the optical properties of the phosphor material exposed to ambient could be changing due to operation in air. However, leaving the device in air without the application of high voltage did not reduce the brightness of the device when operated again. Therefore, it is also possible that electrolysis of the H_2O vapour in the atmosphere near the device is taking place during high field excitation. Hence, the ions generated in the process could be attracted to the active region and diffuse into the material. This could cause a reduction in the efficiency of the phosphor, changes at the emitting facet or modification to the optical guiding properties, e.g. attenuation coefficient. The author proposes a novel measurement technique, given in Further work of Chapter 7, to investigate this phenomenon. In any case, the light measured continuously reduced a factor, which was not reflected in the electrical measurements.

This demonstrates that the operation of ACTFEL device is sensitive to ambient air environment, which leads to negative effect on its EL luminance with operation time. Therefore this has to be prevented in commercial devices by hermetically sealing the structure.

6.2.4 *Comparison with SiON Insulator ACTFEL device*

Electro-Optical measurements were performed on ACTFEL devices utilising Silicon-Oxy-Nitride (SiON) as the top and bottom insulators. The investigation was carried out on commercially available ACTFEL device panels, supplied by Lite Array Inc[20]. The sputter deposition technique was used to fabricate the SiON and the ZnS:Mn phosphor layers. These panels were in the virgin state, which means the standard factory production burn-in process was omitted. The burn-in process involves raising the applied voltage from zero to 40 V above threshold voltage in various time stages, which in total approximates to 3 hours. This voltage is left on for 24 hours to stabilise the device. Finally the burn-in process involves raising the applied voltage by another 20 V to check for dielectric breakdown. In this study, the necessity for the initial ramp up stage is investigated.

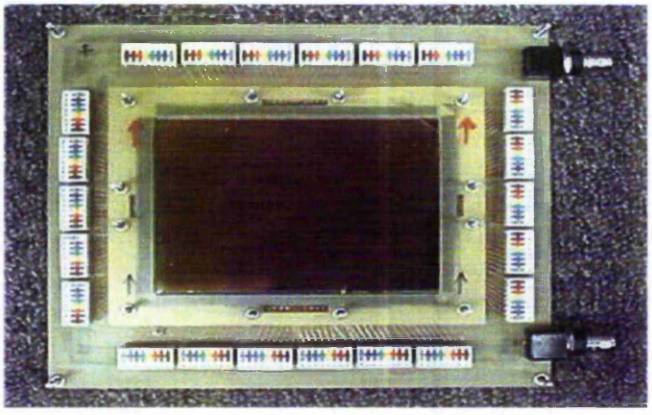


Figure 6.18 A picture of the custom-made measurement rig utilised for testing a commercial ACTFEL quarter VGA display panel. The rig has vertical and horizontal control lines to select a 5 by 5 pixel area.

In Figure 6.18, a custom-made measurement rig for testing of the panels is shown. Measurements were also performed on laboratory testing samples fabricated using the Plasma Enhance Chemical Vapour Deposition (PECVD) technique at Rutherford Appleton Laboratory for the top and bottom SiON layers. The ZnS:Mn layer was deposited using the system described in Section 2.2.1. These devices were used to verify the behaviour of the commercial device.

SiON has a relative dielectric constant ε_r typically[21] between 6 and 7, which is approximately half that of Y_2O_3. However, the lower ε_r value is complimented with a higher dielectric breakdown strength[22,23] E_{bd} typically between 8 and 10 MV/cm. Therefore the figures-of-merit, CSC for these two insulators are comparable. The low ε_r for SiON would require higher voltage to be applied to the ACTFEL device to achieve the same F_P for EL to occur.

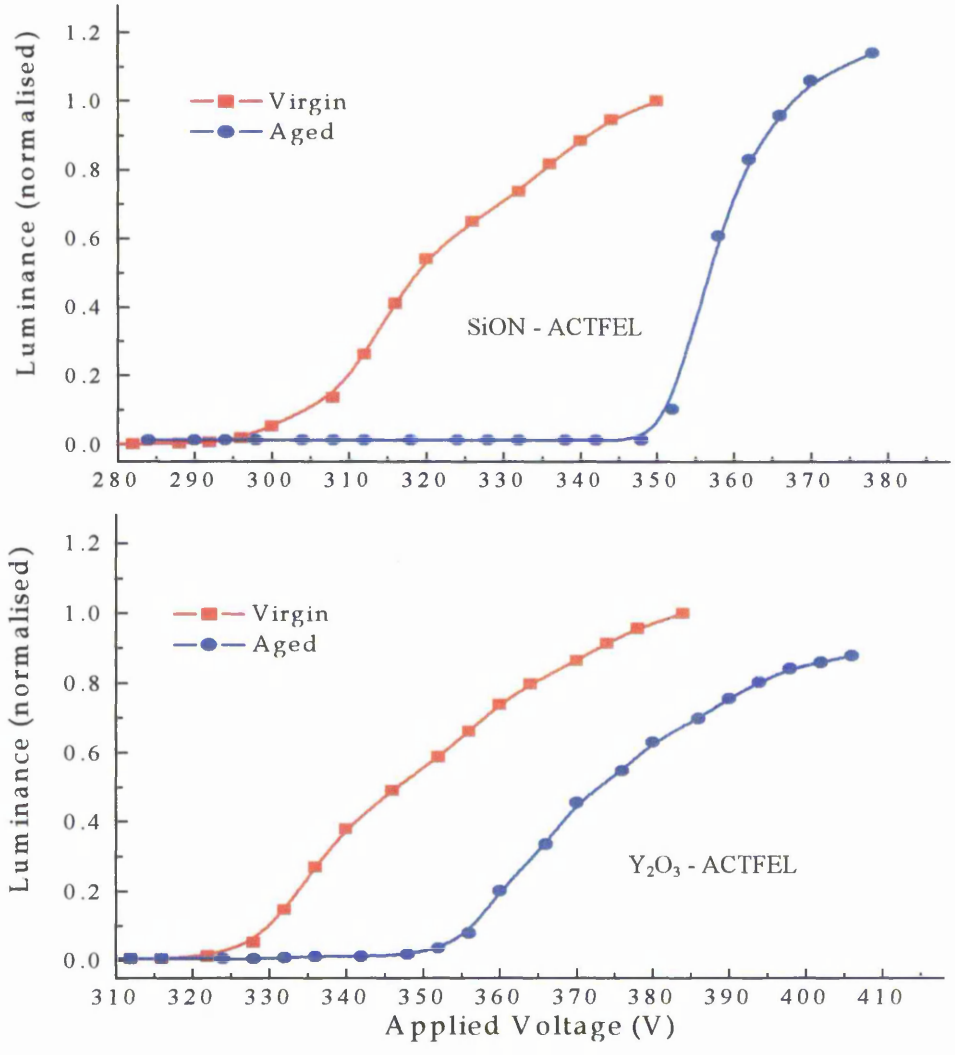


Figure 6.19 LV characteristics for ACTFEL devices with SiON insulator (top) and Y_2O_3 insulator (bottom) in its virgin and aged state. The devices were aged for 25 hours at 50 V above the virgin threshold voltage. The devices were driven with 5 kHz sine wave signal.

Since the SiON insulator has a higher E_{bd}, the extra electric field load on it would not cause a catastrophic breakdown, hence ensuring device operation. Therefore it is common that the SiON insulator layers are made thinner compared to what would be normal for ACTFEL device with Y_2O_3 insulator to achieve a lower device operating voltage. A pronounced difference observed in the characteristics of the SiON insulator ACTFEL device is the large shift in its LV characteristics after ageing. In Figure 6.19, LV characteristics for ACTFEL devices with SiON and Y_2O_3 insulators in the virgin and aged state are shown. EL luminance for these Y_2O_3 ACTFEL devices was measured through the top insulator layer with the active phosphor layer not exposed to ambient. The Aluminium electrode has hole patterns, which allows light to pass through[24]. The devices were aged in air for 25 hours.

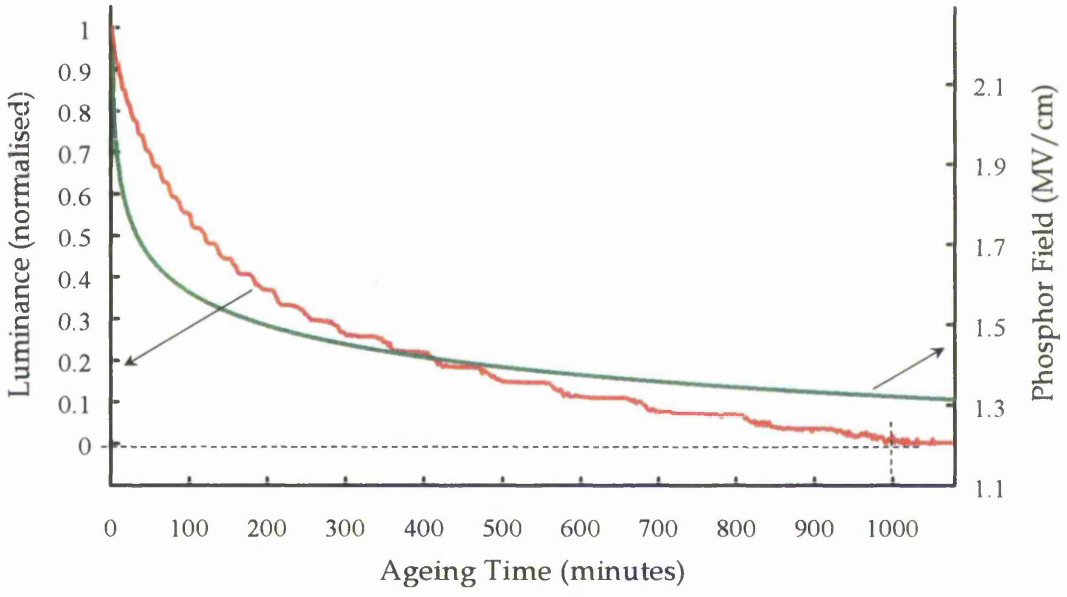


Figure 6.20 Phosphor field and luminance characteristics as a function of ageing time for SiON ACTFEL device, operated at 350 V, 5 kHz sine wave.

The SiON device exhibited a 47 V shift in V_{th} compared to 25 V in the Y_2O_3 device. The shift was mainly due to α reducing, however in the SiON device, α was primarily affected by a decrease in SiON capacitance. The reduction in SiON layer capacitance in combination with the gradual increase in phosphor layer capacitance adversely

degraded EL luminance of the device. This was seen for SiON ACTFEL devices made by both type of fabrication method mentioned above. After approximately 1000 minutes of device ageing no EL luminance was measured from the device. This is because F_P was reduced below E_{th} hence requiring an increase in drive voltage.

The characteristics of F_P and EL luminance as a function of ageing time for SiON insulator ACTFEL device are shown in Figure 6.20. The F_P value falls drastically in the first 50 minutes, which was primarily due to the increase in insulator capacitance. The gradual decrease in luminance after this initial period was mainly due to phosphor capacitance increasing as discussed in the previous section. It is important to note that the LV curve for the SiON device shifts to a point where V_{th} falls close to the voltage at which it was aged, as shown in Figure 6.19 (top).

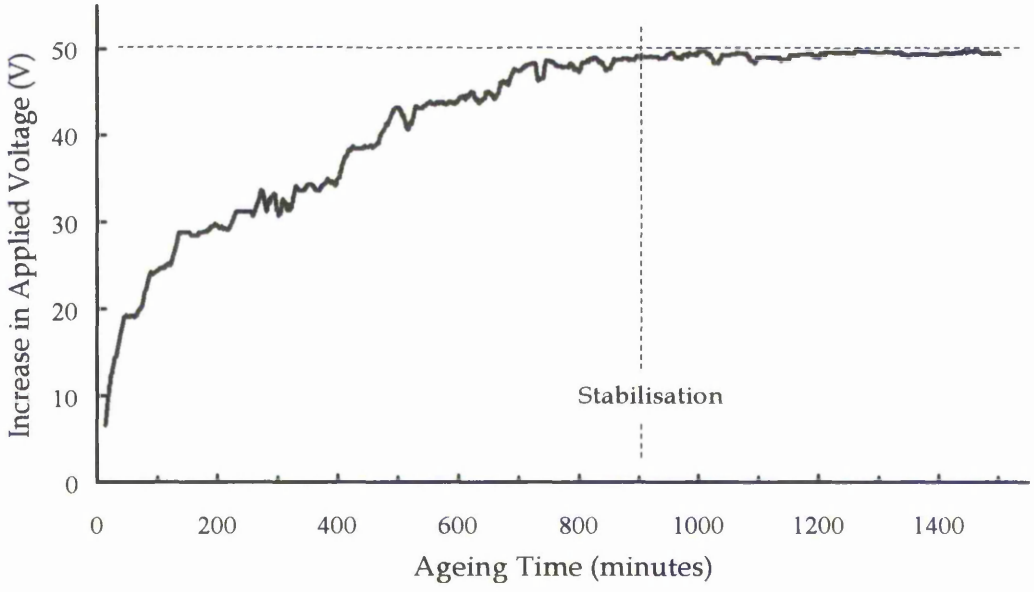


Figure 6.21 The increase in applied voltage that was required to maintain SiON ACTFEL device luminance at 30 V above V_{th} (L_{30}) in its virgin state.

Further investigation was performed to study this behaviour. The applied voltage to the ACTFEL device was increased to maintain device luminance at 30 V above V_{th} (L_{30}) in its virgin state. The increase in device voltage is required to compensate for effects of

ageing, which is primarily a change in α. A computer program was written to control the system described in Section 2.4.1 to automatically perform this task. By maintaining the preset device luminance at L_{30} the increase in applied voltage was monitored. It was found that stabilisation was reached after approximately 900 minutes at which point the applied voltage increase was approximately 50 V as shown in Figure 6.21. The LV characteristic of this type of stressing was also found to produce a softer response shown in Figure 6.22, compared to the typical fixed voltage stressing technique shown in Figure 6.19 (top).

The sharpening of the LV characteristic in the fixed voltage ageing experiment indicates that the interface electron states distribution along the energy bandgap was selectively effected due to the applied field. However in the voltage increase stress experiment only a parallel shift of the LV curve occurred. In Figure 6.23, luminance versus phosphor field graph is shown for the device data from Figure 6.22. The phosphor field for the aged device was calculated with the new value measured for α. The virgin and aged curves fall at the same point with the slopes being very similar, indicating that the shift in V_{th} seen in Figure 6.22 is simply due to a decrease in factor α. This phenomenon was observed in the SiON ACTFEL devices only.

Another important difference between the SiON and Y_2O_3 ACTFEL devices is the amount of recovery in EL luminance achievable with increase in applied voltage. In the SiON device, no permanent reduction in the maximum luminance occurred after stressing. It is simply a matter of increasing the applied voltage to compensate for the decrease in factor α. This is demonstrated in Figures 6.19 (top) and 6.22. This was consistent with increase in I_T measured of a stressed device to it virgin state value at a higher applied voltage. However the Y_2O_3 device showed a permanent drop in the maximum EL luminance achievable, due to redistribution of electron charge at the interface, which effectively decreases Q_{int} as discussed in the previous section. Therefore SiON device has an advantage over Y_2O_3 device for this reason, but requires the initial voltage ramp up burn-in procedure to stabilise the device.

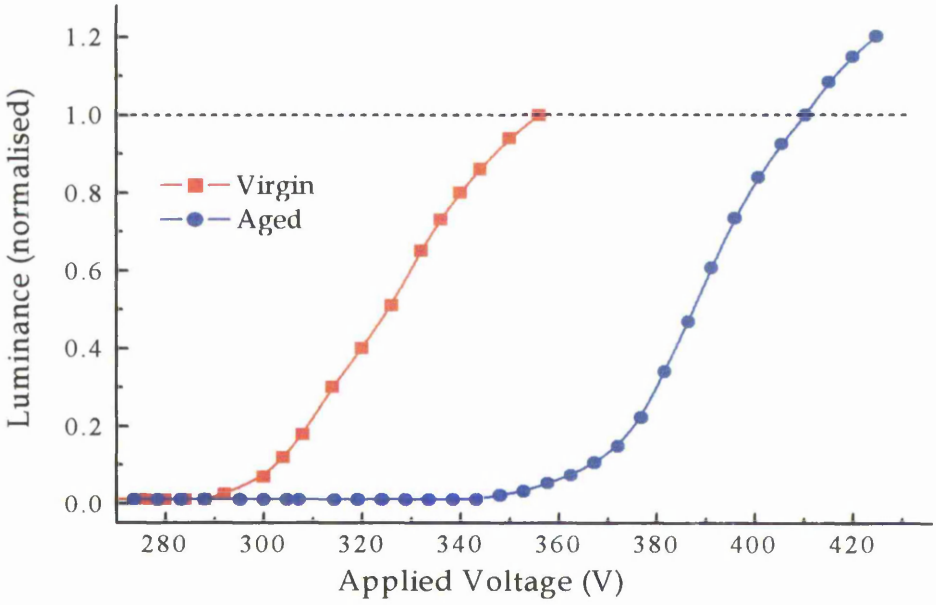


Figure 6.22 LV characteristics for SiON ACTFEL device in its virgin state and electrically aged state by increasing applied voltage from 330 to 380 V gradually in maintaining luminance experiment.

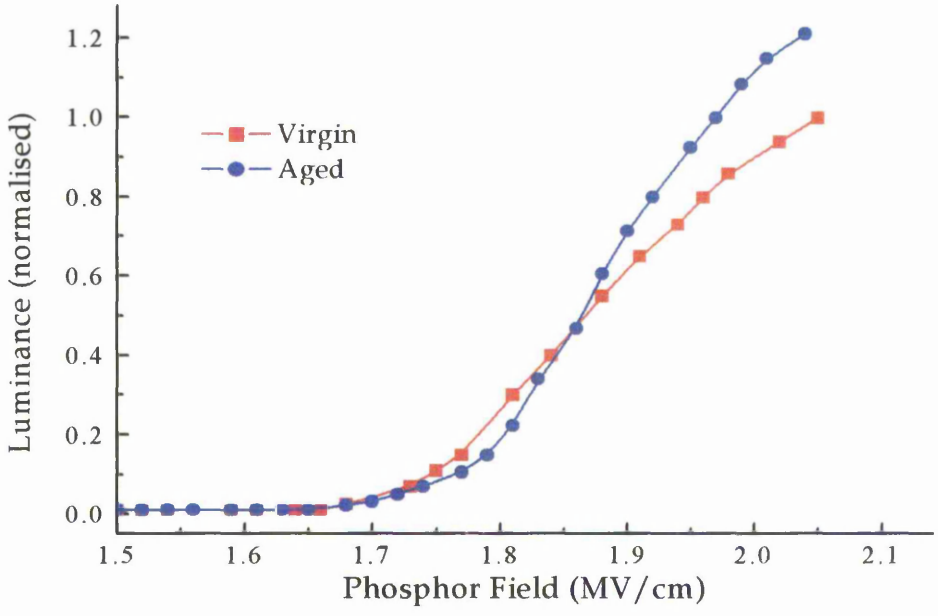


Figure 6.23 Luminance as a function of F_P for the data shown in Figure 6.22. The aged curve is α corrected to compensate for the ageing effect.

The SiON capacitance was found to be not stable in the ACTFEL device especially in the initial period of device operation. Changes in the dielectric capacitance could be due to:

1. Decrease in dielectric constant as a consequence of structural or bulk charge modification.

2. The effective change in layer thickness within the structure due to diffusion at the interface. A reaction such as shown below or partially is likely to take place at the interface.

$$\mathbf{SiON + ZnS \longrightarrow (SO_2)_{gas} + (ZnO)_{conductor} + (ZnN)_{insulator} + (SiO_2)_{insulator}}$$

The formation of Sulphur Dioxide gas could pose a serious problem to the device operation. This would lead into increase in pressure within the ACTFEL structure hence peeling may take place. Peeling of the layers has been observed in some devices here and elsewhere[25]. However, further investigation has to be carried out to study the cause of the instability at the initial operation phase of SiON device.

Absolute EL luminance values of the SiON and Y_2O_3 ACTFEL devices could not be compared because the devices were of different structure. EL light of the SiON devices was measured from the bottom of the stack, whereby light would be attenuated in the bottom insulator layer, Indium Tin Oxide (ITO) and the glass substrate. However it is to be noted that the EL luminance values presented in Figure 6.7 for Y_2O_3 edge-emission structure devices is to the author's knowledge the highest reported luminance for any type of ACTFEL device.

6.2.5 *Device Electrode Breakdown*

Ageing measurements were also performed on ACTFEL device with ITO as a top transparent electrode. A video camera system described in Section 2.4.1 was used to take images of the device to investigate the physical appearance of the display with operation time. In Figure 6.24 a series of pictures of the ITO device at various ageing times are shown. The device was operated in normal ambient condition.

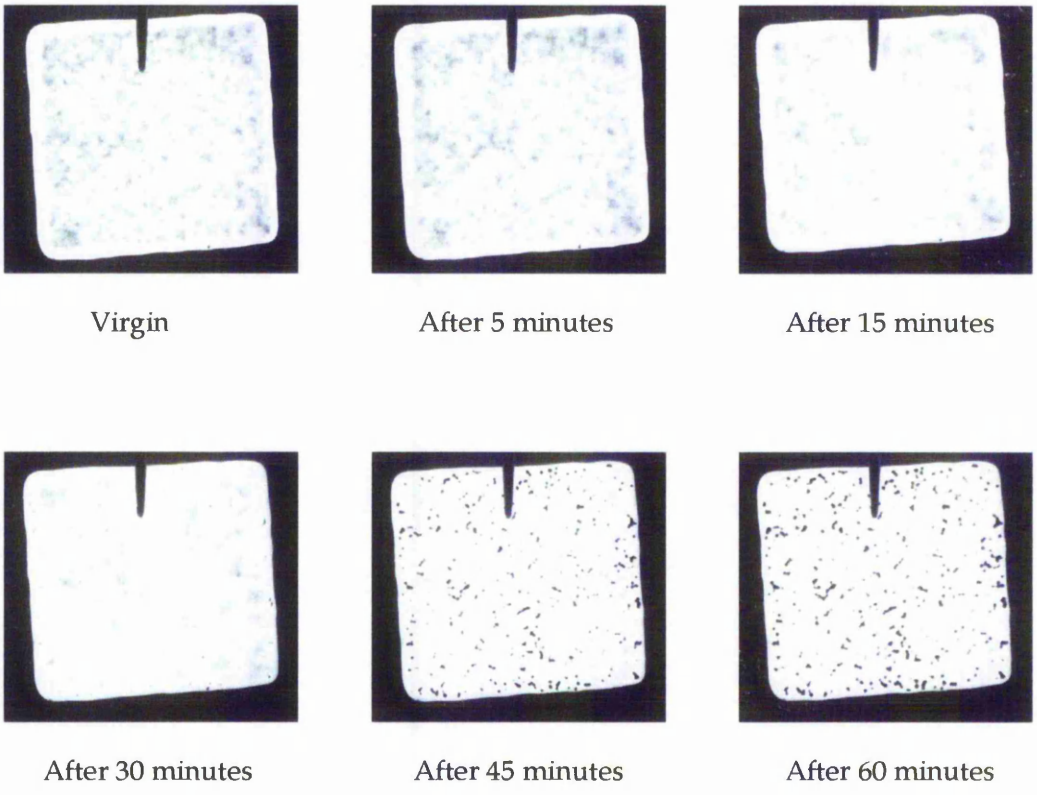


Figure 6.24 Pictures of an ACTFEL device annealed at 400 °C with ITO as the top electrode taken at various times during ageing. The device was operated at 300 V, 5 kHz sine wave in normal ambient.

The above figure shows that as the operation time progresses bright spots appears within the active surface of the device and eventually localised breakdown occurred, forming islands of non-active regions. More pictures of some of the interesting observations made of broken down devices of this type are given in Appendix D.

Breakdown occurred much sooner in this type of device. This is the reason why ageing measurements described in the previous sections could not be carried out on this type of device. ITO was found to be not a good top electrode especially when exposed to the ambient. This transparent electrode turned milky and cracks appeared on the surface after ageing. In Figure 6.25, a picture of an ACTFEL device with top ITO electrode is shown after the device was aged for 15 hours.

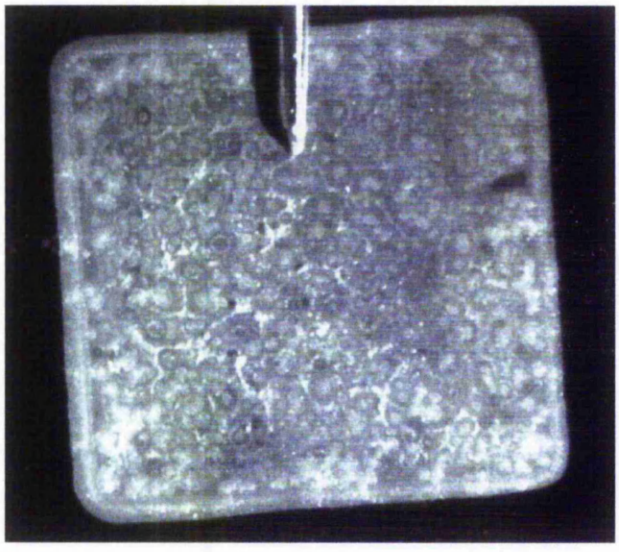


Figure 6.25 A picture of an ACTFEL device with ITO top electrode after being operated for 15 hours at 300V. The picture was taken with external light and the device was turned off. It can be seen that the ITO surface is full of crack and has turned milky.

The pictures shown in Figure 6.24 and 6.25 clearly indicate that the primary reason for the device breakdown is the ITO electrode layer. It is believed that some kind of stoichiometry change between the Indium, Tin and Oxygen could take place during current conduction through the layer by reacting with the ambient gases leading to a chemical instability of the ITO. This could be the cause for the observation. Additionally it was found that the ITO layer was stable when utilised as bottom electrode. This was the case in the commercial SiON ACTFEL device discussed in the previous section. Pictures of broken down ACTFEL device utilising standard Al as top electrode are shown in Appendix D.

6.3 Summary and Conclusions

Characterisation of the electrical and optical mechanisms governing the ACTFEL display device was performed. A systematic experimental approach was utilised to investigate the ageing behaviour of the device. A model of the interface charge properties of the Y_2O_3 insulator and ZnS:Mn phosphor interface is presented. It has been shown that the interfacial charge density and distribution is critical in determining the operation characteristics of the device whereby annealing and ageing affects it. This highlights a potential for interface engineering.

Annealing the ACTFEL device is important for achieving higher EL luminance and improves device stability. However, annealing the samples for more than 1 hour at the same temperature did not reduce the density of non-radiative sites. Devices annealed at lower temperatures (e.g. 400 °C) exhibited a sharp turn on characteristics, which would be suitable for binary addressed display devices, whereas samples annealed at higher temperatures (e.g. 700 °C) are excellent for grey scale display devices. The difference in characteristics is mainly due to redistribution of density of interface states to lower energy levels with increase in annealing temperature.

Annealing the device at higher temperatures did not improve the EL from the ACTFEL device as much as it improved the PL intensity from thin film ZnS:Mn. It was identified that a decrease in injected interface charge was the cause for saturation in EL intensity at higher annealing temperatures. A decrease in EL excitation efficiency is introduced at higher annealing temperatures. For the first time, CV analysis was utilised to explain this phenomena.

All samples had a softer luminance response to applied field after ageing because of the self-annealing of the interfaces from the heat generated in the device during operation. Hence the device characteristics become similar to devices annealed at higher temperature or annealed for an extended time. Concomitantly, creation of shallow interface states occurs during the first few minutes of ageing, contributed to device characteristics after ageing.

Devices annealed 400 °C had the most stable ageing behaviour in vacuum environment. These devices had an initial drop in EL luminance, which was mainly due to a decrease in injected interface charge. However after this initial drop in EL intensity, only a gradual decrease in luminance was measured. This is unlike the devices annealed at higher temperatures. These devices had a significant drop in EL intensity with ageing time, especially during the early stages of operation. It has been shown that this was due to a combination of decrease in injected interface charge and the more prominent occurrence of LDB in ZnS:Mn thin film layer for devices annealed at higher temperatures during the initial phase of operation.

Additionally, the continuous decrease in EL luminance after the initial phase was due to a constant decrease in phosphor field at the same applied voltage because of increase in phosphor layer capacitance. The capacitance instability of the phosphor layer is believed to be due to sulphur vacancies. The experimental observations correlating the thin film studies and the ACTFEL EL luminance degradation for different anneal temperatures during the ageing process were very consistent.

Operating the ACTFEL device in normal ambient condition caused a rapid drop in luminance. EL light output also had an unreliable response. Humidity in the air is believed to cause this detrimental behaviour.

The SiON insulator ACTFEL devices exhibited a large positive shift in LV characteristics, which does not occur in Y_2O_3 insulator devices. It has been demonstrated that the shift was primarily due to a decrease in SiON thin film capacitance, which affects the phosphor field ratio, α. However this degradation mechanism in SiON insulator device can be simply compensated for by increasing the applied voltage. For this reason the SiON ACTFEL device has an advantage over Y_2O_3 device. This is because the initial EL luminance drop that occurs in Y_2O_3 ACTFEL devices cannot be recovered. However, the SiON devices require an initial voltage ramp up burn-in procedure to stabilise the light output.

ITO electrode was found to be not suitable as a transparent top electrode. This is because breakdown occurred on the electrode layer believed to be reaction with ambient air. However its use as a bottom electrode has proven to be very stable.

6.4 References

1 A.F. Cattell & A.G. Cullis, Thin Solid Films, 92 1982 Pg. 211

2 T. Matsuoka, M. Nishikawa, J. Kuwata, Y. Fujita, T. Tohda & A.Abe Jap. J. Appl. Phys., 27/8 1988 Pg. 1430

3 A. Fuh, R.P. Gallinger, P.Schuster, J. Adolph & O. Caporaletti, Thin Solid Films, 207 1992 Pg. 202

4 A.N. Krasnov, R.C. Bajcar & P.G. Hofstra, J. Vac. Sci. Tech., A 16/2, 1997 Pg. 906

5 R.Mach , in 5th International Workshop Electroluminescent 1990. Pg. 85

6 D.H. Smith, J. of Luminescence, 23 1981 Pg. 209

7 J.F. Wager & P.D. Keir, Annual Rev. Mater. Sci., 27 1997 Pg. 223

8 A.N. Krasnov & P.G. Hofstra, Progress in Crystal Growth and Characterization, 2001 Pg. 65

9 W.M. Cranton, Ph.D. Thesis, Bradford University, U.K. 1995

10 J.D. Davidson, J.F. wager, R.I. Khormaei, C.N. King & R. Williams, IEEE Trans. Electron Devices, 39 1992 Pg. 1122

11 E.A. Mastio, Ph.D. Thesis, Nottingham Trent University, U.K. 1999

12 J.F. Wager & P.D. Keir, Annual Rev. Material Science, 27 1997 Pg. 223

13 J.F Wager, Proceedings of 8th Int. Workshop Inorganic and Organic Electroluminescence, 1996, Pg. 33

14 Jörg Rüdiger, Ph.D. Thesis, Nottingham Trent University, U.K. 2001

15 S. Kobayashi, J.F. Wager & A.A. Dayah, Proc. of the Sixth Int. Workshop 1992 Pg. 234

16 A. Aguilera & V.P. Singh, IEEE Transactions on Electron Devices, 41/8 1994 Pg. 1357

17 A.Abu-Dayah & J.F. Wager, J. Appl. Phys., 75/7 1993 Pg. 3593

18 B. Soenen, K. Neyts, J.Vd. Bossche, & P. De Visschere, J. of SID 4/4 1996 Pg. 319

19 S. Shih, P.D. Keir & J.F. Wager, J. Appl. Phys., 79/9 1995 Pg. 5775

20 Lite Array Incorporated, USA, www.litearray.com

21 B. Hajji, P.Temple-Boyer, F. Olivie, A. Martinez, Thin Solid Films 354 1999 Pg. 9

22 J.A. Diniz, A.P. Sotero, G.S. Lujan, P.J. Tatsch & J.W. Swart, Nuclear Instruments & Methods in Physics Research B 166-167, 2000 Pg. 64

23 H. Sato, H. Kato, Y. Ohki, S.S. Kwang & T. Noma, 33rd Symposium on Electrical and Electronic Insulating Materials and Applications in Systems (IEEE), 2001, Pg. 148

24 M. R. Craven, Ph.D. Thesis, Nottingham Trent University, U.K. 2000

25 S.K. Tiku & S.H. Rustomji, IEEE Int. Display Research Conference, 1988 Pg. 36

CHAPTER 7

THESIS CONCLUSIONS

7.1 Introduction

The primary objective of the research presented in this thesis is to investigate the mechanisms which influence the performance of ACTFEL devices. In order to achieve the aim, the individual thin film materials and the resultant ACTFEL devices were separately characterised and modelled. The major areas of study were:

1. **Thin film Y_2O_3** : Electrical and structural properties were characterised to address fabrication issues for a reliable and optimum insulator for use in ACTFEL device construction. Additionally, a feasibility study of Y_2O_3 for use as high-κ thin film material in integrated circuits was performed.
2. **ZnS:Mn phosphor** : Electrical, structural and phosphor efficiency were studied as a function of fabrication parameters and to identify their relationship.
3. **ACTFEL devices** : Electro-optical characteristics and operation behaviour were examined to obtain an understanding of the contributing factors to the behaviour in order to improve of device performance.

7.2 Conclusions of the Studies

The investigations listed above were used to correlate the thin film study to the characteristics of the ACTFEL device. This systematic approach revealed many insights to the operation behaviour of ACTFEL devices.

In the fabrication process of thin films, the quality of the starting material is of high importance. Initially, Y_2O_3 thin films were associated with reproducibility problems. It has been demonstrated that the condition of the target material mainly contributed to this problem. However after a "Pre-Stable" period during the target's lifetime, this problem is removed. The structural properties for Y_2O_3 thin film significantly improved after annealing the samples at a minimum temperature of 300 °C for 1 hour. Additionally, CV analysis verified that annealing the sample at higher temperatures reduced bulk and interface charge traps. However this dielectric material had the best breakdown strength when annealed at 400 °C.

The intrinsic bulk charge of Y_2O_3 thin films has been identified to be positive. Additionally, annealing this dielectric in a low-pressure oxygen environment has been shown to increase its dielectric constant. These evidences indicate that bulk defects could be due to oxygen vacancies. The low-pressure oxygen environment heat-treatment has been demonstrated to also have the advantage of avoiding the creation of a silicon based oxide interfacial layer between Y_2O_3 and the silicon substrate.

A minimum of 100nm thick Y_2O_3 thin film has to be fabricated for its practical use, because the material closer to the bottom interface was found to be defective and have a low breakdown strength and dielectric constant value. It has been demonstrated that Y_2O_3 thin films have good interfacial properties for use as a bottom layer to produce ZnS:Mn thin film of superior crystalline cubic phase structure. Additionally, this material has a high Charge Storage Capacity value of $5\mu C/cm^2$ and was found to be very stable under high field stressing. Therefore Y_2O_3 thin film is a very suitable

insulating material for use in ACTFEL devices and future integrated circuits as high-κ gate material.

Previously, feasibility studies have been performed on integrating this display device with its driver electronics in the semiconductor substrate utilised to fabricate the display structure[1,2]. Additionally, with the growing interest in flexible displays, Y_2O_3 could also be used as a transparent gate or back insulation material. Therefore, the use of Y_2O_3 would have a cost and production advantage being utilised for both applications.

Sputter depositing ZnS:Mn thin films at 200 °C substrate temperature produced the best crystallinity and the brightest PL for all annealing temperatures studied. In addition, annealing the ZnS:Mn thin film phosphor at temperatures between 400 and 600 °C resulted in a linear improvement in PL efficiency with increase in annealing temperature. Hence, this implies that the phosphor material has much more potential than achievable with these annealing temperatures. In conclusion, the PL efficiency for thin film ZnS:Mn has been shown to be dependent on:

1. The crystalline quality of this material, which was primarily dependent on the deposition temperature.
2. The density of luminescent centres, which was proportional to the annealing temperature.

The ZnS:Mn thin film also exhibited the highest breakdown strength when annealed at 400 °C. Additionally, Localised Destructive Breakdown occurrence in ZnS:Mn thin film increased with annealing temperature. Leakage current also increased significantly for annealing temperatures higher than 400 °C. This is believed to be a consequence of increase in sulphur vacancies with increase in heat treatment temperature in vacuum giving rise to donor traps, which behaves as electron hoping centres.

This material exhibits a finite increase in thin film capacitance on the application of high field. It is proposed that this is due to neutralisation of positively charged sulphur

vacancies by injected electrons. This phenomenon contributed to the EL luminance degradation in ACTFEL devices, especially during long period of ageing.

It has been shown that heat-treating the ACTFEL device is necessary for higher EL luminance and better device stability. However the conventional annealing procedure described in the thesis lowers the threshold applied voltage for EL excitation with increase in annealing temperature and time. Additionally, EL response to applied voltage becomes softer with increase in annealing temperature and time. These alterations in ACTFEL device characteristics are a consequence of modifications to the interface properties, which also saturates EL luminance at higher annealing temperatures. A significant part of the research was directed towards investigating these relationships. High voltage CV analysis was used to investigate the interface charge properties. The saturation in EL luminance at higher annealing temperature has been demonstrated to be primarily due to a reduction in the pre-clamping interface charge available for EL excitation. Therefore annealing the whole ACTFEL structure not only conditions the individual thin film layers but also has a negative effect on the efficiency for EL excitation especially at higher annealing temperatures.

The design of the ACTFEL device utilises the interface states to generate the primary source of electrons for EL excitation. This mechanism has inherently proven to be a weakness in the chain of events required to produce high luminance EL light. The materials creating the interface and the fabrication parameters are directly related to the interface state density and distribution. Currently, very little control is available over these interface properties and no formulation available for engineering of these parameters. It has also been demonstrated that the ageing process also affects the interface states and contributes to a dynamic device behaviour.

For the first time, device self-annealing explanation is presented to associate the ACTFEL device ageing behaviour with different annealing temperatures and durations. Additionally, the better stability and long lifetime for ACTFEL devices annealed at 400°C have been shown to be directly related to the better electrical properties of ZnS:Mn thin films annealed at that temperature.

Hence, one should take account of device stability, maximum EL luminance achievable and EL luminance response to applied voltage characteristics for selecting the appropriate post-deposition annealing parameters. Operating the ACTFEL display device exposed to the ambient condition degrades the EL luminance very rapidly and becomes more vulnerable to catastrophic breakdown. Therefore to prolong device lifetime, the active region of the device has to be kept away from air in the ambient.

The comparative study performed on ACTFEL devices utilising Y_2O_3 and a Silicon based dielectric (SiON) revealed that these two types of devices have different EL luminance to applied voltage response, especially after some ageing. Additionally, the SiON ACTFEL device requires a voltage ramp up burn-in procedure to stabiles the large positive threshold voltage shift, which occurs in this device during initial operation. This phenomenon is due to a decrease in the thin film SiON layer capacitance that decreases the field across the phosphor layer. This is not seen with Y_2O_3 ACTFEL devices mainly because this insulator is stable under high field. However, the Y_2O_3 ACTFEL device under goes a permanent drop in EL luminance due to modifications to the interface properties within the first few hundred minutes of operation, which the SiON ACTFEL devices do not exhibit. Therefore the initial degradation mechanism for these two types of devices is different. However a contributing factor to the long term ageing mechanism is the increase in ZnS:Mn thin film layer capacitance that decreases the field across the phosphor layer for an applied voltage.

Finally, the understanding obtained from this study provides room for new concepts and further research, which are detailed in the following section.

7.3 Further Work

7.3.1 Proposed Engineering for Optimising ACTFEL Device

Utilising the understanding obtained from this work, the author proposes a route that incorporates some innovations to the standard fabrication route, which is believed to produce a more enhanced performance ACTFEL device. The innovations given here are for the ACTFEL device type utilised for this study (edge emission or vertical top out emission). However, the processing could be applied to the industrial standard type described in Figure 1.1 in a similar fashion. The innovations mainly concern improving the internal EL efficiency. The following steps corresponds to Figure 7.1, describes the proposed processing route:

1. Deposition of 200 nm thick, bottom Y_2O_3 thin film on a conducting substrate. It has been shown in Chapter 3 and 4 that this oxide insulator has better structural and electrical properties in thicker films, however it is sufficient to utilise 200 nm. This would have an advantage of lowering the threshold voltage of the ACTFEL device. After deposition, the structure should be thermally annealed at 400 °C, which is the most electrically optimum temperature for this insulator among the temperatures studied. Though annealing this oxide insulator at higher temperature would reduce the silicon interface charge traps, demonstrated in the Y_2O_3 MIS study, however this would have no advantage at high field operation required for ACTFEL device.

2. Ion bombardment of the Y_2O_3 surface to "roughen" it. It has been shown in the Y_2O_3 thin film study that thermal annealing produces a more orientated crystal structure, which reduces parasitic charges. However this is not desirable at the interface between the insulator and phosphor. This is because a defective structure has more charges associated with it. Therefore an electronically bad interface would have more defects that could create charge traps. These charge traps are interface states, which are essential for EL excitation. Therefore some method of energetic inert ion bombardment maybe used to create damage to the surface structure hence increasing the possibility of creating more electronic defects at the interface. This process should be performed in-situ to avoid breaking chamber vacuum.

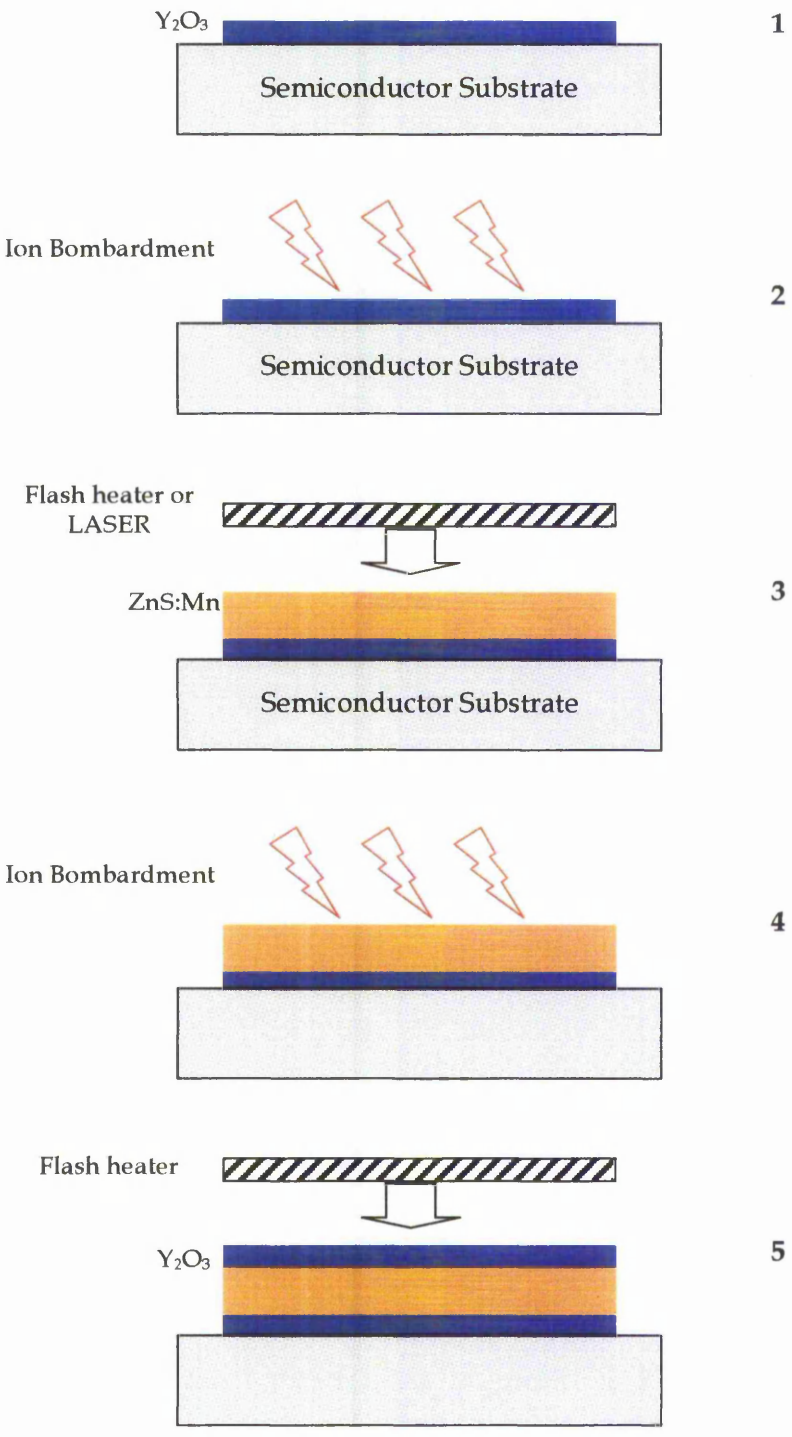


Figure 7.1 The fabrication route proposed by the author for engineering an optimised ACTFEL device. The descriptions of the steps are given in text above.

3. Deposition of 800 nm thick ZnS:Mn thin film on Y_2O_3 thin film with the roughened surface. This process should be followed by annealing the phosphor layer to improve the phosphor efficiency. However this step should be carried out without annealing the interface. It has been demonstrated in Chapter 6 that annealing the interface alters the interface state distribution to become non favourable for efficient EL excitation. Therefore the phosphor layer alone should be selectively annealed. Laser annealing[3,4] or flash annealing the top surface has the ability to perform such a task. Annealing temperature should be optimised for maximum phosphor efficiency.

4. Ion bombardment of the ZnS:Mn surface in-situ to "roughen" it. Again the interface is roughened to increase the possibility of creating more charge traps.

5. Deposition of 200 nm thick, top Y_2O_3 thin film on ZnS:Mn thin film with the roughened surface. Finally flash annealing at 400 °C should be performed for heat-treating the top Y_2O_3 layer without annealing the second interface. This process is also done on the top insulator to improve the dielectric without reducing the EL efficiency of the second interface.

These innovations are believed to produce a high-density interface trap states more efficient for EL excitation. Additionally, the individual and independent thin film post-deposition annealing would have a more optimised heat treatment for improved electrical and structural properties of the individual layers. However it is also believed that there would be limitation associated with this design as given below:

- Increase interface roughness would possibly contribute to more LDB in the ZnS:Mn thin film.
- Increase roughness at the interface could also increase light scattering hence contributing to brightness loss.
- More complex fabrication route would incur more production cost.

Therefore the proposal also includes a systematic study to address these concerns. Additionally, an investigation should be performed in assessing and optimising each innovation presented above.

7.3.2 *Insulator materials*

The study on SiON ACTFEL devices reveals that the insulator capacitance goes through a forming process at the initial operation period, shifting the LV characteristics to a higher voltage scale. On the other hand, the use of Y_2O_3 as the insulating material caused modification to the interface states during initial ageing to become non-favourable for EL excitation. Therefore, it is proposed that the use of SiON interlayer (~10nm thick) between Y_2O_3 and ZnS:Mn thin film could improve the EL ageing characteristics of ACTFEL devices. This new design will address the initial degradation mechanism related to Y_2O_3 thin film being used as the insulator layers in ACTFEL devices.

Additionally, to further understand the forming process in SiON thin films, the electrical stressing experiment should be carried out on this material. Also, the study performed on the Y_2O_3 insulator ACTFEL devices should be carried out on alternative insulating materials, for example materials listed in Table 1.2. This would provide even more understanding of ACTFEL devices, especially on the interface properties.

7.3.3 *ZnS:Mn Thin Film Study*

The increase in ZnS:Mn thin film capacitance under high field stressing is believed to be caused by sulphur vacancies in the bulk. Additionally, these vacancies would behave as donor trap, which are detrimental for efficient EL excitation. This could be reduced or eliminated by using a sulphur rich target material or by the introduction of H_2S in the deposition[5,6] or annealing[7] process. By performing electrical characterisation on the improved thin film, the reason given here for the increase in thin film capacitance and the poorer dielectric properties for sulphur deficient material can be verified. Hence, the long-term degradation and failure mechanisms due to ZnS:Mn layer in ACTFEL devices can be addressed.

7.3.4 *Attenuation Coefficient*

The ACTFEL display devices used for this study are of laterally emitting type, described in Section 2.4.2. Therefore, the light attenuation coefficient (α_{op}) of the phosphor material is an important parameter for the light guiding property of the device. Structural differences observed in ZnS:Mn thin films with changes in fabrication parameters (Chapter 5) could alter the light scattering properties in the material, hence modify α_{op}. Additionally, as discussed in Sections 5.4.2 and 6.2.3.2, with the presence of high field, the light guiding property of the phosphor material may also be affected. The author proposes a novel measurement technique to investigate these issues.

A CCD camera is utilised to obtain images of the region under investigation as shown in Figure 7.2. The Field-Of-View (FOV) of the camera is focused to the area slightly outside the active ACTFEL region where AC high voltage signal is applied for normal EL operation. Since the phosphor thin film has optical wave guiding properties, EL light would be injected into the non-active region. A very thin line (of the order of few microns thick) must be etched on the transparent electrode to have a separation from the active region in order to isolate the region under investigation electrically. In the absence of the thin line of transparent electrode material, the effective refractive index may change, hence could incur some light loss. Ideally this region should be filled with an insulating material of the same refractive index with the electrode material. However, even without the filing material light spreading would still take place into the region, with sufficient light transmission to perform the measurement.

Utilising the camera, pictures of the region under investigation with the active ACTFEL region completely switched on should be taken. Such a measurement was performed previously[8], however without transparent electrodes, revealed that the distance of injection to be less than 0.5 mm. A possible picture of region under investigation is given in Figure 7.3. By analysing the picture digitally, the α_{op} may be approximated. The value can be obtained by plotting the pixel luminance value as a function of material length.

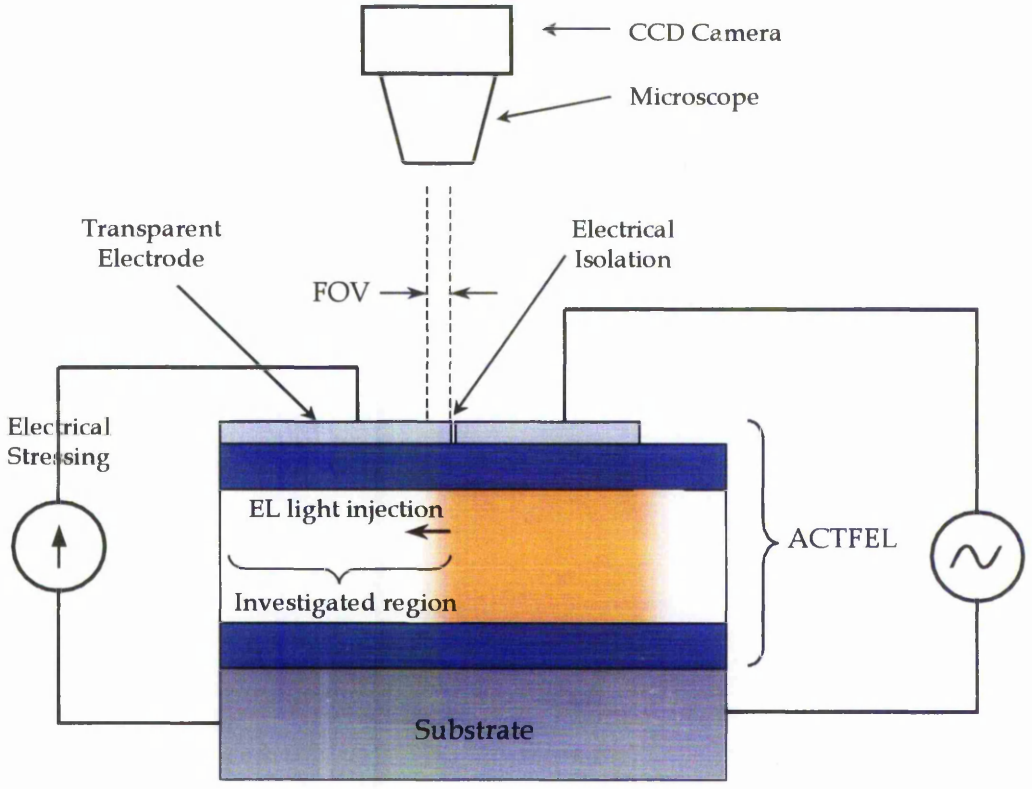


Figure 7.2 Schematics of the CCD image capture of a Laterally emitting ACTFEL device. The configuration could be utilised to investigate decay of luminance as a function of material length injected from an active ACTFEL region into the phosphor region under investigation.

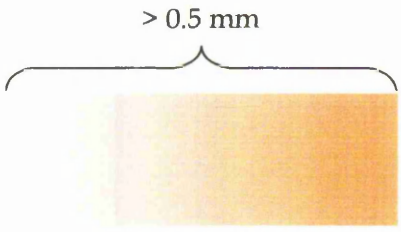


Figure 7.3 A possible image captured from the CCD camera from Figure 7.2 of the region under investigation (FOV) is illustrated.

Luminance (L) as a function of material length (x) can be calculated using Eq. 7.1, given below

$$\mathbf{L(x) = Io\ exp^{(-\alpha_{op} x)}} \qquad \text{Eq. 7.1}$$

where I_0 is the maximum intensity (luminance at the point of injection into the region under investigation). By using a curve fitting routine, α_{op} is obtained.

Performing this measurement on a region under investigation during its virgin and electrically stressed state, differences in α_{op} could be studied. This measurement could also be performed in various humidity levels to give more insight to the reasons behind the rapid EL luminance degradation for devices operated in ambient condition.

Additionally, α_{op} could be measured while applying an electric field across the region under investigation to investigate any variation that this may cause. The structural properties of the phosphor material could also be studied in relation to its light guiding property.

This experiment could not be performed during this programme time frame because the ACTFEL device described in Figure 7.2 could not be obtained in time.

7.3.5 Y_2O_3 Target Surface Analysis

During the early stages of the Y_2O_3 target's life the thin film produced were of lower quality as presented in Chapter 3. Material analysis of the target surface at various stages of its lifetime would reveal information regarding the depletion rate of the individual species of this material. This investigation would assist in making a material graded target to reduce the "Pre-Stable" period.

7.4 References

1 Jörg Rüdiger, Ph.D. Thesis, Nottingham Trent University, U.K. 2001

2 S.P.S. Theng, Ph.D. Thesis, Nottingham Trent University, U.K. 2001

3 H.S. Reehal, J.M. Gallego & C.B. Edwards, Appl. Phys. Lett., 40/3 1982 Pg. 258

4 E.A. Mastio, Ph.D. Thesis, Nottingham Trent University, U.K. 1999

5 C. Chen, S. Husurianto, X. Lu and M.D. Koretsky, J. Elecrochemical Soc., 145, 1 1998 Pg. 226

6 H.Xian, P. Benalloul, C. Barthou & J. Benoit, Thin Solid Films, 248 1994 Pg. 193

7 C. Tsakonas, C.B. Thomas, J. Appl. Phys., 78,9 1995 Pg. 6098

8 M. R. Craven, Ph.D. Thesis, Nottingham Trent University, U.K. 2000

APPENDIX

APPENDIX A

High Voltage Amplifier Design Details

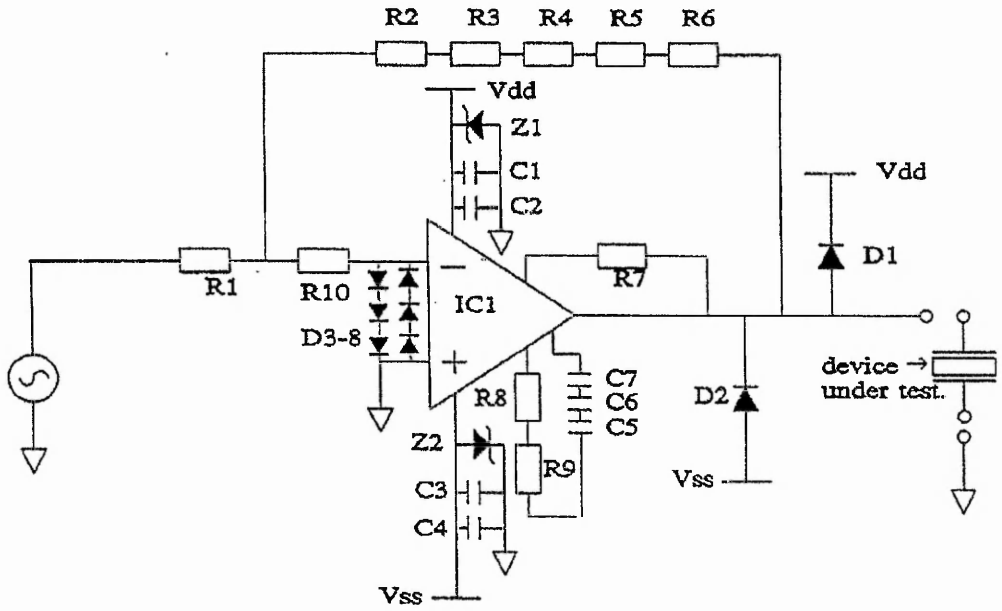


Figure A.1 Circuit diagram of the High Voltage Amplifier used for operating the ACTFEL devices.

Label	Value
IC1	Apex PA89 HV Op-Amplifier
R1	16kΩ
R2 - R6	100kΩ
R7	18Ω
R8 & R9	110Ω
R10	1kΩ
D1 & D2	100nSec, BYT01-400
Z1 & Z2	270V, BZT03C270
C1 & C3	10μF
C2 & C4	10nF
C5 - C7	100pF
C8 - C15	0.47μF
D3 – D8	1N4148

Table A.1 listing the components used in the HV amplifier circuit design.

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIERS

PA89 • PA89A

PATENTED

FEATURES

- 1140V P-P SIGNAL OUTPUT
- WIDE SUPPLY RANGE — ±75V to ±600V
- PROGRAMMABLE CURRENT LIMIT
- 75 mA CONTINUOUS OUTPUT CURRENT
- HERMETIC SEALED PACKAGE
- INPUT PROTECTION

APPLICATIONS

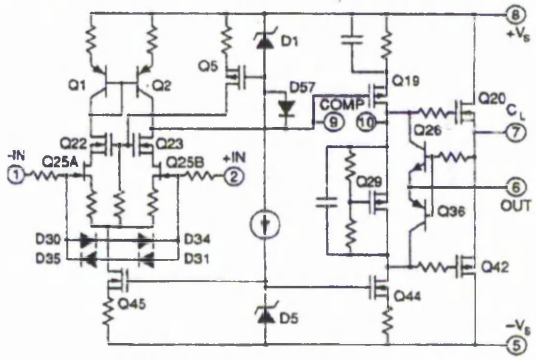
- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC DEFLECTION
- SEMICONDUCTOR TESTING

DESCRIPTION

The PA89 is an ultra high voltage, MOSFET operational amplifier designed for output currents up to 75 mA. Output voltages can swing over 1000V p-p. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration and 120dB open loop gain. All internal biasing is referenced to a bootstrapped zener-MOSFET current source, giving the PA89 a wide supply range and excellent supply rejection. The MOSFET output stage is biased for class A/B linear operation. External compensation provides user flexibility. The PA89 is 100% gross leak tested to military standards for long term reliability.

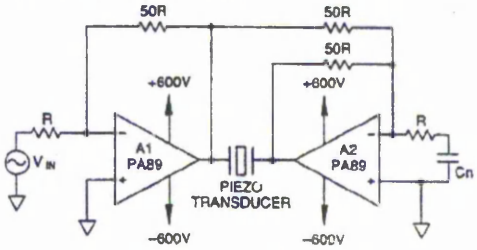
This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The MO-127 High Voltage, Power Dip™ package is hermetically sealed and electrically isolated.

SIMPLIFIED SCHEMATIC



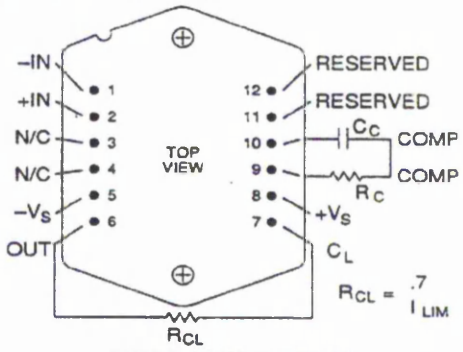
TYPICAL APPLICATION

Ultra-high voltage capability combined with the bridge amplifier configuration makes it possible to develop +/–1000 volt peak swings across a piezo element. A high gain of –50 for A1 insures stability with the capacitive load, while "noise-gain" compensation Rn and Cn on A2 insure the stability of A2 by operating in a noise gain of 50.



SINGLE AXIS MICRO-POSITIONING

EXTERNAL CONNECTIONS*



PHASE COMPENSATION

Gain	C_c	R_c
1	470pF	470Ω
10	68pF	220Ω
15	33pF	220Ω
100	15pF	220Ω

Note: C_c must be rated for full supply voltage –Vs to +Vs.
See details under "EXTERNAL COMPONENTS".

PA89 • PA89A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	1200V
OUTPUT CURRENT, within SOA	100mA
POWER DISSIPATION, internal at T_C = 25°C	40W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S \mp 25V$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to 125°C
OPERATING TEMPERATURE RANGE, case	–55 to 125°C

SPECIFICATIONS

		PA89			PA89A			
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			7			*		µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT,vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			5	50		3	20	pA
INPUT IMPEDANCE, DC			10^9			*		MΩ
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S \mp 50$			*			V
COMMON MODE REJECTION, DC	Full temperature range, V_{CM} = ±90V	96	110		*	*		dB
INPUT NOISE	10kHz BW, R_S = 10K, C_C = 15pF		4					µV RMS
GAIN								
OPEN LOOP GAIN at 10Hz	R_L = 10k, C_C = 15pF	108	120		*	*		dB
GAIN BANDWIDTH PRODUCT	R_L = 10k, C_C = 15pF, A_V = 100		10			*		MHz
POWER BANDWIDTH	R_L = 10k, C_C = 15pF, V_O = 500V p-p		5			*		kHz
PHASE MARGIN	Full temperature range, A_V = 10		60			*		°
OUTPUT								
VOLTAGE SWING[4]	I_O = 75mA	$\pm V_S \mp 30$	$\pm V_S \mp 15$		*	*		V
VOLTAGE SWING[4]	Full temperature range, I_O = 20mA	$\pm V_S \mp 20$	$\pm V_S \mp 12$		*	*		V
CURRENT, continuous	Full temperature range	75			*			mA
SLEW RATE	C_C = 15pF, A_V = 100	12	16		*	*		V/µs
CAPACITIVE LOAD, Av = 10	Full temperature range			1			*	nF
CAPACITIVE LOAD, Av>10	Full temperature range			SOA			*	
SETTLING TIME to .1%	R_L = 10KΩ, 10V step, Av = 10		2			*		µs
POWER SUPPLY								
VOLTAGE, V_S[4]	Full temperature range	±75	±500	±600	*	*	*	V
CURRENT, quiescent			4.8	6.0		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz		2.1	2.3		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz		3.3	3.5		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		15			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

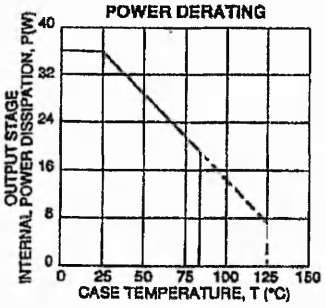
NOTES: * The specification of PA89A is identical to the specification for PA89 in applicable column to the left.
1. Unless otherwise noted: T_C = 25°C, C_C = 68pF, R_C = 220Ω, and V_S = ±500V. Input parameters for bias currents and offset voltage are ± values given.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies only if the output current alternates between both output transistors at a rate faster than 60Hz.

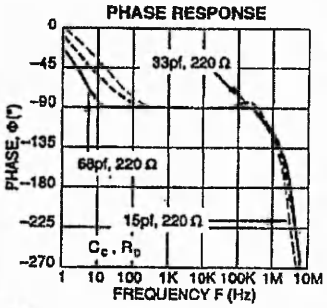
CAUTION The PA89 is constructed from MOSFET transistors. ESD handling procedures must be observed.

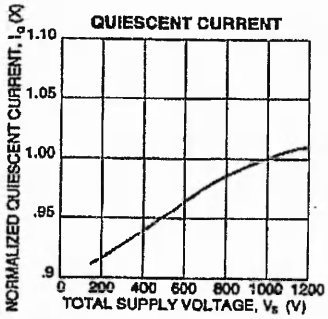
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

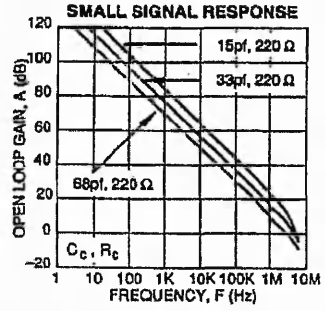
TYPICAL PERFORMANCE GRAPHS

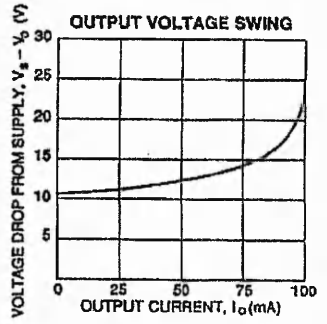
PA89 • PA89A

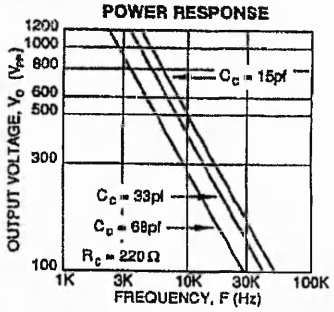


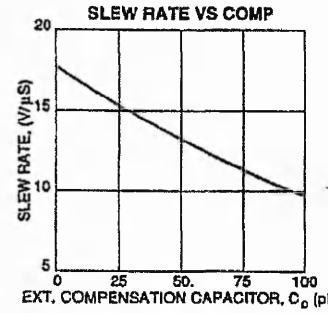


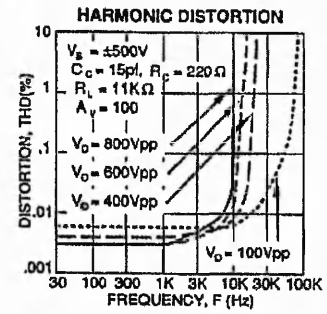


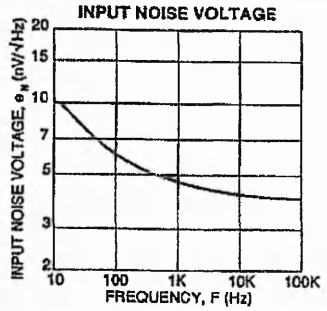


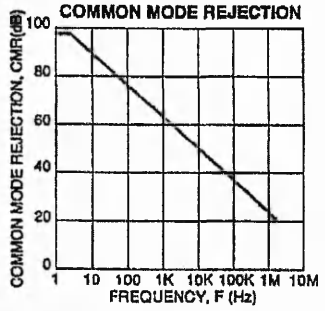


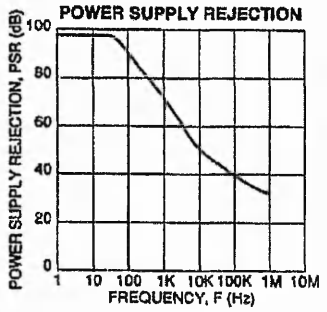


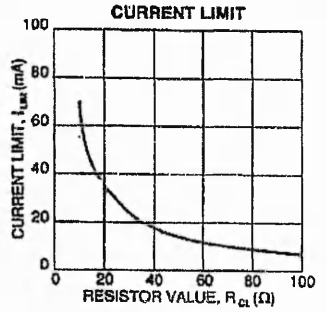












PA89 • PA89A

OPERATING CONSIDERATIONS

GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

STABILITY

Although the PA89 can be operated at unity gain, maximum slew rate and bandwidth performance was designed to be obtained at gains of 10 or more. Use the small signal response and phase response graphs as a guide. In applications where gains of less than 10 are required, use noise gain compensation to increase the phase margin of the application circuit as illustrated in the typical application drawing.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

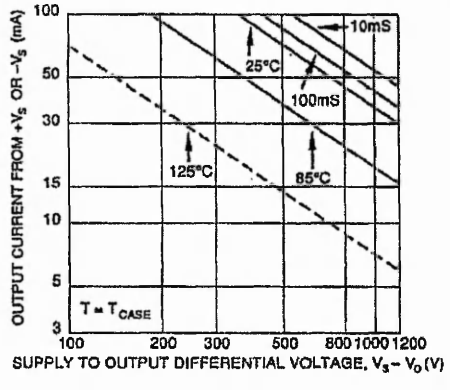
NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.

EXTERNAL COMPONENTS

The very high operating voltages of the PA89 demand consideration of two component specifications rarely of concern in building op amp circuits: voltage rating and voltage coefficient.



The compensation capacitance C_C must be rated for the full supply voltage range. For example, with supply voltages of ±500V the possible voltage swing across C_C is 1000V. In addition, a voltage coefficient less than 100PPM is recommended to maintain the capacitance variation to less than 5% for this example. It is strongly recommended to use the highest quality capacitor possible rated at least twice the total supply voltage range.

Of equal importance are the voltage rating and voltage coefficient of the gain setting resistances. Typical voltage ratings of low wattage resistors are 150 to 250V. In the above example 1000V could appear across the feedback resistor. This would require several resistors in series to obtain the proper voltage rating. Low voltage coefficient resistors will insure good gain linearity. The wattage rating of the feedback resistor is also of concern. A 1 megohm feedback resistor could easily develop 1 watt of power dissipation.

Though high voltage rated resistors can be obtained, a 1 megohm feedback resistor comprised of five 200Kohm, 1/4 watt metal film resistors in series will produce the proper voltage rating, voltage coefficient and wattage rating.

CURRENT LIMIT

For proper operation the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows with the maximum practical value of 150 ohms.

$$R_{CL} = \frac{.7}{I_{LIM}}$$

When setting the value for R_{CL} allow for the load current as well as the current in the feedback resistor. Also allow for the temperature coefficient of the current limit which is approximately -0.3% /°C of case temperature rise.

CAUTIONS

The operating voltages of the PA89 are potentially lethal. During circuit design, develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient absorbers are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

APPENDIX B

Pictures of Other Characterisation Systems

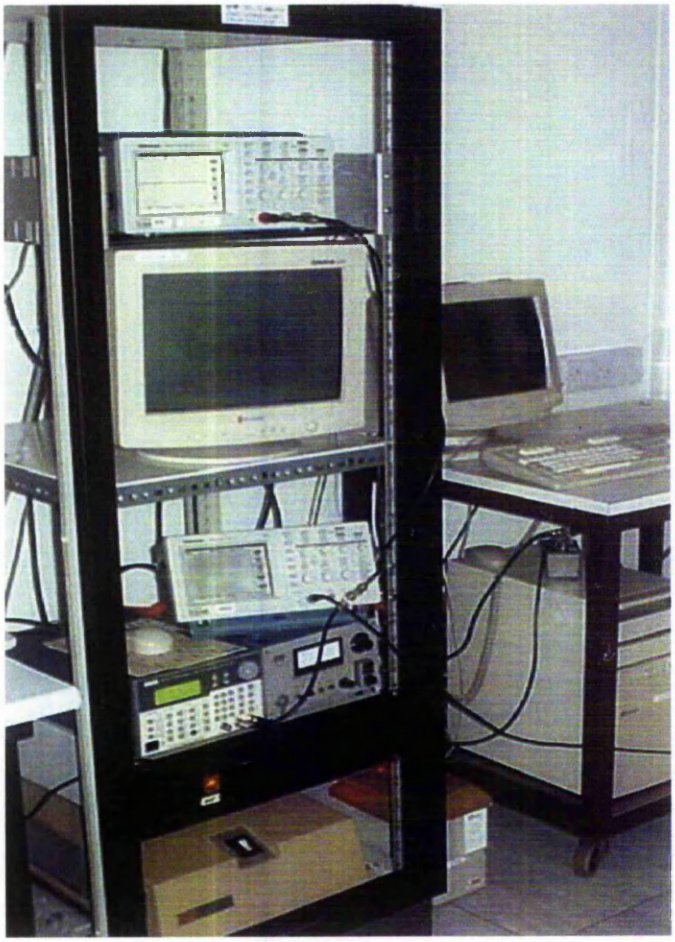


Figure B.1 Programmable control system utilised for the probe station described in Section 2.4.1 and the vacuum measurement unit described in Section 2.5.

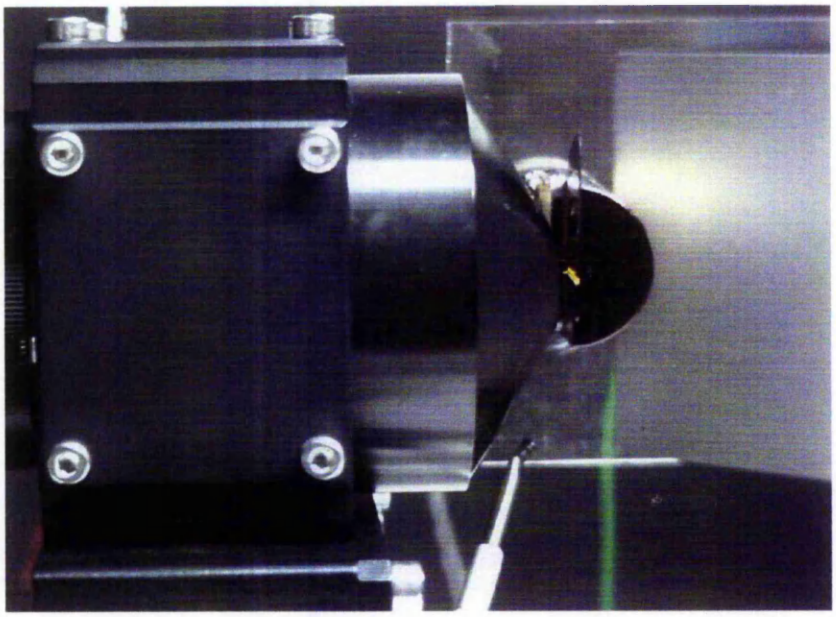


Figure B.2 Microscope attachment used in the Agema thermal imaging system described in Section 2.4.4 to image an active area of 1 mm diameter.

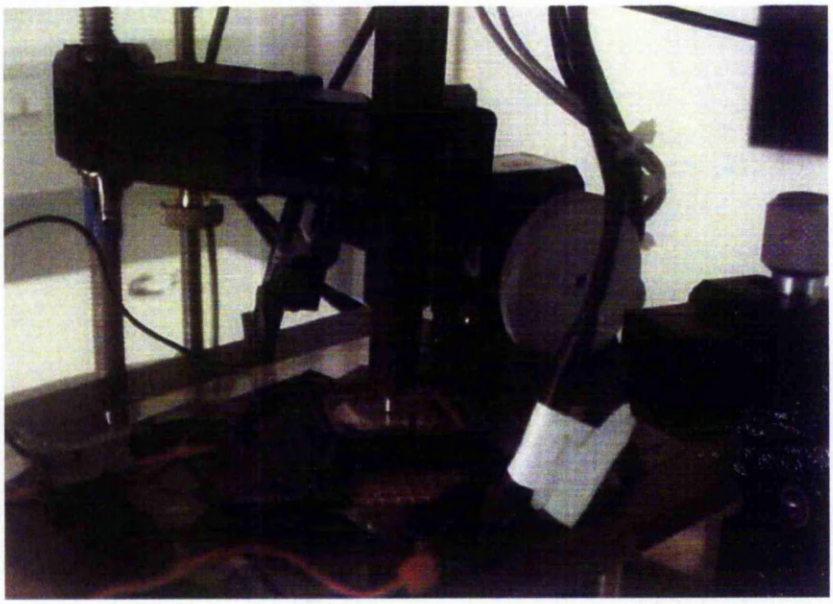


Figure B.3 The fibre optic measurement system for vertical out EL emission ACTFEL device.

APPENDIX C

Constants of Pure Yttrium Oxide Crystal

Yttrium Oxide Crystal could be fabricated utilising Flame Fusion Process

Physical Properties

Density	: 5.03 g/cm^2
Melting Point	: 2710 K
Molecular Weight	: 225.81 (amu)

Electrical Properties

Electrical Resistivity	: ~ 1 x 10^7 Ω/m @ 600°C

Thermal Properties

Thermal Conductivity	: 8 -12 W/m K @ 200 °C
Thermal Expansion Coeff.	: 8.1 X 10^{-6} m/m K

Structural Properties

Structure	: Body-Centered Cubic
Hexagonal Phase Change	: 2640 K
Unit Cell Length	: 1.0604 nm, which has 16 formula Units

Optical Properties

Bandgap	: 5.5 - 6 eV
Refractive Index	: 1.93 @ 555 nm

References

- Y. Nigara, Japanese J. App. Phy, 7 1968 Pg. 404
- F.Jollet, C. Noguera, N. Thromat, M. Gautier & J.P. Duraud, Physical Review B, American Physical Society 42, 12 1990, Pg. 7587
- B.H.O'Connor & T.M. Valentine, Acta Cryst. B25 1969 Pg. 2140
- W. J. Tropf, SPIE 1112, 1989 pg. 9
- http://www.cerac.com/pubs/proddata/y2o3.htm - 2002
- W.J. Troff and M.E. Thomas, Handbook of optical constant of solids II, Academic Press 1991 Pg. 1079
- http://www.webelements.com/webelements/compounds/text/Y/O3Y2-1314369.html - 2002

APPENDIX D

Pictures of Broken-down ACTFEL devices

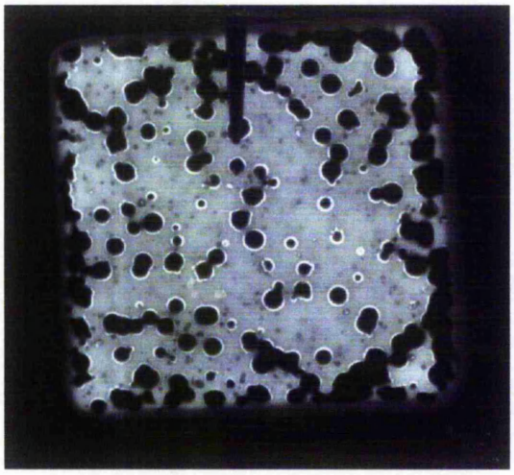


Figure D.1 ITO top electrode ACTFEL device with islands of non-active regions due to selective breakdown.

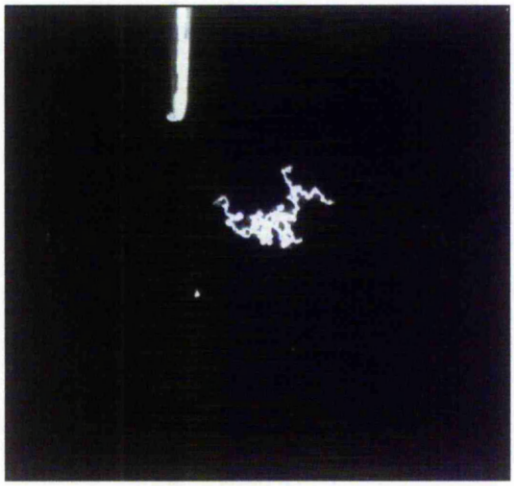


Figure D.2 ITO top electrode ACTFEL device completely broken down with snake like chain indicating the affected area due to high field.

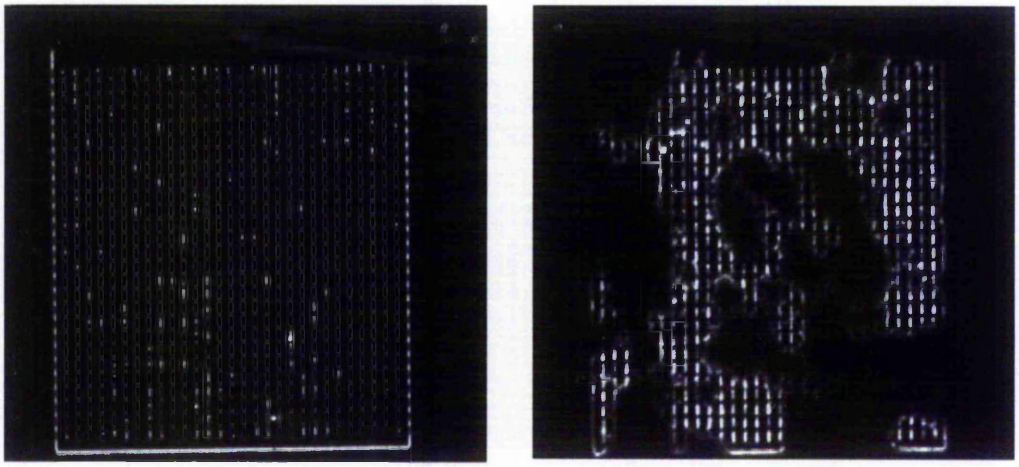


Figure D.3 Al top electrode ACTFEL device. left – a virgin device and right - with regions of selective breakdown.

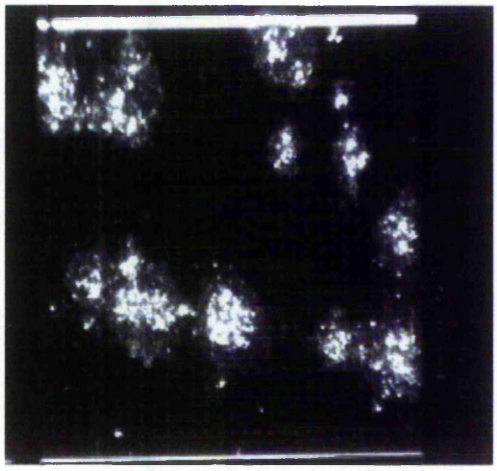


Figure D.4 Al top electrode ACTFEL device, showing peeling of the Al electrode layer after operating the device for 24 hours.

APPENDIX E

Labview Programs

1. **Luminance versus Voltage measurement - (LV)**
2. **Transferred Charge versus Voltage measurement - (QV)**
3. **Current versus Voltage measurement – (IV)**
4. **Transient Capture measurement – (TC)**
5. **Ageing with LV, Capacitances monitoring and Charge capture measurement – (AGE WTC)**
6. **Automatic voltage increase to compensate for luminance degradation with ageing time with LV, Capacitances monitoring and Charge capture measurement – (Vth Age)**

The following pages details the program subroutine hierarchy diagram for the measurements listed above.

Some of the Other Major Labview Programs Developed by the Author

7. **CCD camera image capture and integration program**
8. **Thin Film Capacitance as a function of Voltage measurement control program utilising HP 4192A, LF Impedance Analyser (Co. programmer: Dr. Costas Tsakonas)**
9. **Thin Film Current as a function of Voltage measurement control program utilising HP 4140B, Pico Ammeter (Co. programmer: Dr. Costas Tsakonas)**
10. **Capacitance monitoring of thin film during high field stressing measurement control utilising HP 4192A, LF Impedance Analyser**

Figure E.1 Luminance versus Voltage measurement subroutine hierarchy diagram - (LV)

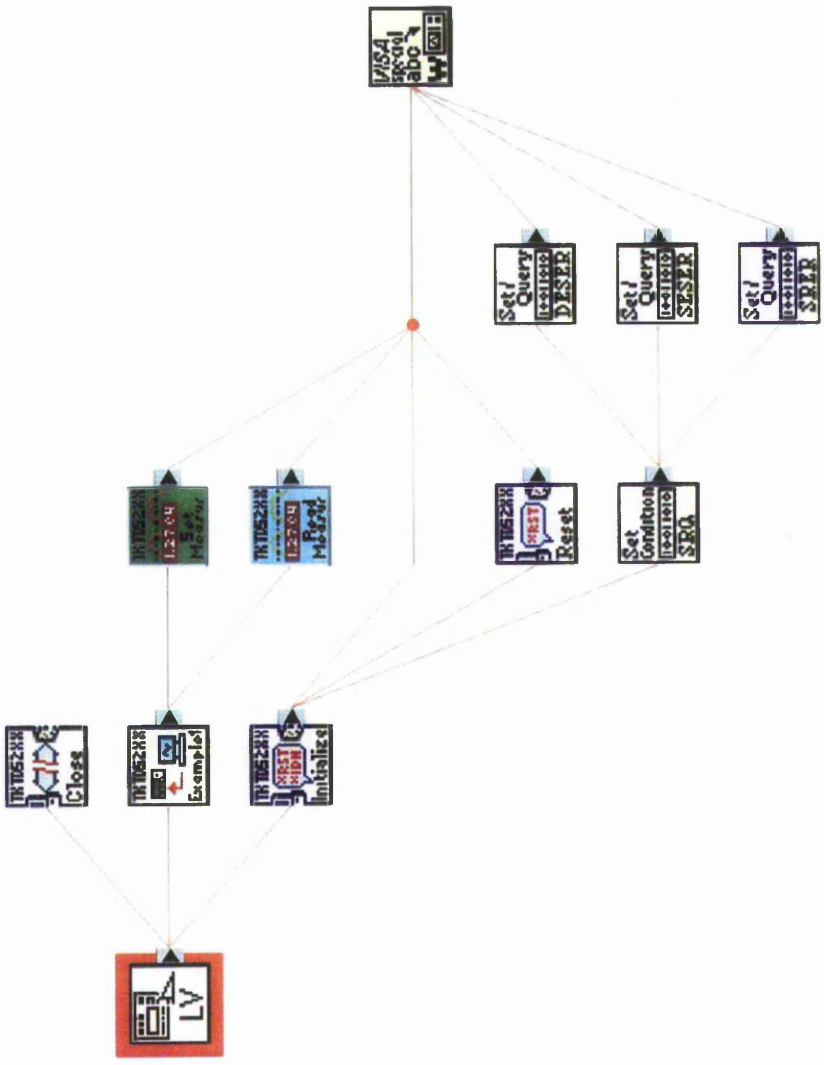


Figure E.2 Transferred Charge versus Voltage measurement subroutine hierarchy diagram - (QV)

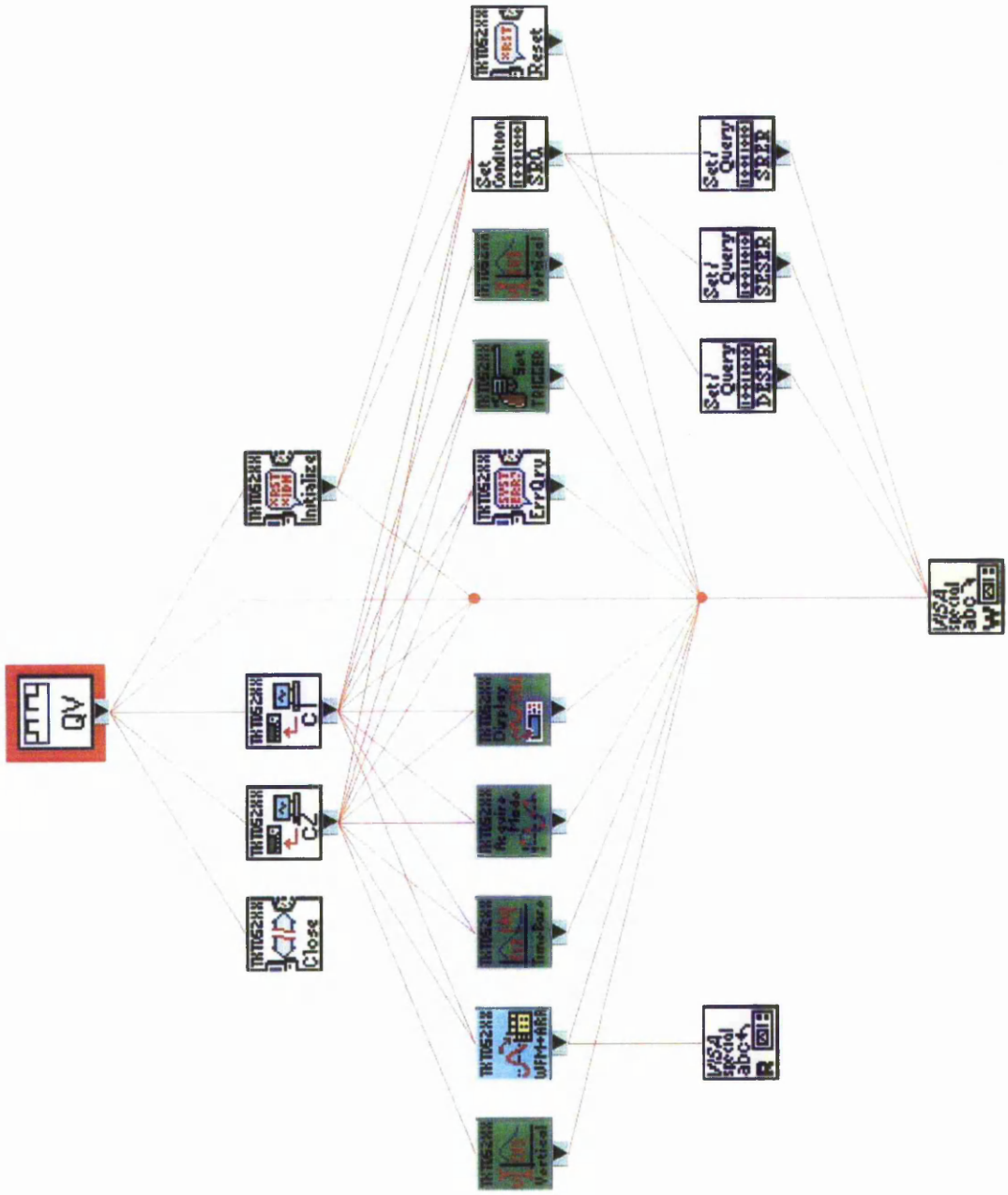


Figure E.3 Current versus Voltage measurement subroutine hierarchy diagram – (IV)

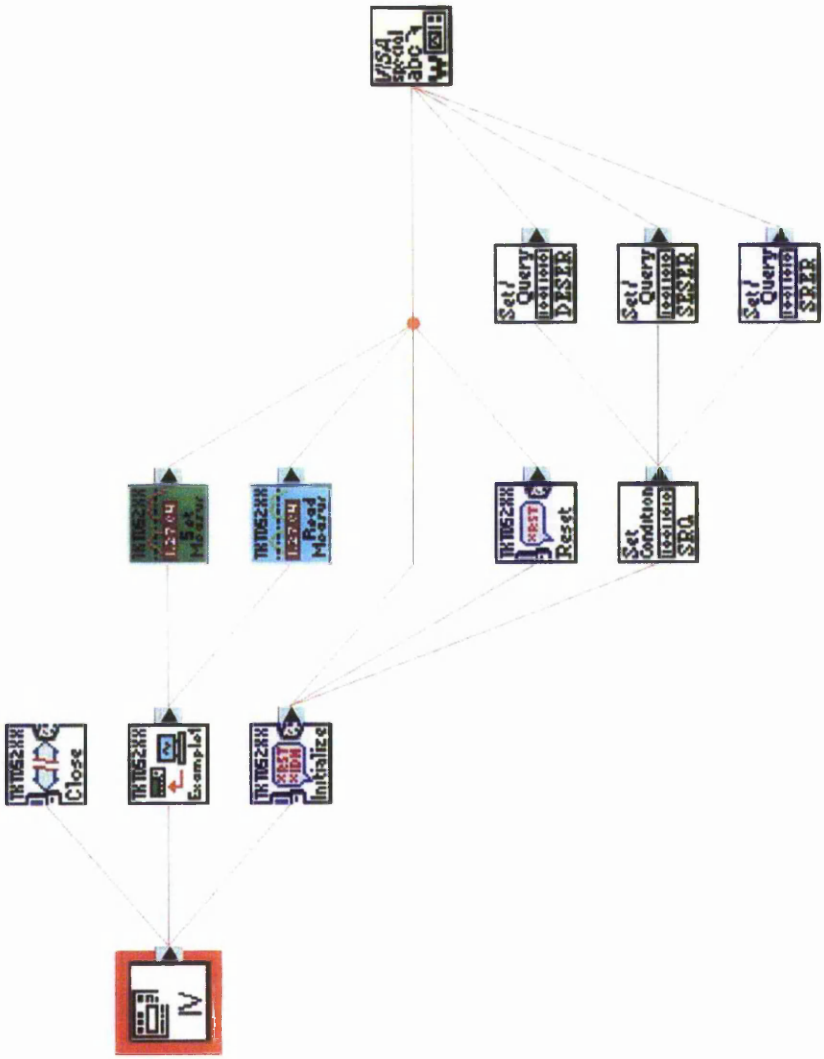


Figure E.4 Transient Capture measurement subroutine hierarchy diagram – (TC)

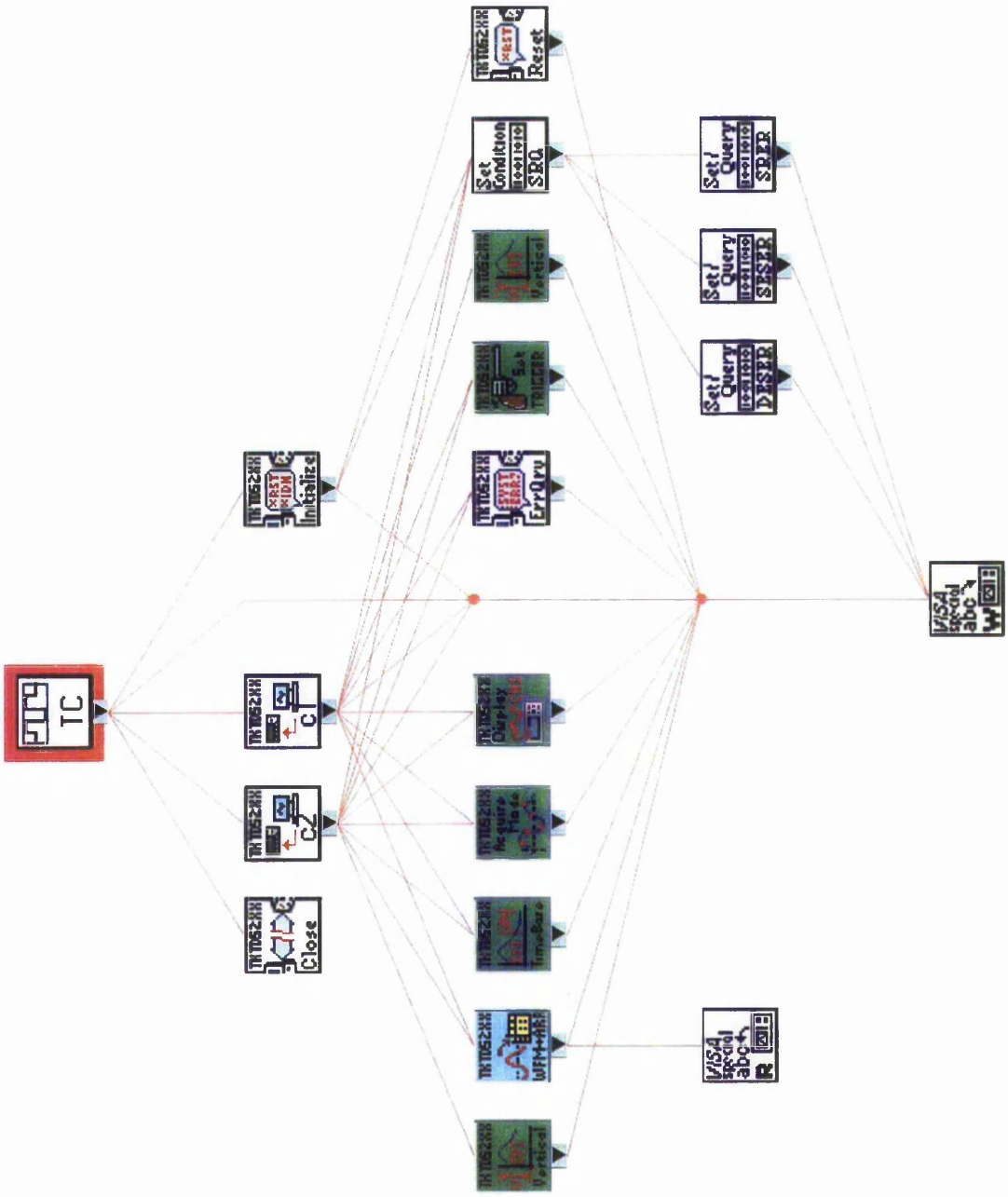


Figure E.5 Ageing with LV measurement subroutine hierarchy diagram – (AGE WTC)

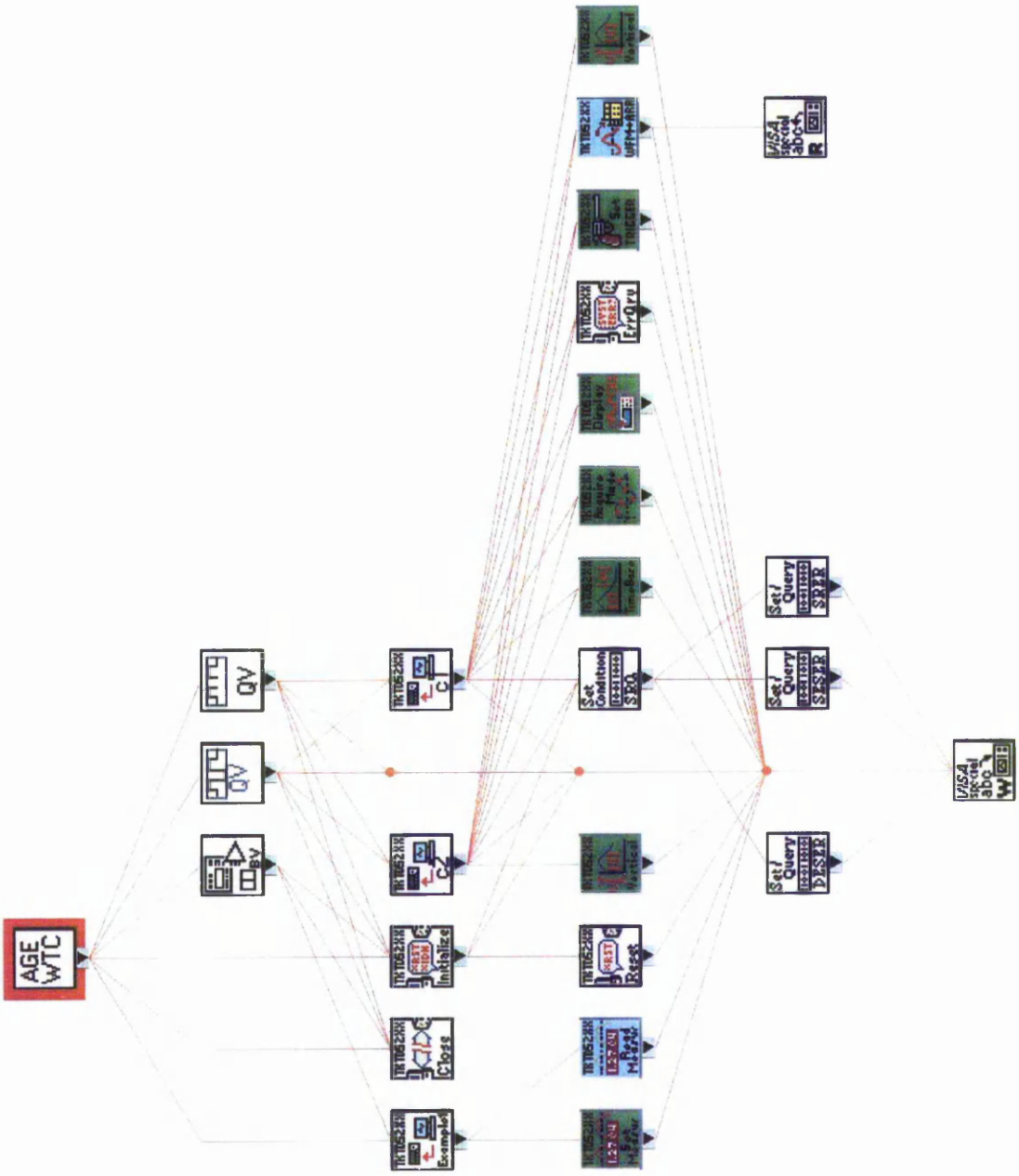


Figure E.6 Automatic voltage increase measurement subroutine hierarchy diagram – (Vth Age)