A Study of Dielectric Thin Film Materials for Display Applications

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Abstract

By advances in information and telecommunication technology (ICT), a display device is one of the most important information technologies. In particular, flat panel displays and technologies have been considered as the centre of a next generation engine in society, academia, business, and other communities.

This thesis is based on an inorganic alternative current thin film electroluminescent (ACTFEL) device which is one of the flat panel display technologies. Investigation of electrical and dielectric properties of $Ba_{0.5}Sr_{0.5}TiO_3$ (BST) thin film to enhance device stability and reduce a driving voltage of the TFEL device was carried out. In addition, yttrium oxide dielectric thin film, yellow emitting ZnS:Mn and blue emitting SrS:Cu,Ag phosphors are also discussed. These thin films and TFEL devices were fabricated by rf-magnetron sputtering method except for the aluminium(Al) electrode, which was deposited by thermal evaporation.

Various characterisations techniques were applied to the candidate dielectric thin films and the EL devices. These were performed by fabricating Metal-Insulator-Semiconductor (MIS) capacitors and lateral- and surface emitting- TFEL devices, respectively. Meanwhile, materials and device engineering included laser annealing and barrier layers were utilised.

In this study the optimum growth conditions for rf-sputtered barium strontium titanate (BST) thin films were established. The substrate temperature, sputtering pressure, oxygen ratio, and rf power were 300 to 350 °C, 10 mTorr, 10% O_2 mixture, and 100 watts, respectively. Also, it is found that an additional post-annealing process was necessary to improve BST thin films. Thus, BST thin films prepared in the optimum conditions showed a high dielectric constant of 32.4 and a high breakdown field of 8 MV/cm. Thus, the charge storage capacity of 100 nm-thick BST thin films is as high as 22.95 $\mu C/cm^2$, which is 8 times larger than the minimum requirement of charge storage capacity in selecting candidate dielectric material.

Leakage current was as low as 1. 58 $\mu A/cm^2$ at 80 V. In device structures, $Ba_xSr_{1-x}TiO_3$ (BST)/ZnS:Mn/Y_2O_3 EL devices exhibited far better performance in turn-on characteristics, luminance and device stability compared to other $Ba_xSr_{1-x}TiO_3$(BST)/ZnS:Mn/ $Ba_xSr_{1-x}TiO_3$ (BST) and Y_2O_3/ZnS:Mn/Y_2O_3 EL devices.

For blue emitting SrS:Cu,Ag EL devices, the device performance had a high correlation with barrier layer thickness. A 10 nm-thick barrier layer and 5-laser pulse at 1.8 J/cm^2 laser annealing process were the optimum conditions for the barrier layers. Meanwhile, high laser fluence (> 2.0 J/cm^2) may cause a "laser ablation" effect on the surface of the samples and as a result, a lower performance was observed. Therefore, overall improvement of EL emission could be achieved by combination of the device and materials engineering.

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List of Abbreviations

4-TP	4-Terminal Pair
A	Ampere
Å	Angstrom (10^{-8} cm or 10^{-10} m)
ABO_3	Perovskite Structure Material such as $BaTiO_3$ and $SrTiO_3$
AC, ac	Alternating Current
AD, A-D	Analog-to-Digital
ACTFEL	Alternating Current Thin Film Electroluminescent
AES	Alkaline-Earth Sulphide
Ag	Silver
Al_2O_3, Al_xO_3	Aluminium Oxide
Al	Aluminium
APCVD	Atmospheric Pressure Chemical Vapour Deposition
ALD	Atomic Layer Deposition
ALE	Atomic Layer Epitaxy
Ar	Argon
ArF	Argon Fluoride
a.u.	Arbitrary Units
Au	Gold
β_{PF}	A Poole-Frenkel emission coefficient
$Ba_xSr_{1-x}TiO_3$	Barium Strontium Titanate
$BaTiO_3$	Barium Titanate
BL	Barrier Layer
BLU	Back-Light Unit
BSD	Ballistic-electron Surface-emitter Display
BST	Barium Strontium Titanate
BT	Barium Titanate
BV, *B-V*	Brightness versus Voltage (= *L-V* or *LV*)
BZB	Barium Strontium Oxide/ZnS:Mn/Barium Strontium Oxide
BZY	Barium Strontium Oxide/ZnS:Mn/Yttrium Oxide
°C	Degree Celsius

Continued (List of Abbreviations)

CRT	Cathode Ray Tube
CCD	Charge Coupled Device
Ce	Cerium
CDT	Cambridge Display Technology
CL	Cathodoluminescene
CMOS	Compliment Metal-Oxide Semiconductor
CN	Chiral Nematic (or Cholesteric)
CNT	Carbon-Nano Tube
CSC, c.s.c	Charge Storage Capacity (or Figure of Merit)
Cr	Chromium
Cu	Copper
CV, *C-V*	Capacitance versus Voltage
CVD	Chemical Vapour Deposition
DAQ	Data Acquisition
DC, dc	Direct Current
DLC	Diamond-Like Carbon
DLP	Digital Light Processing
DMD	Digital Micromirror Device
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
EIL	Electron Injection Layer
EL	Electroluminescence
EML	Emitting Layer
EOT	Effective Oxide Thickness
EPD	Electronic Paper Display
ETL	Electron Transfer Layer
eV	Electron-Volts (= 6.242×10^{18} Joule)
FED	Field Emission Display or Field Emission Device
FET	Field Effect Transistor
FLCD	Ferroelectric Liquid Crystal Display

Continued (List of Abbreviations)

FOM	Figure of Merit (see CSC)
FWHM	Full Width Half Maximum
GLV	Grating Light Valve
GaN	Gallium Nitride
GaN:Eu	Europium doped Gallium Nitride
GPIB	General Purpose Interface Bus
He-Cd	Helium-Cadmium
HD	High Definition
HDPCVD	High Density Plasma Chemical Vapour Deposition
HDTV	High Definition Television
HIL	Hole Injection Layer
High-κ	High Dielectric Constant or materials
HMD	Head-Mounted Display
HTL	Hole Transfer Layer
HUD	Head-Up Display
IC	Integrated Circuit
ICBM	Ion Cluster Beam Deposition
IrO2	Iridium Oxide
IV, *I-V*	Current (Current density) versus Voltage
ITO	Indium Tin Oxide
k	Boltzmann constant
K	Degree Kelvin
KrF	Krypton Fluoride (for an excimer laser)
LPCVD	Low Pressure Chemical Vapour Deposition
$LaAlO_3$	Lanthanum Aluminium Oxide
$La_xSr_{1-x}CoO_3$	Lanthanum Strontium Cobalt Oxide
LA	Laser Annealing

Continued (List of Abbreviations)

LASER, laser	Light Amplification by Stimulated Emission of Radiation
LC	Liquid Crystal
LCD	Liquid Crystal Display or Liquid Crystal Device
LCoS	Liquid Crystal on Silicon
LD	Laser Diode
LETFEL	Laterally Emitting Thin Film Electroluminescent
L/HTPS	Low/High Temperature Poly-Silicon
LV, *L-V*	Luminance versus Voltage
MBE	Molecule Beam Epitaxy
MEMS	Micro-Electro-Mechanical System or simply Micromachining
MFC	Mass Flow Controller
MIS	Metal-Insulator-Semiconductor
MIM	Metal-Insulator-Metal
MISIM	Metal-Insulator-Semiconductor-Insulator-Metal
MOCVD	Metal-Organic (Organo-metallic) Chemical Vapour Deposition
MOS	Metal-Oxide-Semiconductor
Mn	Manganese
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
nm	nano metre (10^{-9} m)
NT	Nano (-scale) Technology
NTU	Nottingham Trent University
O_2	Oxygen
OEL	Organic Electroluminescence
OLED	Organic Light Emitting Diode
pA	Pico Ammeter, or Pico Ampere (10^{-12} Ampere)
Pb	Lead
PC	Personal Computer
Pd	Palladium
PECVD	Plasma Enhanced Chemical Vapour Deposition
P-F	Poole-Frenkel

Continued (List of Abbreviations)

PL	Photoluminescence
PLA	Pulsed Laser Annealing
PLD	Pulsed Laser Deposition
pk-pk	Peak-to-Peak
PMT	Photo-Multiplier Tube
PPI, ppi	Pixels per inch
Pt	Platinum
PVD	Physical Vapour Deposition
RF, rf, r.f.	Radio Frequency
QV, *Q-V*	Charge versus Voltage
RTA	Rapid Thermal Annealing
RTP	Rapid Thermal Annealing Process
RuO_x	Ruthenium Oxide
SEM	Scanning Electron Microscopy
S	Sulphur
SED	Surface-conduction Electron-emitter Display
Si	Silicon
SID	Society of Information Display
Si_3N_4, Si_xN_y	Silicon Nitride
SiO2, SiO_x	Silicon Dioxide, Silicon Oxide
SiO_xN_y	Silicon Oxynitride
SOI	Silicon on Insulator
SRAM	Static Random Access Memory
SrS	Strontium Sulphide
SrS:Ce	Cerium doped Strontium Sulphide
SrS:Cu	Copper doped Strontium Sulphide
SrS:Cu,Ag	Copper and Silver doped Strontium Sulphide
ST	Strontium Titanate
$SrTiO_3$	Strontium Titanate
STN	Super-Twisted Nematic

Continued (List of Abbreviations)

Ta_2O_5	Tantalum Oxide
TDEL	Thick Dielectric-layer Electroluminescent
TFEL	Thin Film Electroluminescent
TFT	Thin Film Transistor
Ti	Titanium
TN	Twisted Nematic
UPS	Uninterruptible Power Supply
UV	Ultra Violet
wt%	Weight percentage
XRD	X-ray Diffraction
XZ	X and Z direction
Y	Yttrium
Y_2O_3	Yttrium Oxide
YZY	Yttrium Oxide/ZnS:Mn/Yttrium Oxide
ZnS	Zinc Sulphide
ZnS:Mn	Manganese doped Zinc Sulphide

List of Symbols and Variables

Å	Angstrom (10^{-10} m or 10^{-8} m)
A	Area
a, c	Lattice constants (for cubic or hexagonal structures)
χ_e	Electric susceptibility
χ_m	Electron Affinity (m = material)
χ'_m	Modified Electron Affinity (m = material)
β_{PF}	Poole-Frenkel coefficient
c	Speed of light
C	Capacitance (F) or Capacitance per unit area (F/cm^2)
C	Curie Temperature (T_c)
cm	Centimetre
C_{acc}, C_{ACC}	Capacitance at Accumulation condition
C_{BST}	Capacitance of BST thin film at Accumulation (from C-V)
cd	Candela
cd/m^2	Candela per square metre
C_{FB}	Capacitance at flatband condition
C_i	Insulator Capacitance
C_{inv}	Capacitance at inversion condition
C_{min}	Minimum Capacitance (at inversion condition)
C_{oxide}	Oxide Capacitance
C_{total}	Total Capacitance of MIS capacitor
C_p	Phosphor Capacitance
C_{se}	Capacitance of Sensing Capacitor
C_T	Total Capacitance of series connected capacitors
d, t	Thickness
d_{hkl}	Plane Spacing or d-spacing
D	Electric Displacement Density
D_{it}	Interface Charge State Density
Δ	Change (such as Voltage drop or Potential Drop)

Continued (List of Symbols and Variables)

ΔC	Change in Capacitance
ΔV	Change in Voltage
ε^*	Complex Permittivity (= $\varepsilon' - j\varepsilon''$)
$\varepsilon_{r,}$	Relative permittivity or relative dielectric constant
$\varepsilon_{o,}$	Permittivity in Vacuum
ε_s	Semiconductor dielectric constant
$E, \mathcal{E}$	Electric Field
E_{BD}	Breakdown Strength Field
E_c	Lowest Energy Level in Conduction Band
E_i	Intrinsic Fermi Level at thermal equilibrium
$E_{i(bulk)}$	Fermi Level in Bulk region
E_{FS}	Fermi Level of Silicon
E_{Fm}	Metal Fermi Level
E_{Fn}	n-type Semiconductor Fermi Level
E_v	Highest Energy Level in Valence Band
F	Farad
F_p	Electric field across Phosphor layer
γ	Charge distribution factor
G	Conductance
h	Plank's constant
h, k, l	Miller indices
i	Current
k	Boltzmann constant
κ_s	Permittivity of Silicon
κ'	Relative Permittivity of material (=$\varepsilon_{r,}$)
kHz	Kilo Hertz
λ	Wavelength
L_B	Extrinsic *Debye Length*
L_D	Intrinsic *Debye Length*

Continued (List of Symbols and Variables)

μ	Electric dipole moment
μ	micro (10^{-6})
mm	millimetre
MHz	Mega Hertz
MV	Mega Volt
η	Luminous efficiency
n	Refractive index
n	Electron concentration (cm^{-3})
n_i	Intrinsic Silicon carrier concentration
N_d	Acceptor Carrier Density (#/cm^3)
N_d	Donor Carrier Density (#/cm^3)
N_f	Fixed Oxide Charge Density
p	Hole concentration (cm^{-3})
P	Dipole Moment
ρ	Charge density (p-n junction)
q	Electron or proton unit charge
Q	Charge
$Q(t)$, $q(t)$	instantaneous charge
Q^{ext}	External Charge
Q^{int}	Internal Charge
Q^{ss}	Interface Charge Density
Q_f	Fixed Oxide Charge
Q_{it}	Interface State Charge
Q_{ot}	Oxide Trap Charge
ϕ_m	Metal work function (V)
ϕ_{ms}	Work function difference between metal and semiconductor
ϕ_s	Surface potential
ϕ_B	Bulk Potential difference between Fermi Levels (E_{FS}-$E_{i(bulk)}$)
σ	Conductivity or standard deviation
θ	Angle
t	Crystallite size

Continued (List of Symbols and Variables)

T	Temperature (K)
T_c	Curie Temperature
T_o	Curie-Weiss Temperature
ν	Frequency (= c/λ)
v	Voltage(ac)
V	Voltage (ac + dc, or dc only)
V_{BD}	Breakdown Voltage
V_G	Gate Bias
V_i	Voltage across the insulator
V_{th}	Threshold Voltage
$V_{th(z)}$	Phosphor Threshold Voltage
ω	Angular frequency (= $2\pi f$)
W_{max}	Maximum Depletion Width
W	Depletion Width

Chapter 1 Introduction

Overview

This chapter begins by discussing the current situation in flat panel display technologies: various electronic information display formats, the social and technical impact on our society and technical progress. The first and second sections of this chapter introduce a summary of economical and technical advantages and difficulties in the major flat panel display technologies including an electroluminescent display. The purpose of the comparison table is to provide background knowledge of display technologies, as well as a starting point to be extended in detail later. Finally, the aims, objectives and structures of the thesis are outlined.

1.1 Current situation in flat panel displays and information technologies

Through advances in information technology, material engineering technology, nanotechnology and biotechnology, our lives in 2015 will be revolutionized by the growing effect of these multidisciplinary technologies across all dimensions of life: social, economic, political and personal[1]. In particular, advances in nano-, material- and information technologies are combining to enable semiconductor devices and integrated microelectronic systems with potential global effects on individual and the public. In many cases, the significance of these technologies appears to depend on the synergies afforded by their combined advances as well as on their interaction with the so-called information revolution. The emerging technology revolution with ongoing information technology can open up possibilities for increased economic prosperity and quality of life regardless of time and place [1].

It is well known that semiconductor devices and their fabrication technologies have had a powerful impact and wide range of usage so that they affect the entire range of the industry. In particular, the multidisciplinary semiconductor technology can possibly produce products, components and systems that are smaller, smarter, multi-functional, environment-friendly, more robust and customizable. These products will not only contribute to the growing revolutions of information but will have additional effects on manufacturing, logistics and personal lifestyles [1].

A display device is one of the most important information technologies and at the same time the field is highly multidisciplinary combining chemistry, physics, materials science and electronics. More specifically, a flat-panel display(FPD) with information and communication/tele-communication technology(ICT) have been considered as a core strategic technology in many major countries and research activities have been undertaken actively in university research laboratories, companies and other private or government research institutes all over the world since late '80s [9].

During the past 20 years there has been unprecedented growth in various electronic information display technologies such as cathode-ray tubes(CRTs), vacuum florescence displays(VFDs), field-emission displays(FEDs), inorganic electroluminescent display(ELDs), plasma display panels(PDPs), inorganic/organic light-emitting diodes(LEDs), digital micromirror displays(DMDs), liquid crystal displays(LCDs), Electronic paper(ie., E-ink) and so on[2,3,4,5,6,7,8,9]. Among them, thanks to rapid developments in personal computers, telecommunication and the internet, flat-panel display devices are becoming much more important economically, socially and politically. We can see tremendous impact and benefit at home, offices, schools and virtually everywhere as end-users and researchers. These flat panel display devices (or technologies) are more energy efficient, lighter and thinner compared to conventional cathode-ray tubes[10], which have been used on our desktops widely until now. A summary of the important advantages and difficulties that most flat panel display technologies possess are presented briefly in Table 1-1[11]. The cathode-ray tubes (CRTs) are included in that table for comparison purpose.

Liquid crystal display technology has overcome some of the problems of conventional† CRTs - weight, volume, power consumption and electromagnetic wave compatible/interference (EMC/EMI) issues. They have replaced the position of CRTs dramatically in the display market, particularly, in computer monitors, small and medium-size TV applications and have facilitated personal portable devices such as mobile phones, MP3 players, DVD players and so on. The LCD displays are the dominant player in the flat-panel display devices. However, LCD systems have several fundamental drawbacks, including being a non self-luminous - non-emissive - system, limited operating temperature, relatively slow

† Conventional means a bulky cathode-ray tubes(CRTs) in order to avoid ambiguity in its meaning. Currently slim CRTs are developed and available to the public. The overall width of desktop slim CRTs is comparable with that of desktop LCD TVs or monitors.

response time, high power consumption due to a back light, non-full solid state device. Thus, various research attempts have been made to find alternative device technologies to replace LCDs and to provide better flat panel displays for general and specific purpose display sectors.

As a result, considerable interest has been placed in thin film electroluminescence displays (TFELD) for some time, even though EL devices were not the best solution to replace LCDs and CRTs. In terms of device performance, the alternating-current thin film electroluminescence (ACTFEL) device was potentially a good competitor to the cathode-ray tubes. It has many advantages in brightness, fast response time, wide viewangle, long lifetime, wide range of operating temperature and is a full solid-state device.[12,18] However, the electroluminescent devices have drawbacks in high-driving voltages, and difficulties with defining a suitable blue-phosphor material for full-colour devices [12,18,19].

Table 1-1. Display Technologies: advantages, disadvatanges, and typical applications[11]

Display Technologies		Advantages	Difficulites	Typical Applications
Liquid Crystal Displays (LCDs)	Passive Matrix (PM)	mature cheap flexible substrate possible	switching speed contrast graphics non-emissive effectiveness temperature range	broad range of small displays (e.g. mobile phones and automotive applications)
	Active Matrix (AM)	mature and video-capable many technical options minimum pixel size: 15 μm(reflective type) 50 μm(transmissive type) flexible substrate possible	non-emissive effectiveness low yield for production of large huge capital investment necessary temperature range	Computer Monitors, Laptops, TVs, full colour navigation devices HDTV lauch
Plasma Display Panels (PDPs)		emissive simple construction video-capable robust large size	complicated driving scheme weight power consumption contrast minimum pixel size 300 μm expensive	HDTVs Information Systems for publics (e.g. pubic transportations, billboards, outdoor signposts, etc.)
Vacuum Flourescence Displays (VFDs)		emissive mature brightness temperature range	high voltage necessary full colour and graphics power consumption installation depth	low information contents displays for audio and video devices, household applications
Electroluminescent (EL)	Inorganic EL	emissive device simple device structure, robust thin, lightweight minimum pixel size - only few mm transparent flexible substrate possible easy production	high AC voltage necessary limited colour range brightness effectiveness large size displays hard to realize	Backlight units for LCD & mobile phone keypad Passenger information systems in German High Speed Train(ICE), Specific-purpose equipments (e.g. military and medical devices) in the past
	Inorganic Light-Emitting Diodes (LEDs)	emissive device mature brightness lifetime, robust easy production	graphics pixel size	Outdoor applications like large-sized video screens, tickers Traffic Information Systems and traffic signals
	Organic LEDs	emissive device brightness video-capable thin, lightweight minimum pixel size few μm flexible substrate possible	lifetime <> colours extensive encapsulation current driven	Potential broad range from large area lighting, backlight to full-colour video displays microdisplays market lauch with car audios and mobile phones
Field Emission Displays (FEDs)		emissive device large view angle temperature range video-capable minimum pixel size few 10 μm effectiveness	high voltage necessary vacuum full colour liftime low production yield	Possible applications: ruggedised displays automotive aviation
Digital Mirror Displays (DMDs)		brightness, contrast, and compact colour reproduction	expensive and non-emissive fabrication process and production	Projection TVs Presentation equipments
Electronic-Ink(E-Ink) Electronic Paper		power conusmption(bistable) contrast cheap and large size flexible, thin, lightweight	black and white or two-colour only switching speed non-emissive	Possible applications: electronic newspapers and price tags, and large scale advertisement
Cathod Ray Tubes (CRTs)	Conventional	mature in production and technology contrast, brightness, and full-colour emissive and response speed cheap and long lifetime	EMI/EMC heavy, Volume high AC voltage necessary not portable	Broad range of dispalys - TVs, Monitors
	Slim(thin) CRTs	holding conventional features reduced weight and volume size	not portable, high AC voltage need	Potential large demand for TVs and desktop monitors

1.2 Luminescent Displays

In 1936, the French scientist, Destriau[13] observed the luminescence phenomenon from applying an electric field to ZnS compounds. This experiment was considered the first demonstration of electroluminescence. Although the electroluminescent (EL) phenomenon was known to the world after that, there was no real achievement in EL until a viable transparent electrode - ITO(Indium Tin Oxide, Sn doped-In_2O_3) was developed. In 1974, the Japanese scientist Inoguchi[14] developed an excellent and stable thin film electroluminescent(TFEL) display device which was demonstrated at the Society for Information Display(SID) symposium. After this, EL technology and research activity became a subject of intense study in terms of the physics and engineering of TFEL devices. Meanwhile other display devices have been emerging as new contenders: liquid crystal displays (LCDs), plasma displays(PDPs), field emission displays(FEDs) and more recently organic light-emitting diodes and EL displays(OLEDs)[15].

In luminescence, commonly there are three types of mechanisms in a solid: electroluminescence (EL), photoluminescence (PL) and cathodoluminescence (CL)[16]. Literally, electroluminescence has a relatively simple definition in meaning. EL phenomenon is basically initiated by an electric field. Often electroluminescence (EL) is classified into two types: low electric field EL and high electric field EL. EL by high electric field is the process in inorganic TFEL devices, while the light emitting diode (LED) devices are operated in low electric field. Low field EL (i.e., LED) is also called "*injection* EL"[13,17,18] due to the mechanism relying on the injection of charge carriers.

There are two factors that distinguish the difference between LED and EL devices: one is that LEDs are based on a p-n junction, but TFEL devices have a Schottky barrier structure, or metal-semiconductor structure [17]. In other words, LED devices have two carriers - electrons and holes, but EL devices have only majority carriers – electrons [18]. As mentioned above, the other factor is the magnitude of applied electric fields. An LED is operated with high-current at low voltage, but EL devices use low-current at high voltage [17]. If one thing could be added, interestingly, EL devices should have dopant(s)-doped semiconducting phosphor layer(s), while there is no actual phosphor layer within most LED devices.

In flat panel display technologies (FPDs) and the commercial market, the survival game of the various technologies has become much more tough and competitive. Recently, organic EL display devices have been developed successfully and rapidly so that it is now necessary to mention whether the EL devices are inorganic or not. Inorganic TFEL devices have been known for having many advantages since they have full solid state characteristics, hence inorganic EL device was previously treated as one of the promising next-generation display technologies. Now, however, because other flat panel displays show better performance than inorganic TFEL devices in general-purpose display markets, the interest for inorganic TFEL devices is reducing. One of the reasons is that inorganic TFEL devices have been suffering from the lack of blue phosphor materials, resulting in a development delay of full-colour TFEL devices. Although Planar, Sharp and iFire provided a prototype full-colour device, the full colour TFEL panels are of limited availability commercially. In addition, TFEL devices are operated by a high electric field, so the driving voltage is high and the expensive cost of driver circuits became one of the technical obstacles.

Through many efforts to develop blue phosphor materials and reduce driving voltage for TFEL devices in many countries, there is the opportunity to improve performance, colour gamut, stability, brightness, efficiency and driving voltage of TFEL devices. New phosphor materials for blue phosphor such as SrS:Cu,Ag have been investigated since Sun's work[19]. In order to enhance performance, stability and brightness of EL devices, the barrier layer structure[20] and pulsed laser annealing[21,22] treatment has been introduced and utilized in the experiments for this thesis. At the same time, blue EL devices have been realised using SrS:Cu,Ag phosphor materials. It was already known that the barrier layers in the middle of phosphor layers (II_B-VI_B ZnS:Mn phosphor) in EL devices had positive effects on brightness and efficiency in EL emission[20]. Also, pulsed laser annealing treatment as a material engineering technique has been demonstrated. In particular, pulsed laser annealing treatment to phosphor materials has offered good opportunities to improve performance of EL devices [22,23].

Of major significance, the stability and lifetime in operation and performance of the device greatly depend on insulating layers because the dielectric constant and dielectric breakdown strength of the insulating layers are affecting stable operation and efficiency of the devices. Thus, the choice of an appropriate insulating material is critical to guarantee the device's stable operation. Therefore, in order to reduce the driving voltage, perovskite-structure (ABO_3)

ferroelectric oxides[24] will be good candidate materials due to their high dielectric constant. In particular, barium strontium titanate[$Ba_xSr_{1-x}TiO_3$] thin films are one of next-generation dielectrics and are becoming more important in dynamic random-access memories (DRAMs)[25], ferroelectric-based random-access memories (FeRAMs)[26], gate oxide in compensate metal-oxide-semiconductor (CMOS)[25,27] and other microwave and wireless applications[5,6,28] due to high dielectric constant, good structural stability properties and low dielectric loss. In fact, the materials are currently widely used or studied elsewhere. However, this dielectric has not commonly been used for the insulating layers of TFEL devices, in which high dielectric material or thin film is more than necessary. Thus, in this study, the structural and electrical properties of barium strontium titanate thin films grown by rf magnetron sputtering technique were investigated and luminescence properties of full EL devices with $Ba_xSr_{1-x}TiO_3$ thin film layers are examined.

1.3 Aims and Objectives

Aims:

The major aims of the study are to investigate the effect of the dielectric layer on the optimization of blue-emitting TFEL devices. Research activities are intended to investigate high-κ perovskite-format ferroelectric insulating layer - barium strontium titanate [$(Ba,Sr)TiO_3$] - for enhanced stability and performance of ACTFEL devices.

Objectives:

1. Investigate and optimize the luminescence properties of Cu and Ag co-doped strontium sulphide - SrS:Cu, Ag - as a blue phosphor materials using PL and EL characterisations.

2. Investigate the feasibility of improving brightness of the EL devices using barrier layers and laser annealing effects by comparing to TFEL device without barrier layers and pulsed laser treatment.

3. Characterise the structural, dielectric and electrical properties of perovskite barium strontium titanate thin films and investigate the feasibility of using this materials to lower the turn-on voltage, increasing stability and brightness in TFEL devices.

4. Study the luminescence mechanism to enhance understanding of the blue emitting TFEL device.

The thesis consists of seven chapters:

Chapter 1 is a brief introduction of the flat panel display, inorganic TFEL devices and the current situation of the information technologies. The aims and objectives of the research program are presented.

In Chapter 2, the main topics are a literature review and background study of inorganic TFEL devices and other general display devices/technologies. Inorganic ACTFEL technologies, dielectrics and blue phosphor materials are discussed extensively as background to the experimental work of the thesis.

Film depositions, device fabrication, various measurement/characterisation methodologies are discussed in Chapter 3.

Chapter 4 presents the structural, electrical and dielectric properties of yttrium oxide (Y_2O_3) and Y_2O_3 Metal-Insulator-Semiconductor(MIS) devices by X-ray diffraction analysis, Capacitance – Voltage (*C-V*) and Current- Voltage(*I-V*) characterisation.

The structural, electrical and dielectric properties of barium strontium titanate ($Ba_{0.5}Sr_{0.5}TiO_3$) thin film and MIS devices will be discussed in Chapter 5.

Chapter 6 deals with the performance of fully fabricated ACTFEL devices with perovskite barium strontium titanate ($Ba_{0.5}Sr_{0.5}TiO_3$) thin film and ZnS-based phosphor. In addition, photoluminescence (PL), electroluminescence (EL), laser annealing effects and barrier layer effect of blue emitting SrS-based TFEL devices which are undertaken in the first part of the programme.

Finally, Chapter 7 describes the summary of the research and suggests the guidance for further work.

REFERENCES

[1] Anton, Philip S. et al The Global Technology Revolution - Bio/Nano/Material Trends and Their Synergies with information Technology by 2015, National Defence Research Institute, CA, USA. 2001

[2] Chinnock, Chris, Laser Focus World, pp. 121 ~ 124, Feb. 1996 PennWell

[3] *Flat Panel Displays in the UK: A guide to UK capability, 2005/6 Edition* by Department of Trade and Industry(Dti), UK, pp. 2-21

[4] Im, James S. et al Materials for Flat Panel Displays, MRS Bulletin, Vol. 21, No.3, pp. 27 ~ 68, 1996

[5] Auciello, Orlando, et al. Electroceramic Thin Films Part I: Processing, pp. 21 ~ 58, Vol. 21, No. 6, 1996, MRS

[6] Auciello, Orlando, et al. Electroceramic Thin Films Part II: Device Applications, pp. 29 ~ 65, Vol. 21, No. 7, 1996, MRS

[7] Keller, Peter A. Laser Focus World, pp. A8 ~ A9, Oct, 1989 PennWell

[8] Whitaker, Tim (Ed.) LEDs magazines-Technology and applications of light emitting diodes (series of e-magazine from issue no. 1, April 2005), IOP, It is available at www.ledsmagzine.com

[9] FPD Technology Report - Building U.S. Capabilities in Flat Panel Displays, Department of Defense(DoD), USA, 1993

[10] Birk, Jane D. Information Display, pp. 10 ~ 13, Sept. 1992

[11] Maiser, Eric(Ed.) *European Technology: Flat Panel Displays 3rd and 4th Ed.* by German Flat Panel Display Forum(DFF), German Engineering Federation(VDMA), 2003-4

[12] Kitai, A. H. (Ed.) *Solid State Luminescence - Theory, Materials and Devices*, Ch 5, 1993 Chapman & Hall

[13] Shionoya, Shigeo and Yen William M, *Phosphor Handbook*, Ch 2, Sec. 10, 1999 CRC (references therein)

[14] Inoguchi, T, *et al.*, Stable high brightness thin-film electroluminescent panels, SID 1974 Digest, p.84

[15] Kincade, Kathy, Laser Focus World, pp. 75 ~ 81, June 2004 PennWell

[16] Vij, D. R. (Ed.) *Luminescence of Solids*, Ch 1- 4, & 6, 1998, Plenum Press

[17] OE Reports - Revolutionizing light: LEDs, ELDs and OLEDs, No 2004, Dec 2000, SPIE

[18] Mueller, Gerd, *Electroluminescence II - Semiconductors and Semimetals*, Preface and Ch 2-3, 2000, Academic Press

[19] Sun, S.-S, *et al.*, Proceedings of 17th IDRC, Toronto, Canada, p. 201, 1977

[20] Cranton, W., ***Ph.D. Thesis***, Bradford University, UK, 1995

[21] Dahotre, Narendra B. Laser Surface Engineering, pp 35 ~ 39, Advanced Materials & Processes, April 2002,

[22] Koutsogeorgis, D. C. ***PhD Thesis***, Nottingham Trent University, UK, 2003

[23] Mastio, E. A, *et al.*, Phosphor dopant activation using pulsed KrF laser annealing, CLF Annual Report 1997/98

[24] ANSI/IEEE Std 180-1986, *An American National Standard* IEEE Standard Definitions of Primary Ferroelectric Terms, 1986

[25] Kingon, A.I. et al. Alternative dielectrics to silicon dioxide for memory and logic devices(Insight review article section), pp. 1032-1038, Vol. 406, Nature, 2000

[26] Arimoto, Yoshihiro and Ishiwara, Hiroshi, Current Status of Ferroelectric Random-Access Memory, pp. 823 ~ 828, MRS Bulletin, November 2004

[27] Wallace Robert M. and Wilk, Glen (Eds.) Alternative Gate Dielectric for Microelectronics, pp. 186 ~ 225, MRS Bulletin, March 2002

[28] Liu, Yu ***PhD Thesis***, MEMS and BST Technologies for Microwave Applications, University of California, Santa Barbara (UCSB), USA, 2002

2. Background & Literature Review

Overview

This chapter focuses on how the EL devices work, the fundamental electroluminescent mechanisms, basic device structures and equivalent circuits of thin film electroluminescent display (TFEL). A chronicle of major development in electroluminescence (EL)-related materials and devices is presented and the physical and important optical properties of materials (ie., phosphors and dielectrics) reported from literature review are discussed to understand the basics of other major flat panel display technologies and EL phenomenon. This chapter begins with an extended briefing on various flat panel display technologies mentioned in Chapter 1.

2.1 Flat Panel Display Technologies and Devices

A single display device or technology meeting all technical requirements is extremely difficult and virtually impossible; so each one has its advantages and disadvantages. Thus, each device or technology is of importance in specific applications. In this section, other major flat panel display technologies will be discussed. The review of this section will be focused on each display technology's brief history, technical features and current research & developments(R&D) for better understanding other display technologies and extending related display knowledge.

Liquid Crystal Displays (LCDs)

Liquid crystals (LCs) were discovered by the Austrian biologist Friedreich Reinetzer[1,2,3] in 1888 and it took nearly 80 years before the materials and electronics were advanced enough to use them practically[3,4]. There are various liquid crystal modes such as twisted nematic(TN), super-twisted nematic(STN), smectic (soap-like), chiral nematic (cholesteric-like) and others according to different developments. The classification[1] of liquid crystal modes is determined by the electro-optic effects: (a) current, (b) electric field and (c) thermal. For a reference, the most widely used liquid crystal type is the twisted nematic (TN) which means "thread" from the Greek word and the liquid crystal cell appears thread-like[3]. The TN-mode was invented by the Swiss researchers, Martin Schadt and Wolfgang Helfrich[1,2,3,4] in 1971. The twisted

nematic liquid crystal and its optical transmission properties (on/off state) is shown in Figure 2-1[3,4].

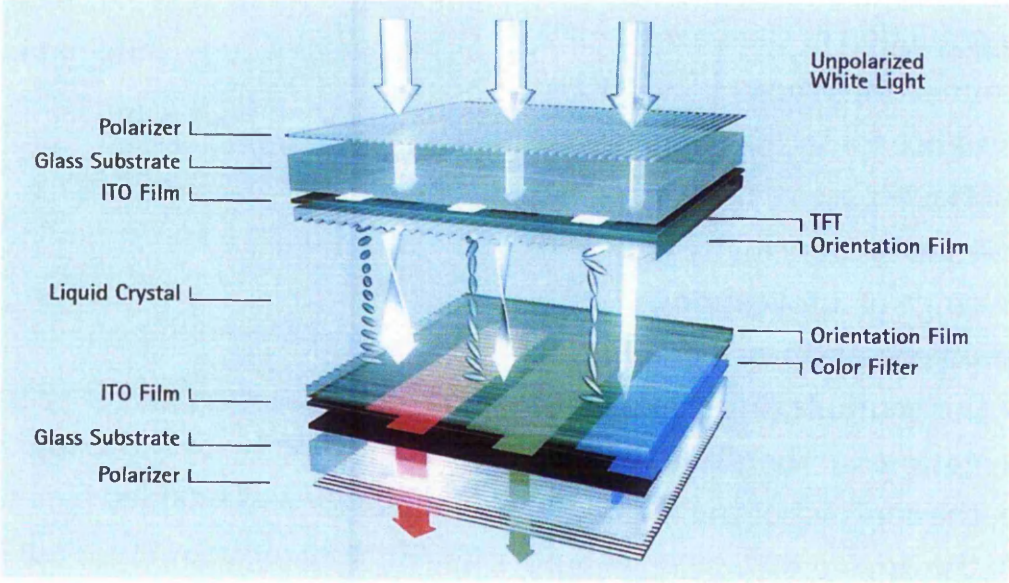


Figure 2-1 The twisted nematic (TN) liquid crystal display (LCD)and its light transmission properties.[3,4]

Most substances have a single melting point at which they change from a solid to an ordinary transparent liquid, but particular types of materials have a certain intermediate temperature range to show an opaque and cloudy liquid property and then they can turn to normal transparent liquid at higher temperature.[1] The term "liquid crystal" has a double meaning which literally comes from its phase of matter when a substance behaves externally with the fluidity, but at the same time shows a crystalline structure which exhibits optical double refraction[1,2,3]. The structural orientation of molecules in a liquid crystal can be easily re-oriented by an external stimulus such as an electric field and temperature. Initially, the molecules of liquid crystal displays have their own orientation and this can be changed by the application of a voltage or by heat and thus, the optical characteristics can be controlled[1]. As a passive and non-emissive device, a liquid crystal display utilizes the modulation of light by the liquid crystal cell. In other words, the liquid crystal cells play a role as a "light valve"[3,4].

Typically the liquid crystal displays (LCDs) have following advantages[1]: (a) low power consumption(~ $\mu W/cm^2$), (b) low driving voltage (< 10 V), (c) thin and lightweight, (d) mature

technology and (e) easy to make full colour. However, there are some disadvantages, too. One of the most critical issues is the necessity of a backlight unit (BLU)** as a light source due to the non-self luminous property of the LCD devices. As a result, it causes large increase of overall power consumption and cost. In addition, the liquid crystal displays have a relatively short range of operational temperature, a narrow view angle and contrast issue compared to other displays. More detailed advances and difficulties in technical, manufacturing and economic point of views was presented in Table 1-1 in the previous chapter.

The liquid crystal displays (LCDs) are already dominant and is also trying to expand its possibility dramatically in its size, cost, resolution, various applications and almost every aspect. Among various flat panel displays on the commercial market, the LCD panels have been replacing conventional cathode ray tubes (CRTs) in TV screens, computer monitor applications and other small-size portable personal devices. Thus, liquid crystal displays (LCDs) have been becoming synonymous with a terminology, flat panel displays[5] due to its dominance and impact to the public and the market. Some manufacturers demonstrated over 40 to 80 inch-wide TFT-LCDs for HD†† ready with a minimum 1366 × 768 resolution (approx. 1.05 million pixels, 16:9 aspect ratio) at the 2006 International Consumer Electronics Show (CES), Las Vegas. Now LCD panels are comparable to the plasma panel displays (PDPs) segment in size and they can have stronger competitiveness in the cost. The "Gen 7"‡‡ production facilities enable the mass production of large screen sizes and at the same time reduce the cost of the LCD panels. Using a liquid crystal technology, various types of the display with alternative processes and architectures such as microdisplays based on a liquid crystal-on-silicon (LCoS), or low/ high temperature poly-silicon(L/HTPS) have been developed. As a result, a LCD technology has a full line-up from micro- to large-format displays (See Figure 2-13).

Plasma Display Panels (PDPs)

Once plasma displays were known as the representative of a "display-on-the wall" or "hanging-on-the-wall" TV concept. Plasma displays utilise the physical phenomena of gas

** Currently the back light unit(BLU) has two types of a fluorescent lamp(FL) and LEDs. FLs have a cold cathode fluorescent lamp(CCFL) and an external electrode fluorescent lamp(EEFL).

†† A full standard resolution of high definition television(HDTV) is 1920 x 1080 lines (approx. 2.1 million pixels) with 16:9 aspect ratio. Simply, 1080p is used frequently.

‡‡ Gen 7 means a manufacturing facilities providing approximately 1950 x 2250 (LG.PhilipsLCD) or 1870 x 2200 mm (Samsung) glass substrate and can produce twelve 32" LCD panels.

discharge and photoluminescence (PL)[6]. Gas discharge has such a long history back to the astronomer Jean Picard[2] in 1675. Practically, the very first prototype for a plasma display monitor was invented in 1964 at the University of Illinois by professors Donald Bitzer and Gene Slottow[1,2,7]. After invention, the Bell System used a receiver based on a gas discharge display for demonstration of their live television in 1927[2]. However, it was not until after the advent of digital and other technologies that successful plasma televisions became possible. During the 1970s and early 80s, plasma displays started from the pilot production to full-scale production. Currently, plasma panel displays are available on the market in large-format display segment only from 40" to 80"-wide screens[8] and the world largest 103"-wide plasma display prototype was demonstrated by Panasonic/Mastushita at the2006 International CES. The schematic cross-section of a plasma display panel (PDP) is shown in Figure 2-2. The PDPs have the following characteristic pros and cons[1,2,4]: ① self-luminous(ie., emissive), ② easy luminance control, ③ fast response speed, ④ good resistance to vibration, ⑤ CRT-like colour gamut and ⑥ long life (≥ 65,000 hours, ie., approx. 10 years). However, due to the size limitation, PDPs are not suitable for small- and medium-size high resolution applications. In other words, plasma display panels have minimum pixel size(approx. 300 μm) and its weight matters even if the screen is thin and flat. A high driving voltage is necessary to operate the gas discharge and thus, leads to high power consumption. In addition, it is relatively expensive in manufacturing.

Plasma displays are typically filled with an inert (or noble) gas such as neon(Ne) or xenon(Xe) and driven by row-column electrodes. High driving voltage can ionize gas at each pixel which is created by row and column electrode and then UV light emission(from ionized particles with high kinetic energy) can collide with phosphor materials deposited inside of the pixel as a form of energy transfer. Finally, excited electrons in the phosphor go back to the ground level and they can emit visible light from the energy difference between an excited and the ground levels.[1,2,4] Luminescence in plasma display is initiated by UV light which is driven by the external high voltage and thus, it is known as photoluminescence (PL)-based emissive display.

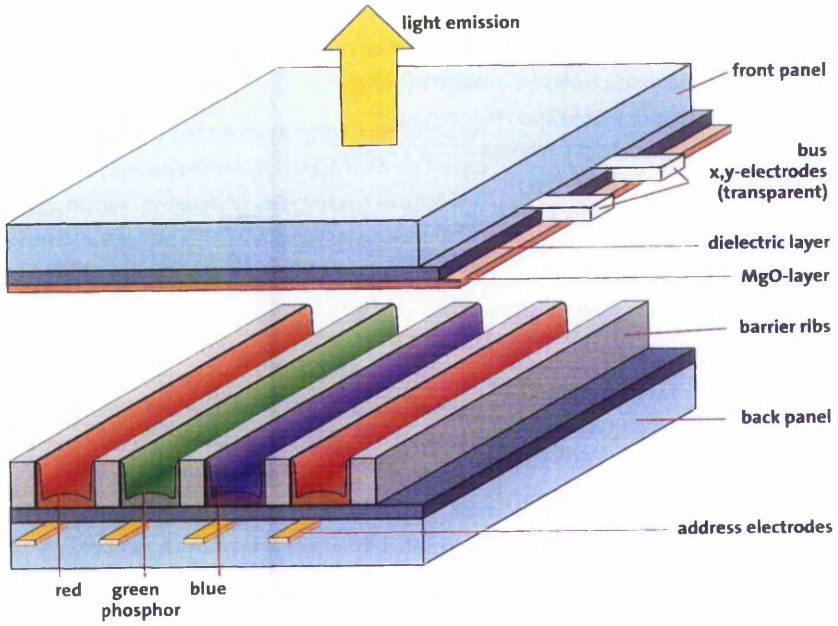


Figure 2-2 A schematic cross-sectional structure of a plasma display panel(PDP)[4]

Field Emission Displays (FEDs)

In order to implement a thin CRT display, a field emission cold cathode was demonstrated for the first time by C.A. Spindt[9] at Stanford Research Institute in 1968 since D.A. Buck and Shoulders[10] had reported the theory and possibility of field emission devices in 1959. In 1987, the first high resolution colour FED prototype was demonstrated by Holland et al. at SRI International.[11] During the 90s, PixTech(1994, from LETI[11]) produced the first 0.8" full-colour FED products on the market and Futaba(1995) produced 4.7"(12cm)-monochromatic commercial FED displays using the Spindt-type emitter. In the meantime, unlike a microtip emitter, Cannon suggested a novel structure which is called "Surface-conduction Electron-emitter Display (SED)[12]" as a flat-type emitter in 1997. Motorola demonstrated a full-colour 5" FED in 1997. In 1999, Samsung showed a full-colour 5" FED using carbon nanotubes (CNTs) technology while Futaba developed a full-colour 5" FEDs which can operate at low voltage. During the 2000's, the screen area of the FED increased dramatically. Candescent/SONY reported a 13.2" full-colour FED and Samsung and Cannon/Toshiba showed a demonstration of 32" & 38" CNT-FEDs and 36" SED displays in 2003 and 2004, respectively[13,14].

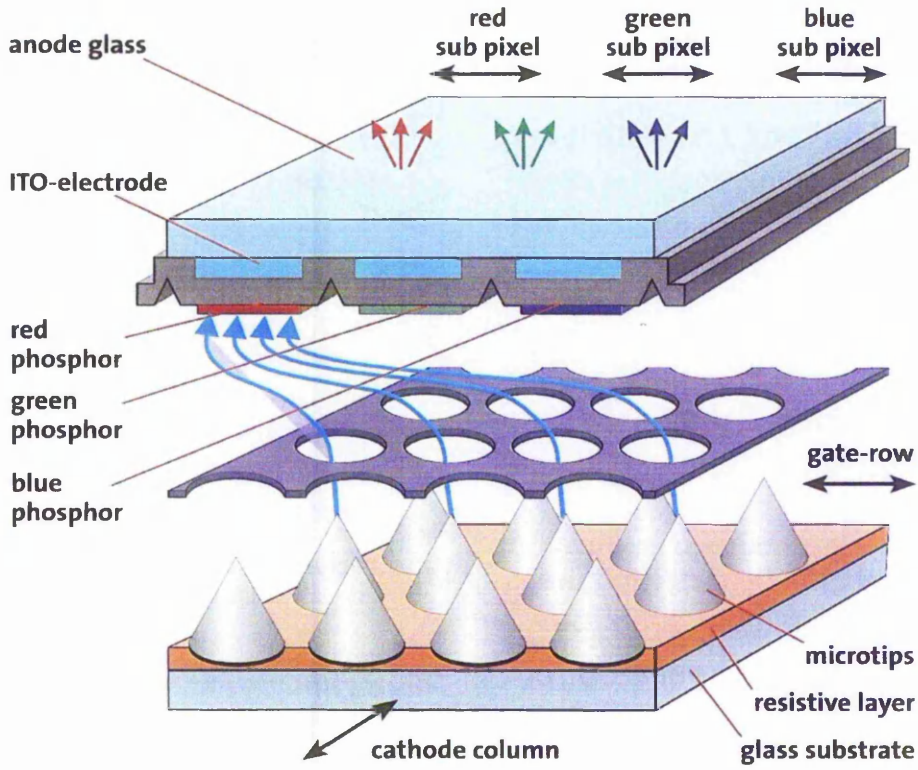


Figure 2-3 A typical architecture of a field emission display (FED) with the Spindt-type Microtip array[4]

Field Emission Displays (FEDs) and CRTs have many similarities in their structure and mechanism. However, there are differences between them and FEDs have several characteristic advantages [13,14,15,16] in that they do not have electron-beam scanning requirement because each pixel has its own array of cold cathodes(up to several thousand field emitter array per pixel) and thus, it can provide high luminous efficiency and massive redundancy[13]. The display panels are very thin (approx. 1 cm) and light. In addition, they have better view angle (up to 180° degree) than CRTs. Unlike CRTs, there is no shadow mask so that the electron beams can collide with the phosphor layer directly in front face. They have wide range of operational temperature (-45 ~ 85°C) due to being a solid state device. As a vacuum microelectronic device, there are no heating, power dissipation and radiation damage[13,14,15] problems. However, field emission displays have technical difficulties [4,13,15] such as high voltage operation, short-lifetime, low production yield and complication in fabrication. These technical disadvantages have been improved and new alternative structures and technologies - surface(flat) emitters -

mentioned above have been developing. The fabrication of field emission displays is based on a micro-electro-mechanical system (MEMS)[17], or micromachining techniques with a vacuum microelectronics. A typical architecture of field emission displays is shown in Figure 2-3.

Various alternative structures or developments of a field emission cathode were categorized by materials and a type of the emitter tip[13,15,18]: (a) Micro tip material: Si, metal(Mo), carbon(DLC or CNT), (b) a type of the emitter: ① cone-like(eg, Spindt), ② wedge-like, ③ whisker-like(eg, CNT), ④ plane or flat emitter(eg, surface-conduction electron emitter from SED), ⑤ thin film edge emitter, ⑥ metal-insulator-metal(MIM) emitter, ⑦ ballistic electron surface emitter (eg, BSD) and ⑧ screen printing field emitter (eg, PFED)[15]. In order to improve the electron emission stability and uniformity of the Microtip materials, carbon nanotube (CNT)-FED prototypes was demonstrated by Motorola and Samsung, respectively. The surface-conduction electron emission display(SED), a metal-insulator-metal (MIM) and the ballistic-electron surface-emitter display (BSD)[19] devices based on field emission phenomena are under development by Cannon/Toshiba, Hitach and Matsushita, respectively. General structures and electron emissions of the BSD and the SED devices are shown in Figure 2-4 and 2-5, respectively.

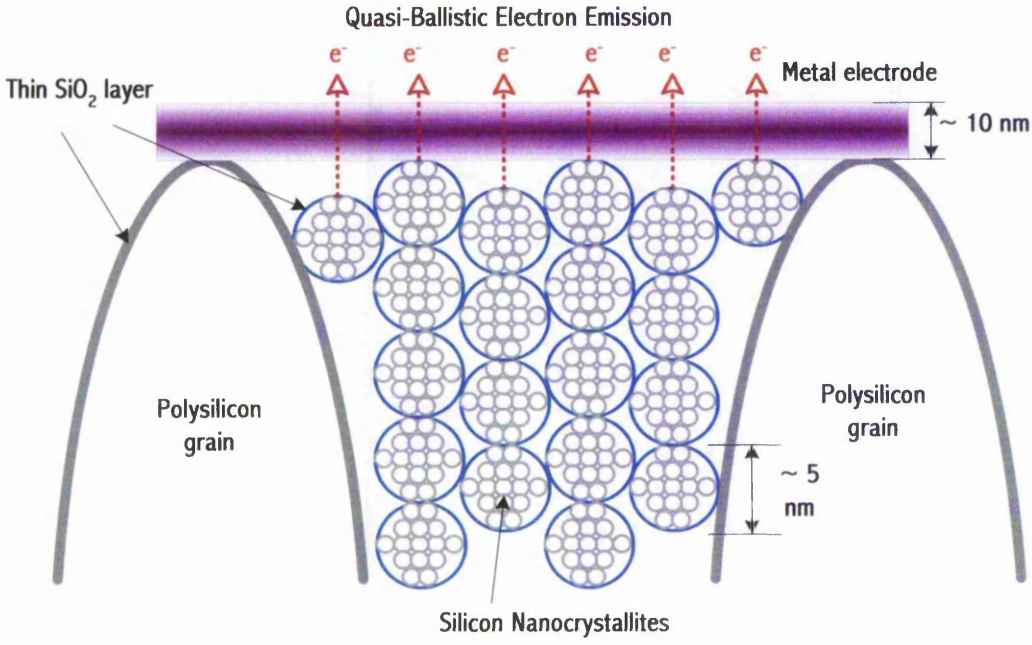


Figure 2-4 The ballistic electron surface emission model of the BSD device (Mastushita/Panasonic)[15,19]

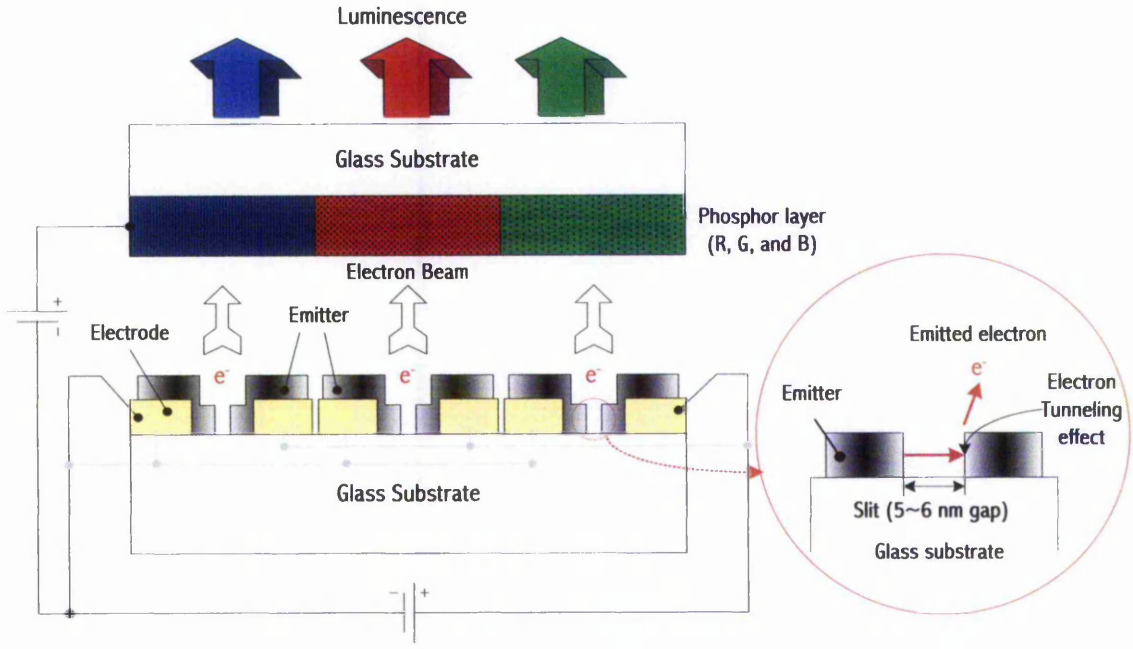


Figure 2-5 A schematic cross-section and surface electron emission of the SED device (Cannon/Toshiba)[12]

Organic Light Emitting Diodes (OLEDs), and Organic Electroluminescence

Flat panel display devices using organic materials have been extensively studied so that organic light emitting diodes (OLEDs) and polymer-based EL devices are presented and now they are available on the market mainly in small-size applications like a mobile phones, digital camera viewfinders, car stereos and PDA screens. Many manufacturers - Sony, Samsung SDI, Sanyo, Sharp, NEC and others - demonstrate their medium-size applications for TV and laptop computer screens. In 1963, light emission with a specific wavelength was discovered from an organic thin films by M. Pope[20], and W. Helfrich[21]. 25 years later, light emission from thin films of small molecule organo-metallic compounds was first discovered by Kodak in 1987[22]. In 1990, a conjugated polymer-type EL[23] devices were developed by R.H. Friend's research team at Cambridge University. After that, OLEDs have been becoming one of the most promising display technologies. Unlike any other display technologies, it has only taken about 20-30 years to fully commercialize this display technology[4,24].

OLED technology shows its feasibility to play a significant role in the flat-TV market, offering

an excellent image quality due to its important features such as high contrast, large viewing angle and fast response time combined with an ultra-thin form factor and low power consumption.[4,25] Encapsulation[28] in OLED structure is the most important issue because basically organic materials are very weak or sensitive to moisture and oxygen.[28] Thus, it needs an extensive encapsulation technique. At the same time, there are lifetime issues of the device's stability and uniformity in colours.[4]

A basic structure[25] of the organic EL device and its luminescence mechanism are illustrated in Figure 2-6 and 2-7, respectively. Typically, a transparent conducting oxide, Indium Tin Oxide (ITO) and low work-function metals - Ca, Li, Al; Li, Mg, Ag - are used for anode and cathode electrodes, respectively. When a forward bias is applied to the electrodes, holes and electrons are injected to their transfer layers through their injection layers. These layers are called a hole-transfer layer (HTL) and an electron-transfer layer (ETL), respectively. The externally injected holes and electrons are bound to each other to create excitons[§§] in the emitting layer (EML). The organic luminescence (OLE) takes place from the radiative recombination of these excitons[26,27] in the emitting layer.[28]

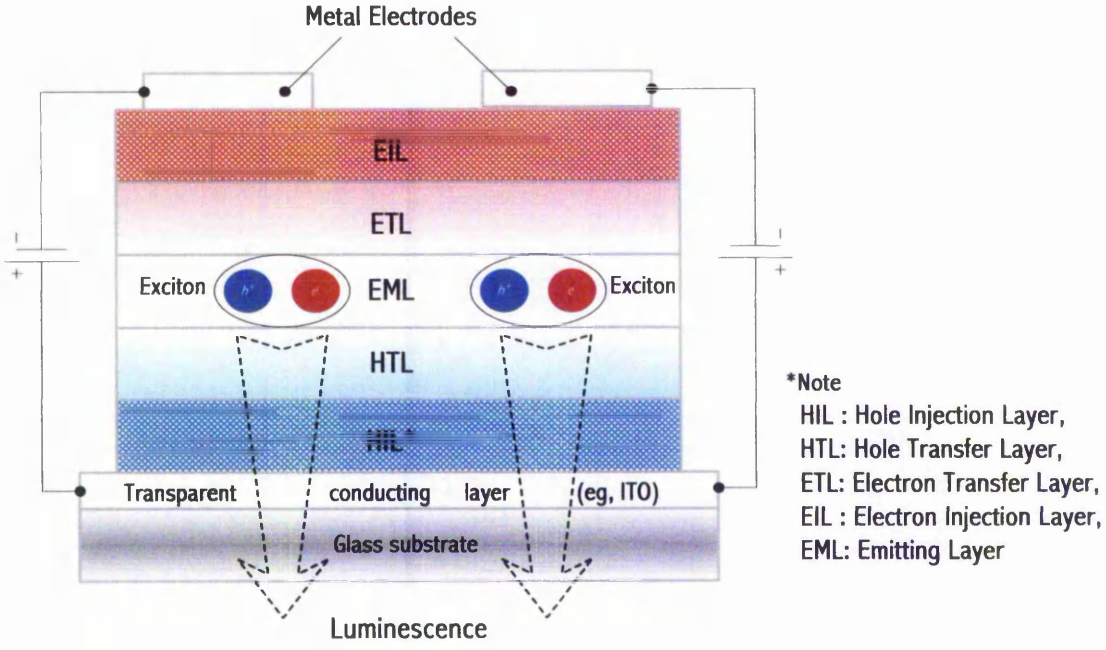


Figure 2-6 A typical across-sectional structure of OLEDs[25]

[§§] An Exciton is the electronically excited state consisting of an electron and a hole under various correlated motions. In other words, it means the excited bound electron-hole pairs(EHP). See ref. 26 and 27 for the details.

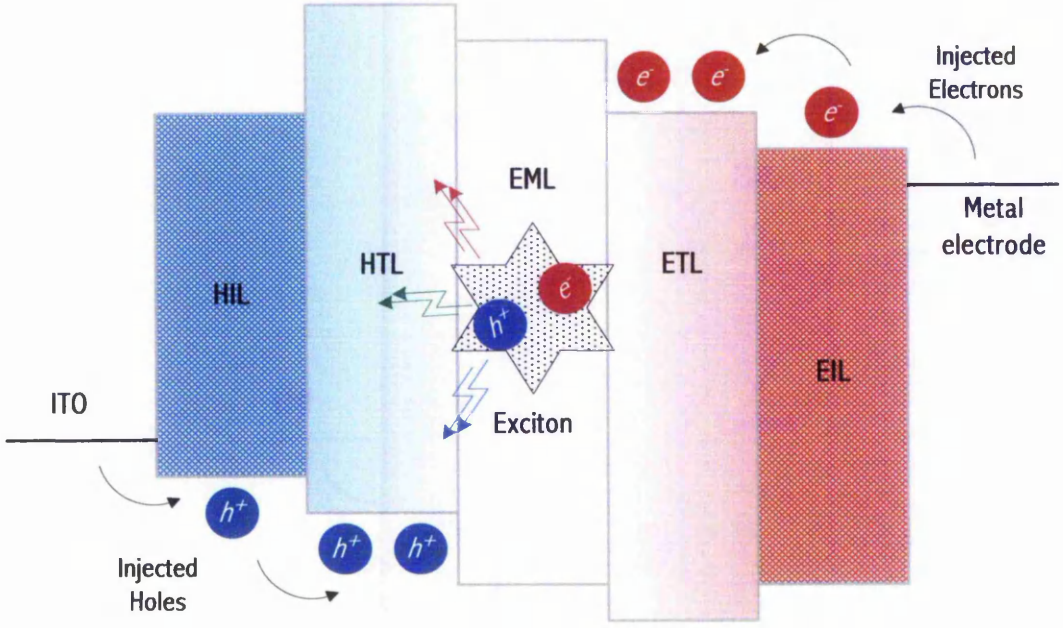


Figure 2-7 The simplified luminescence mechanism of mono-molecule OELD cell[25]

Red, green and blue organic materials for a full-colour OLED display are already developed and Cambridge Display Technology (CDT) reported a very bright green OLED device(100 cd/m^2 at 2.6 V) which showed better luminance efficiency(22 lm/W)[23] than inorganic LED devices with maximum luminance efficiency (~ 20 lm/W).[23,29] Thanks to these series of excellence in OLED research and development, OLED devices are showing feasibility in its applications, technology and the display market.

Flexible Displays, or Paper-Like Display

Most flexible displays are based on reflective properties, so they are often called "reflective displays". These flexible display can be a symbolic representative in a ubiquitous computing*** [30] and information display environment. This display technology can provide more unique and extended freedom in access to information no matter where we are and thus, the flexible displays can be applied to not only e-papers or e-books, but smart cards/IDs, tags, sign posts, large posters for a bulletin board/advertisement, fashion apparels and so on. Any format

*** It also is called "pervasive computing." The idea means the embedded computation into the environment enable people to move around and interact with computers more naturally than they do now. It was known by Mark Weiser's papers. (refer to ref. 30)

display will be possible in the future through this kind of foldable, rollable and wearable display technologies.

Currently, several different types (or architectures) of flexible displays have been developed while emissive flexible displays based on OLED are demonstrated.[31] E ink Corporation, one of the leading flexible display/material providers and a spin-off of Massachusetts Institute of Technology (MIT) Media Lab., in collaboration with Lucent Technology suggested the first new concept of an Electronic Paper Display (EPD)[32,33] technology which is called Electronic Ink (i.e., E ink)[34], utilising the electrophoretic° effect from a bi-stable ink-like material. This is a paper-like electronic information device for e-newspapers and e-books. E ink Corp., Phillips Electronics(Netherlands) and Sony Corp.(Japan) announced the world's first active-matrix electronic paper display e-book reader - LIBRIé ™ [31]- application based on E ink's electronic display material in Japan, 2004, but its expectation was not successful. In 2006, Sony launched the 2nd version 6" black-and-white handheld e-book reader which is called "Sony Reader" at International Consumer Electronics Show(CES) in Las Vegas. Besides, E-ink 2-bit black-and-white displays showed 170 pixels per inch (PPI). E-ink Corp and Toppan Printing Co. Ltd demonstrated an advanced 12-bit colour electronic paper display prototype with 400 x 300 resolutions (83 pixels per inch) in 2005. Now a segmented display and a high resolution black-and-white display are now available.

Xerox's Palo Alto Research Center (PARC) rediscovered a similar technology which is called Gyricon rotating ball display[35,36] based on the electrophoretic effect. The difference[37] between two technologies is that Gyricon used one element per a pixel sphere with a dark and a white side, but E-ink is composed of microencapsulated clear spheres containing a dark-coloured liquid dye material with thousands of microscopic particles of white-coloured titanium dioxide[37]. In Figure 2-8, E ink's microcapsules and Xerox's Gyricon rotating balls are illustrated[37]. SiPix Imaging Inc. developed a new electrophoretic flexible display with a novel structure[38]. There is a micro-scale container - Microcup® - which holds minute quantities of materials such as fluid and particles and the display has good resistance to impact and pressure due to its architecture of supporting walls. The SiPix's flexible display device structure and pixel patterns are shown in Figure 2-9. The SiPix Imaging Inc. reported passive-

° Electrophoretic effect, or Electrophoresis is the movement of an electrically charged substance under the influence of an electric field. This movement is due to the Lorentz force: $F = qE$ (F, force; q, charge; E, electric field).

and active-matrix electrophoretic displays[39]. Currently a segmented, active-matrix and custom e-paper displays or modules are available.

Royal Phillip Electronics has demonstrated innovated flexible display technologies such as a printable, an electrowetting and a rollable display.[31] The printable displays are based on a cost-effective new method in a flexible and ultra-thin LCD layer production on a single plastic substrate by using a double-UV radiation process in fabrication.

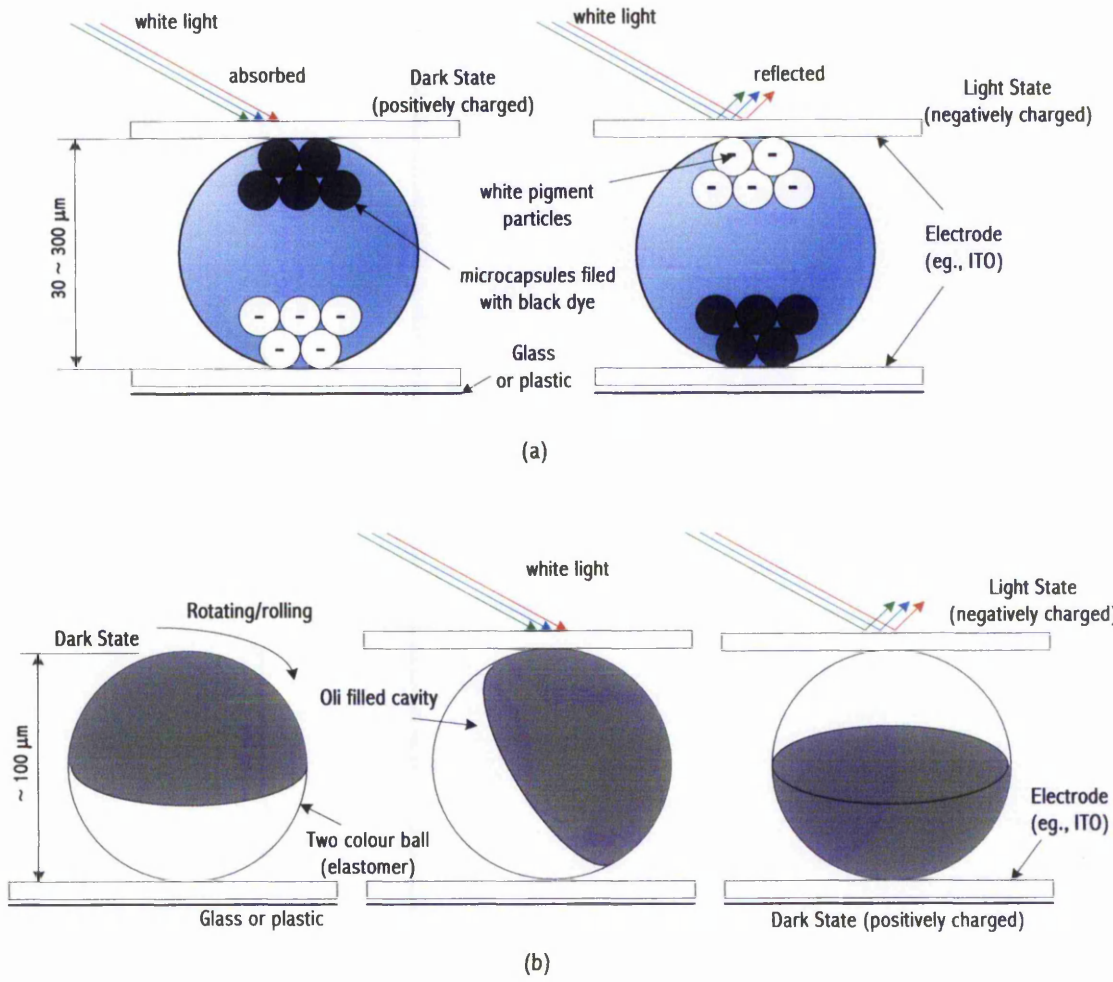


Figure 2-8 Illustration of reflective and electrophoretic effect: (a) E ink's Microcapsules (pixel spheres), and (b) Xerox's PARC Gyricon Rotating Balls[33,34,35,36,37]

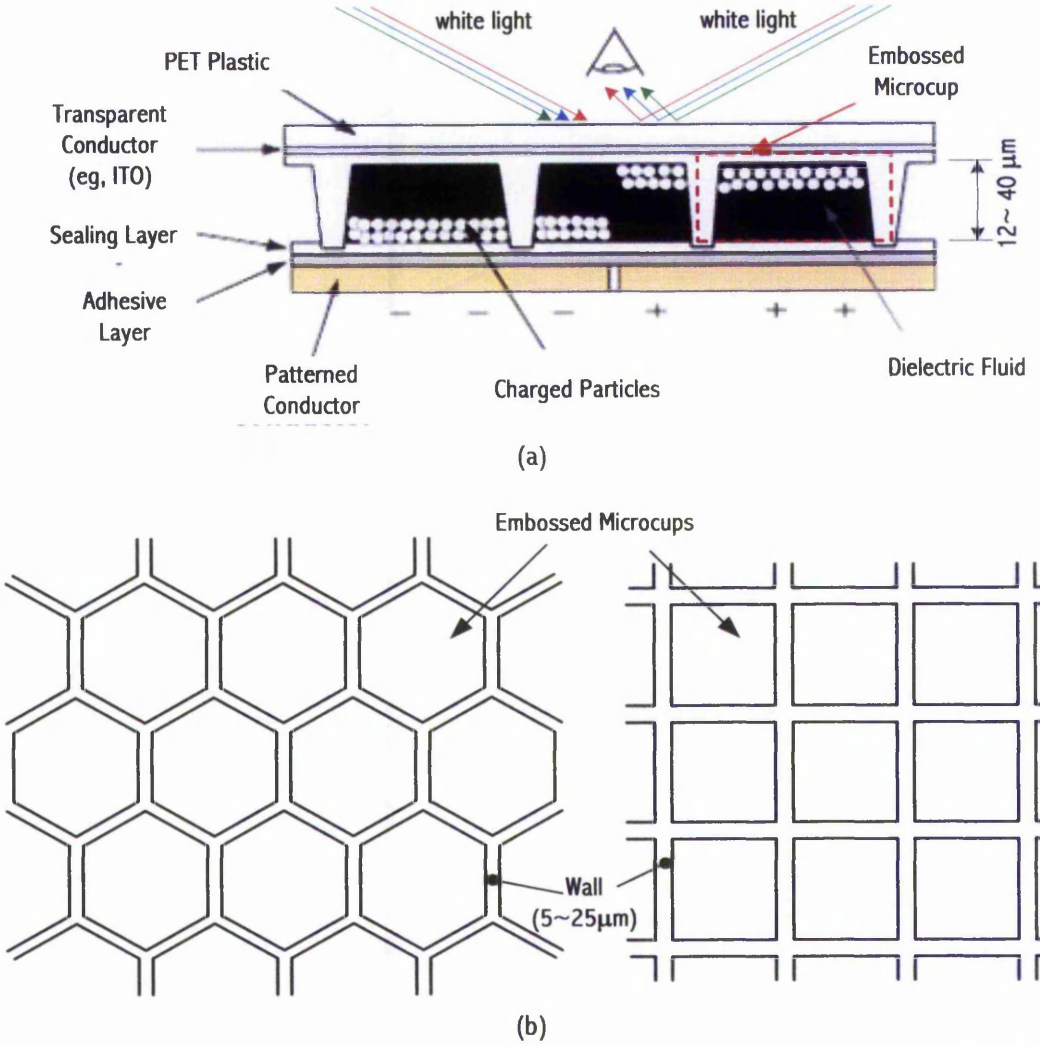


Figure 2-9 SiPix Imaging Corp.'s flexible display: (a) A schematic cross-section structure with the Microcup® and (b) Two Patterns of the embossed Microcup® - Hexagonal (on the left) or Square (or Rectangular which is omitted) grid[38,40]

When a water droplet is placed on a hydrophobic substrate, its contact area on the substrate depends on the surface tension properties at the interface and an applied electric field. In other words, an external applied voltage can control or modify a wetting property of a material. This is the principle of the electrowetting technology[41,42,43]. For a display, when homogenous oil and water mixture on the hydrophobic insulator, the oil moves aside when the electric field is applied and then the reflecting surface can be exposed. When the applied electric field is removed, the oil returns to original state. The electrowetting display structure and mechanism are illustrated in Figure 2-10. The important advantage of this electrowetting display is that it

can provide a very similar paper-like environment in its technical parameters[42], which is given in Table 2-1. For reference, the properties of paper are included.

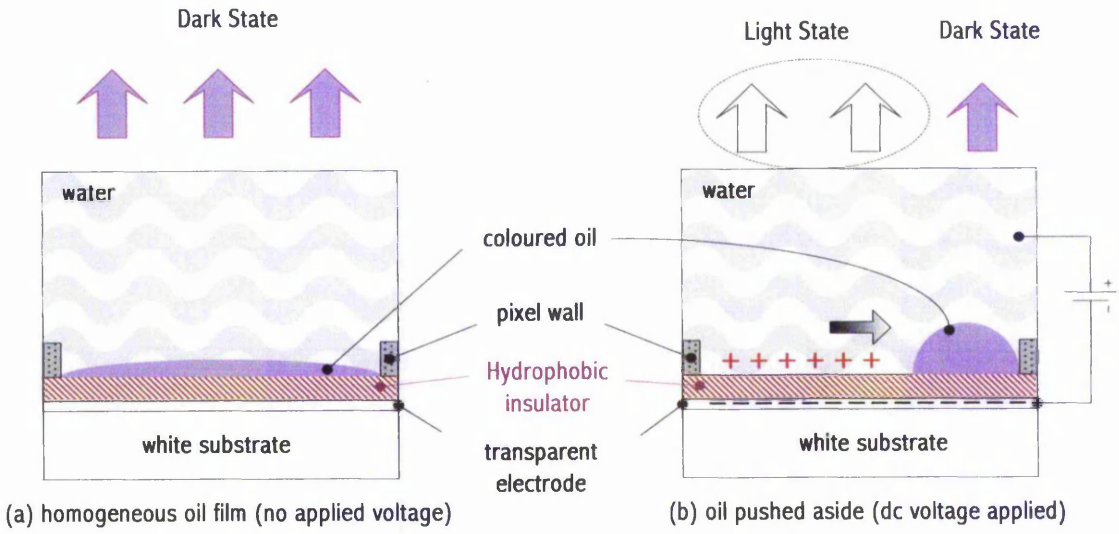


Figure 2-10. Illustration of a simple structure and mechanism of electrowetting display when the dc voltage is applied or removed[41,42,43]

Table 2-1 Comparison of key characteristics of various reflective display technologies[37,42]

	Paper*	Electrowetting**	Gyricon	Electrophoretic	TN-LCD	CN-LCD
Contrast	15-20:1	20-30:1	10:1	10-30:1	<5:1	15:1
Reflectivity	70-80%	40%	20%	40%	<5%	60%
View angle	good	good	good	good	narrow	good
Response time	-	30-100 ms	80 ms	100-150 ms	15-20 ms	<10 ms
Full colour	Yes	Yes	No***	No****	No	Yes
Substrate	-	Plastic / glass	Plastic / glass	plastic/ glass	glass	Plastic / glass

* paper: laser print; TN-LCD = reflective twisted nematic LCD; CN-LCD = Chiral nematic (Cholesteric) LCD
** optical properties: in-pixel x 0.9 (accounting for losses at walls)
*** Development is under way; **** Colour filter array may be possible.

Phillips PolymerVison (or PolymerVision) showed the first prototype of a 5" QVGA(320 × 240 pixels) rollable electronic-document reader(Readius®)[44, 45] with four gray levels at Internationale Funkausstellung (IFA) in 2005. The rollable electronic-document reader is based on the bi-stable electrophoretic material from E Ink Corp. Plastic Logic (Cambridge, UK) developed a printed active matrix backplane technology[46] for the flexible display applications including LCDs and OELDs. They have been focusing on all-plastic flexible displays based on their printed backplane process and the imaging film of E ink Corp. The substrate materials and packaging techniques for the flexible displays have been becoming more important and researched actively in many aspects [47].

So far, the flexible displays can provide the following common features against other flat panel displays: ① ultra-low power consumption (and no power needed to retain contents), ② various size of displays (mobile phone ~ A3 size and larger[37]), ③ light, thin and flexible, i.e. bendable or rollable, ④ low cost in production, ⑤ various application formats and ⑥ good contrast[37,42].

Thin Flat CRTs, and other display technologies

The direct view CRT has been no longer the only possible display choice for many years. Now it has to compete with LCDs, plasma and projection technologies based on CRT and microdisplay engines. At the same time, other flat panel technologies such as OLEDs, and CNT-FEDs are on the list of potential contenders.

In August 2004, Samsung SDI and LG.Philips Display for the first time demonstrated so-called "slim" CRTs with approximately 35 cm thickness (total 38 cm for TV set depth) for 32" digital TVs at the joint Asia Display and IMID conference in Korea, respectively. They made an effort to reduce conventional cathode-ray tube depth and now the slim CRTs are in volume production. They do not take much of the space and are comparable to LCD screen. CRT technology is fully matured and CRT screens have had various applications from a specific-purpose to general entertainment applications for a long time. Although portability is getting important in display devices and the wireless communication environment, the thin CRTs might have feasibility in small and medium-size TV screens and monitors sector due to supporting by the four features of low price, image quality, brightness and innovation[48].

Current display technologies for the large projection TVs are based on CRT, LCD and digital light processing/digital micromirror device (DLP/DMD) technologies[49]. In particular, LCD and DLP-projection TVs are becoming more important in projection technologies and on the market. There are three different technologies in LCD-based projection TVs[50]: amorphous silicon (a-Si), polycrystalline silicon (poly-Si) and liquid crystal-on-silicon (LCoS)[51] technologies. The LCoS technology††† is a relatively new light engine for the projection TVs. Basically, as light is passing through the three - red, green and blue - LCD panels, each pixel on the panels can be opened to allow light to pass or to block the light (see Figure 2-1). The "light valve" activity can modulate the light and then produces the image which is projected onto the screen. Like the flexible displays discussed in previous section, DMD and LCoS-based displays use reflective mode for projection TVs (PTVs), but transmissive mode liquid crystals (LCs) are used for most LCD projectors.

A DLP engine which is based on DMD technology is competing with LCD - the LCoS-based engine - within the projection TV market. In fact, DMD technology is interesting due to its architecture, theory and advantages in display technology.[52] Digital Light Processing (DLP) projection systems based on the DMD provide high-quality, seamless, all-digital images which have exceptional stability and freedom from image lag.[50] However, DLP projection systems have been reported to have a couple of issues such as expense, rainbow effects and dithering problem[53] while LCoS-based projection screens are free from those problems and better in overall performance and manufacturing cost. On the contrary, LCoS systems have upcoming challenges such as the optical system efficiency, its architecture, material selection, the lifetime and working conditions.[49] Both of these systems are based on a fully matured existing silicon technology, which is the critical advantage for mass production and wide range of integration possibility. Thus, the DLP(or DMD) and the LCoS systems will be the major technologies on the market for the time being.

The digital micromirror devices (DMDs) were developed by a scientist, Larry J. Hornbeck[54], at Texas Instruments Inc. in 1987. An advent of the DMDs could open the possibility of so -called "all-digital display" system[52]. The DMD is a reflective mirror array of fast, digital light switches which are monolithically integrated on a silicon address chip. The DMD pixel's

††† LCoS display technology is , of course, used for microdisplays and near-to-eye displays. The DMDs is also one of microdisplay technologies.

structure is made entirely of aluminum and fabricated using standard semiconductor deposition and micromachining techniques. Structurally, the tiny arrays of mirrors (16 μm square) are constructed on an individual (CMOS) SRAM cell (see Figure 2-11). Typical mirror tilt is +/- 10 degrees forming a plane parallel to the underlying silicon substrate. The mirror is titled by electrostatic attraction produced by voltage differences developed across an air gap between the mirror and the memory cell. When the memory cell is in an on-state, the mirror is tilted by +10 degrees. The mirror is tilted to -10 degrees when it is in an off-state.[3] The DMD pixel architectures and SEM photomicrographs of a DMD pixel array are illustrated in Figure 2-11[55, 56] (refer to Migl's paper[57] for interface of DMD). Interestingly, Philips and Japanese manufacturers have been much more interested in LCoS-based projection TV systems, while the other manufacturers have made use of the DMD-based technology. Both of these commercial products are available.

Another technology for the rear-projection TV is a grating light valve (GLV) device. The GLV device was invented by David Bloom's (now Silicon Light Machines, formerly Echelle, Inc.) team at Stanford University in 1994.[58,59] Like the DMD devices, the GLV device is based on a micro-electro-mechanical-system (MEMS) technology and has a similar background to that utilizing a spatial light modulation as a light valve. The GLV[60] device consists of parallel rows of reflective ribbons. Alternative rows of ribbons can be pulled down one-quarter wavelength to create diffraction effects on incident light. The ribbons are typically 100 μm long, 3 μm wide and 100 nm thick for a 25μm pixel. Six ribbons are needed for each pixel. When all reflective ribbons are in the same displacement, it can produce a "dark state." If the alternative ribbons are downward, diffraction produces light at an angle which is different from that of the incident light. It creates a "light state (bright spot)". In 2002 Sony developed a prototype of GLV-based projection TVs. A basic structure of the GLV device is illustrated in Figure 2-12[58,59,60].

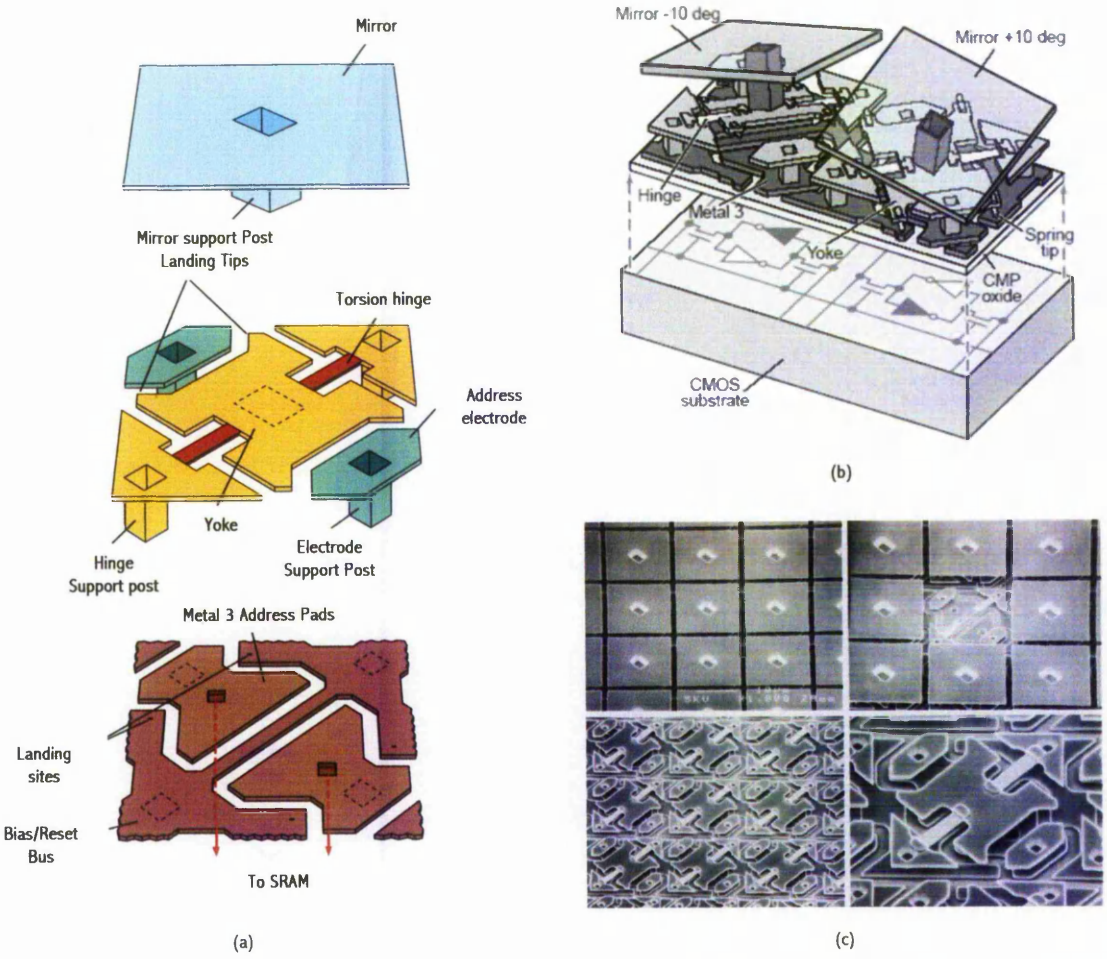


Figure 2-11 The DMD device: (a) DMD architecture (exploded view), (b) Two DMD pixel device (mirrors shown as transparent) and (c) SEM images of a portion of the fabricated DMD mirror array[55,56]

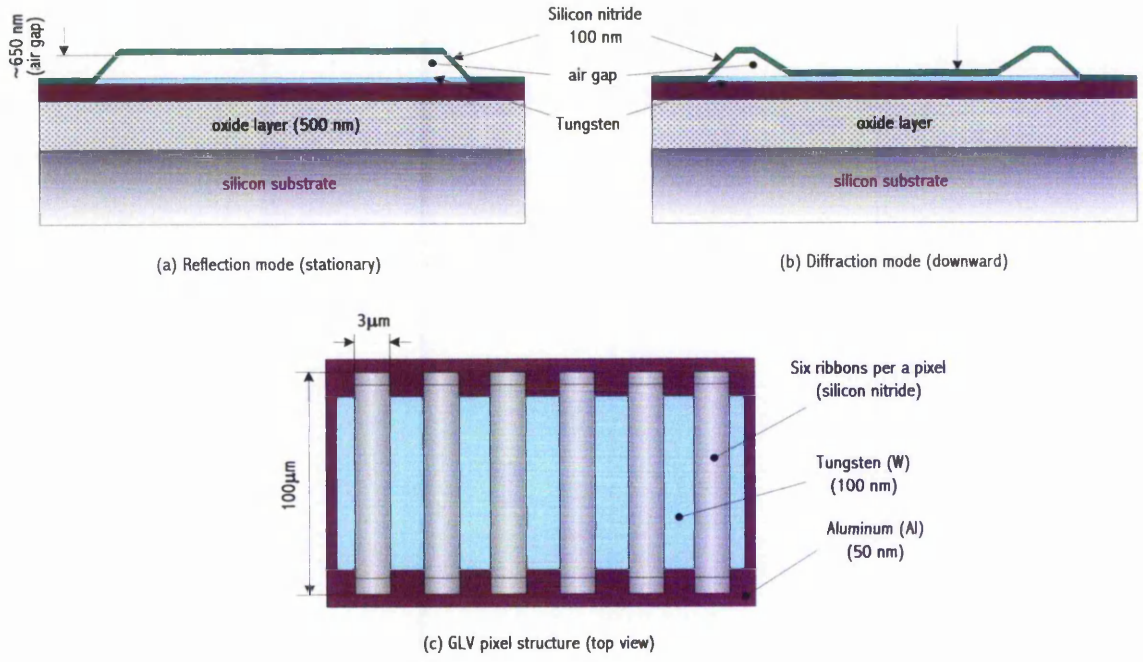


Figure 2-12 A Schematic diagram of a Grating Light Valve(GLV) device

The relationship of Microdisplays and the projection TVs is very close because the projection TVs are one of the final applications based on Microdisplay devices except CRT-type projection TVs. In fact, Microdisplays and the projection TVs can be overlapped in their technologies. In this section, the Microdisplay's definition, types and applications will be discussed briefly.

Microdisplays are usually less than 1 in. size in diagonal, but they have various resolutions from VGA (ie., 640 × 480) to UXGA(1600 x 1280, 4:3 aspect ratio) to HDTV[61]. In addition, the smaller the display, the higher resolution it has. Thus, Microdisplays are the small but powerful imagers behind various lightweight digital applications such as business projectors, digital cinema, head-up displays for vehicles/airplanes and advanced head-mounted units for gaming, surgery or military-purposes[62]. The microdisplays vary in type according to their inherent properties. Broadly, there are three categories such as transmissive, reflective and self-luminous modes[61]. For the transmissive types, high-temperature polycrystalline TFT LCD (HTPS) and Silicon-on-Insulator (SOI) LCD technologies can be applied. LCoS, DMD and Grating Light Valve(GLV) technologies as the reflective mode can use a silicon wafer as a substrate and they have good reflection ratio due to metal electrodes deposited on the silicon

wafer. Inorganic or organic electroluminescent (EL) devices can fall into the self-luminous microdisplay category. An inorganic EL (eg., LETFEL[63]) prototype and OLEDs have been developed. In particular, OLEDs are expanding their range of applications such as microdisplays, flexible displays and desktop or home applications. The Microdisplay's category and its applications are summarized in Table 2-2 and 2-3, respectively.

Table 2-2 The classification of Microdisplay Technologies[61]
(for the manufacturers of Microdisplay devices, refer to reference[64])

Microdisplay Technology	
Transmissive	HTPS
	Silicon-on-Insulator(SOI)
Reflective	LCoS TFT LCD
	DMD/DLP
	GLV
Self-luminous	Inorganic EL(LETFEL)
	OLED

Table 2-3 Typical applications of Microdisplay devices[61]

Microdisplays	Applications
View Finders	Camcorders, digital cameras, mobile phones, PDAs (personal digital assistances), PMPs (personal multimedia players), and digital binoculars
Head-Mounted Displays (HMDs)	Military, Virtual Reality(VR) – Gaming and Surgery,
Head-Up Displays (HUDs)	Vehicles and airplanes
Front Projector	Business conference/presentation, Home Cinema, Control/Console room (eg, military, space shuttle, or airports)
Rear Projector	Projection TVs, Business conference/presentation, Control/Console room (eg., military, security, or airport)

2.2 Electroluminescent Displays, Classification and History

Various display technologies discussed in the previous section can be categorized as several subgroups according to their display nature: ① emissive (i.e. self-luminous) or non-emissive ② solid, liquid or gas state ③ organic or inorganic ④ direct- or indirect view ⑤ luminescence types; electro-, photo-, or cathodo-luminescence. Among these categories, it is common that displays are subdivided into emissive or non-emissive systems. As emissive displays, there are several systems: cathode ray tubes (CRTs), plasma display panels (PDPs), field emission displays (FEDs), organic/light emitting diodes (O/LEDs) and electroluminescent displays (ELDs), while liquid crystal displays represent the most significant non-emissive display system. A general classification of electronic information display technology is shown in Figure 2-13. In the classification, the dotted arrows indicate the technologies are currently in progress and the line arrows mean developed and available technologies.

Electroluminescent Displays (ELDs)

Once, inorganic electroluminescent display technology was considered as one of the promising display devices after Inoguchi's study[65]. Like a CRT, EL phenomenon and its display have such a long history. In 1907 and 1923 Round, H J and Losev, O V discovered luminescence from crystalline materials, respectively.[2] After that, Prof Destriau[66,67] at University of Paris observed EL phenomena from ZnS:Cu *polycrystalline* materials when a high electric field was applied to the sample. This was the first scientific description on EL phenomena. About 40 years later, in 1978 Sharp Co.(Japan) demonstrated a 240 × 320 line thin film electroluminescent (TFEL) monochromatic TV at Consumer Electronics Show (CES), US. In 80s and 90s, Sharp (Japan) and Planar(Finland and US) manufactured TFEL panels as major suppliers in mainly special applications market for medical and military usages. A Canadian manufacturer, iFire, demonstrated a 34 inch full-colour TDEL(Thick Dielectric EL) display prototype for HDTV at SID conference at Seattle in May 2004. According to iFire's plan in mass production, for the first time a commercial full-colour EL-based TV screens for HDTV will be launched in 2006.

Since the discovery of EL phenomenon, EL has about a 100-year history. The major milestones in EL technology development history are shown in Figure 2-14[1,2]. The Figure includes some EL-related devices – inorganic EL, organic EL and LEDs – development.

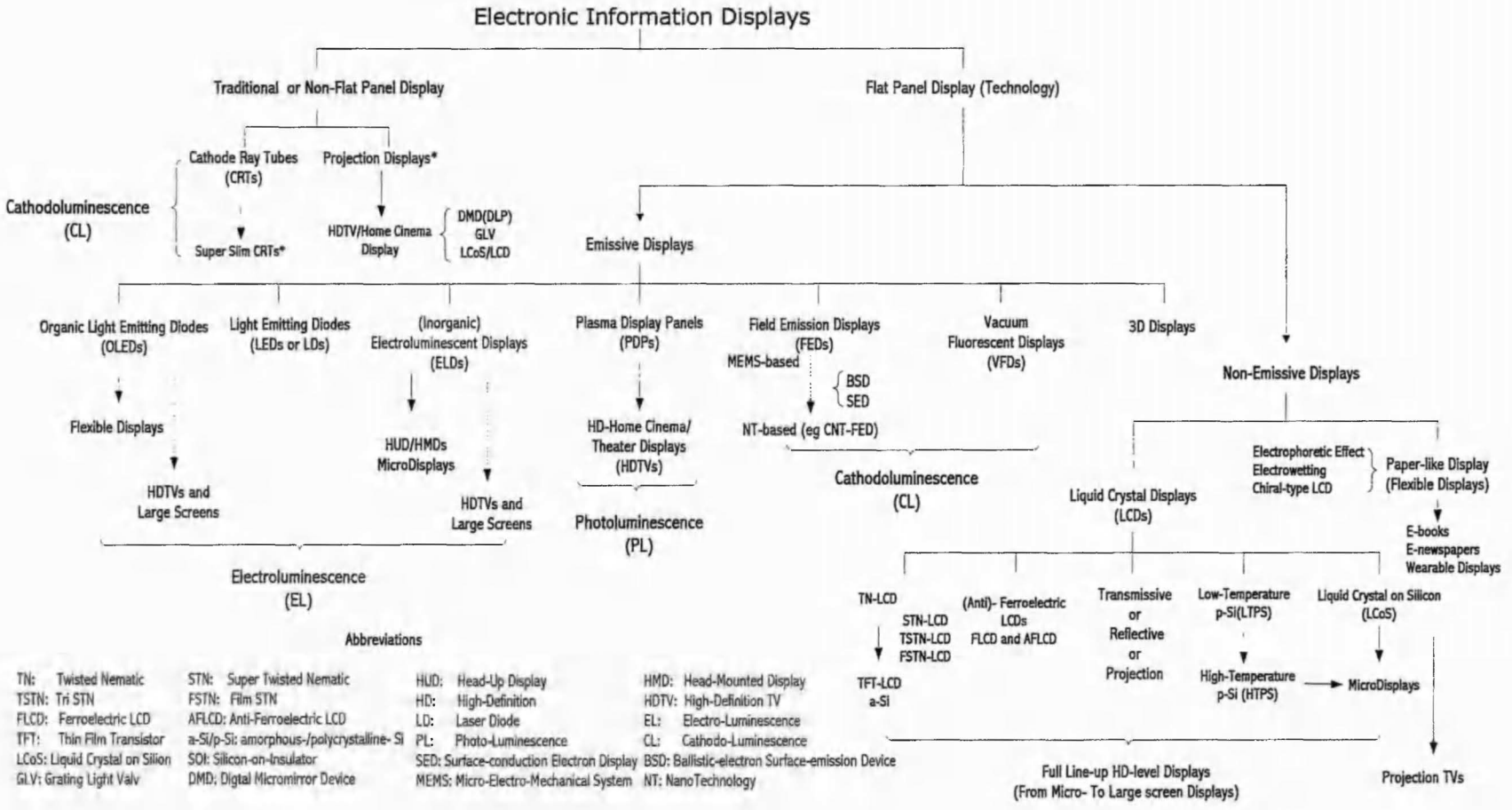


Figure 2-13 A general classification of the electronic information display technologies[1,2,4,146]

* Projection displays, super slim CRTs and other technologies can be overlapped with other categories due to the different point of views and their applications.

Figure 2-14 A brief timeline of major development milestone in EL technology[1,2]

Figure 2-15 visualizes a simple classification of electroluminescence-based devices - ELDs, LEDs and OLEDs according to excitation mechanisms, materials, driving voltage types and device types. Inorganic TFEL display devices have been reported to have the following advantages[1,2,4,16,68]: ① full solid-state device, which means that they are not affected by external environment such as temperature, so they can guarantee stable operation even in extreme weather conditions and regions, ② wide view-angle(>170 degree), ③ fast response time, which makes EL devices more suitable for displaying multimedia information, ④ self-luminous, or emissive device, so they do not require an additional light source such as a backlight unit in LCD devices, hence TFEL devices are more energy efficient, ⑤ simple fabrication processing, which can reduce the total cost of the device manufacturing, and hence has price competitiveness.

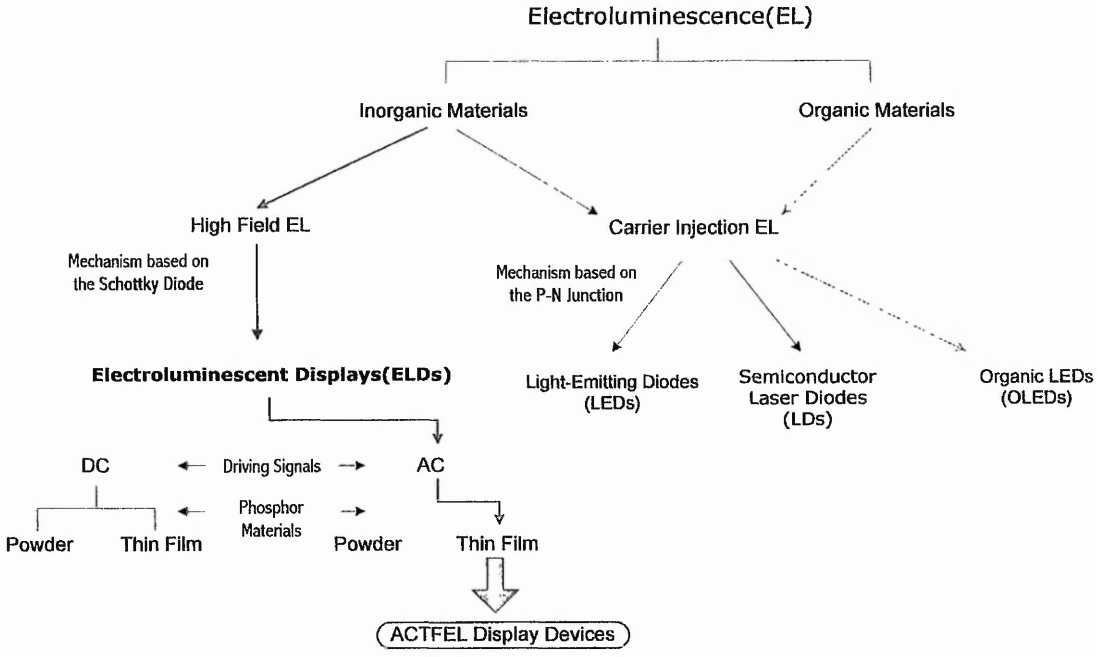


Figure 2-15 Sub-classification of electroluminescence (EL) and mechanisms among various display devices

Meanwhile, the inorganic EL devices have two important technical obstacles to be solved: ① a

high driving voltage (also termed "turn-on voltage" or "threshold voltage")# and ② suitable blue phosphor materials. In terms of the driving voltage of the TFEL devices, the voltage is normally in the range of 150 ~ 300 V to operate the EL device under saturated brightness. The driving voltage is relatively high for personal portable electronics compared to that of other flat panel display devices. Hence this causes high power consumption and raises the cost of driving circuits. As one of the solutions to tackle the current driving voltage problem in inorganic EL device, many researchers and engineers have been trying to find more suitable insulating materials with high dielectric constant (or high-κ, relative permittivity) to lower the driving voltage. The high-κ dielectric material should have the following properties: low leakage current, high breakdown strength and good adhesion to a substrate and neighbouring thin films. The importance of the insulating layer/thin films in EL device will be discussed in the following sections – TFEL and dielectrics, respectively.

Although phosphor materials of red (R) and green (G) among three primary light sources[69] were developed, blue phosphor materials for inorganic TFEL devices are not fully developed. As a result, lack of proper blue phosphor materials for inorganic TFEL devices has delayed full-colour EL display devices. Prototype full-colour EL devices have been developed by Planar and Sharp, but practical EL devices have been suffering from the lack of reliable blue phosphor materials. Currently iFire has started to operate a pilot production for manufacturing the full-colour TDEL screen panels. The TDEL devices are fundamentally based on EL theory and architecture, but they use a thick dielectric layer instead of a thin dielectric layer for the TFEL devices.

In order to realize a full colour inorganic TFEL device, developing blue phosphors among other primary phosphor materials is, needless to say, the most important factor. As a solution, white light-emitting phosphor materials were used with a blue colour filter (so-called "colour by white" method[70,71]), alkaline-earth sulphide(AES)-based phosphors (SrS:Ce[72,73,74], SrS:Cu[75,76,77], or SrS:Cu,Ag[78,79,80]), and GaN:Eu[81] for blue phosphors have been studied actively as promising candidates. For the TDEL device, a $BaAl_2S_4$:Eu[82] blue phosphor was developed. More details for phosphor materials will be discussed in the phosphor section in this chapter.

In definition, often turn-on voltage and threshold voltage have different meaning, but sometimes they can be interchangeable. The threshold voltage may be defined by a voltage corresponding to a luminance of 1cd/m^2.

2.3 Thin Film Electroluminescent (TFEL) Devices

The TFEL device has a simple sandwich structure with phosphor (or active) layers between two insulating layers. It is also called an MISIM (Metal (ITO) - Insulator (lower, or bottom) - Semiconductor (phosphor) - Insulator (upper or top) - Metal (Top)) structure. The typical ACTFEL device structures are shown in Figure 2-16. For EL device substrates, a transparent glass or a silicon (Si) wafer is mainly used. ITO electrodes (for glass substrate), the first (bottom) insulating layer, luminous centre-doped phosphor (eg ZnS:Mn for emitting yellow light) layer, the second(upper) insulating layer and finally the top electrodes (mainly Al) are deposited in order on the substrate by various deposition techniques such as sputtering(rf or dc)[83,84,85], chemical vapour deposition(CVD)[86], molecular beam epitaxy (MBE)[86], thermal evaporation[86], atomic layer epitaxy(ALE)[87].

According to the magnitude of the ac voltage applied to the EL device, there are two distinctive operational properties before and after turn-on (or threshold) voltage. Turn-on voltage is defined as the value of applied voltage when light emission just starts. A typical luminance vs. applied voltage (*L-V*) curve of the TFEL device is illustrated in Figure 2-17. Once the EL device starts giving off light emission, the phosphor layer will act as a conductor (i.e. electrically short circuit) so that the layer no longer has any dielectric (capacitive) properties and is thus lossy. When the magnitude of the applied voltage is below the turn-on voltage, the EL device is equivalent to a parallel plate capacitor with three stacked dielectric layers. In fact, the parallel plate capacitor having three stacked dielectric layers inside – two insulating and one phosphor layers - can be understood/substituted as a series connected capacitor network circuit. Commonly, the EL device is presented as a single capacitor with the capacitance of the EL device for simplification (See Fig. 2-16). However, in terms of the operational properties of the EL device mentioned above, we can possibly obtain a more suitable equivalent circuit of the EL device. The equivalent circuit is shown in Figure 2-18. More details in operational properties and dielectrics will be discussed later in the Dielectric and Ferroelectric section. In addition, the on/off conducting (or dielectric) properties of the phosphor layer require additional circuitry to explain the EL mechanism more properly. Therefore, a "back-to-back Zener diode" circuit should be attached to the capacitor in parallel[68].

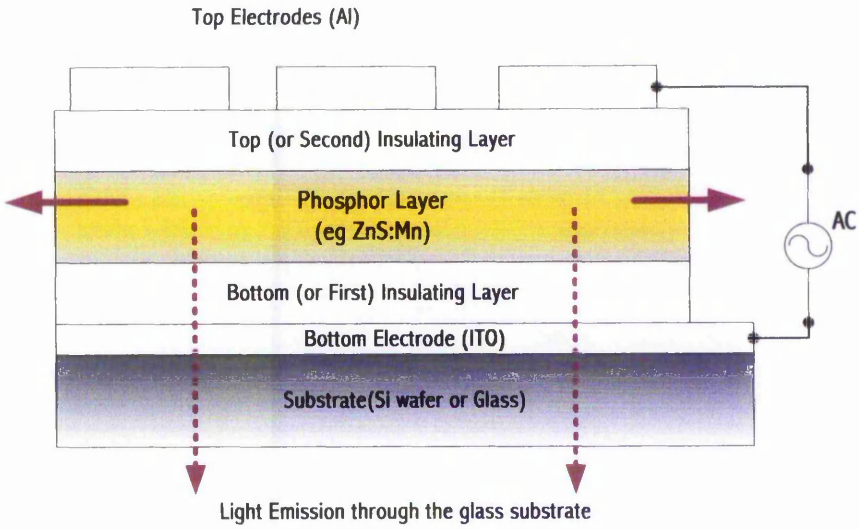


Figure 2-16 A schematic cross-section of typical inorganic ACTFEL test device structures

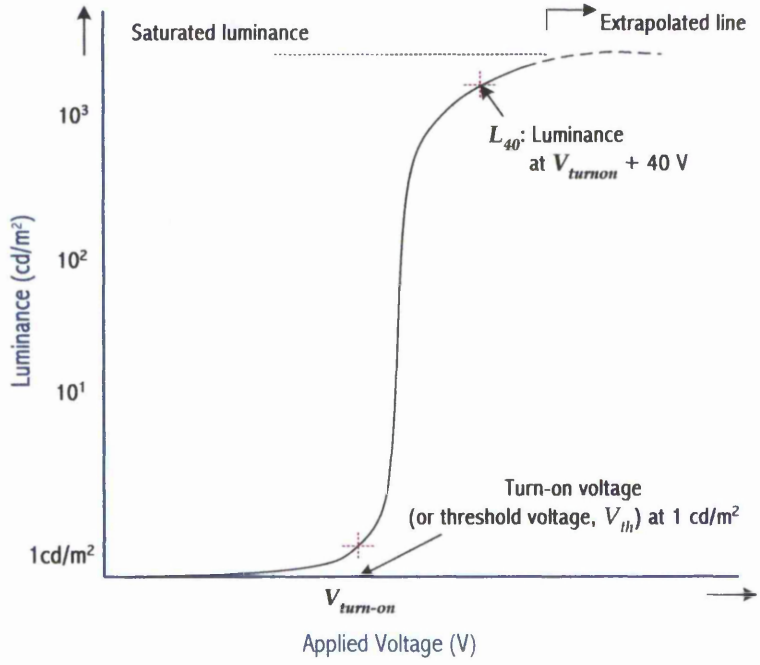


Figure 2-17 A typical luminance-applied voltage (L-V) curve of the TFEL devices[88]

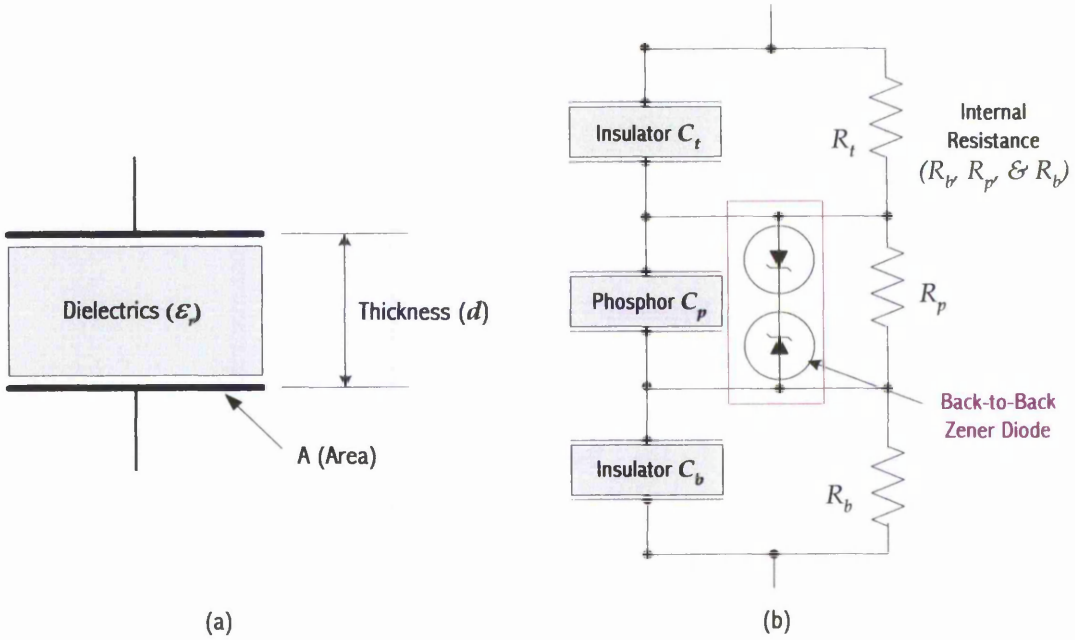


Figure 2-18 A parallel plate capacitor and the equivalent circuit of a TFEL device[68,89]

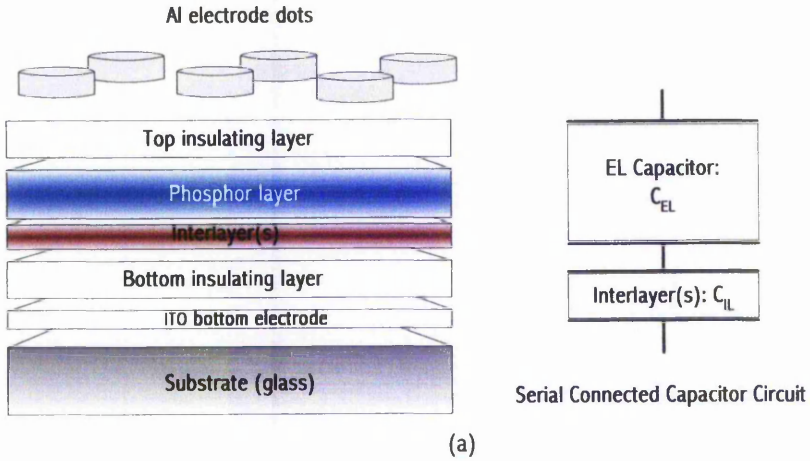
For light emission phenomena of EL devices, the general EL mechanism within the device can be easily and visually understood by using an energy-band diagram of EL device. First, at the interface between bottom insulating layer and phosphor layer, electrons, by ❶tunneling, are injected into the conduction band of the phosphor layer. By the high field within the phosphor layer, the electrons can be accelerated with an increase in energy, hence they are called, "❷hot electrons." The hot electrons then experience an energy transfer with their excess kinetic energy lost to host materials and activators (luminescent centers) during ❸ collisions (or impacts), while a ❹ multiplication process takes place by the means of collision. The energy transfer between host electrons and activators can occur so that the bound electrons of luminous centres are excited and the bound electrons can excite other bound electrons within the same atom. The events are ❺impact excitations (impact excitation and impact ionization look similar, but are different: impact excitation is a multiple internal process, but impact ionization excites the bound electron to be free)[90] by collisions. Finally, excited electrons return to the ground state and at the same time energy difference between the excited and the ground states ($\Delta E = h\nu = E_{es} - E_{gs}$; E_{es}-excited state, E_{gs}-ground state) emit as ❻light (photons). Meanwhile, the majority of electrons that did not participate in light emission (i.e. electrons with insufficient energy; lose their energies after collisions; or were not captured by luminous

centres) are ❼trapped at the opposite interface. These processes are repeated❽ continuously due to changing of the polarity of the ac applied voltage. Figure 2-19 shows a diagrammatic representation of the luminescence mechanism of TFEL device with ZnS-based phosphor layer.

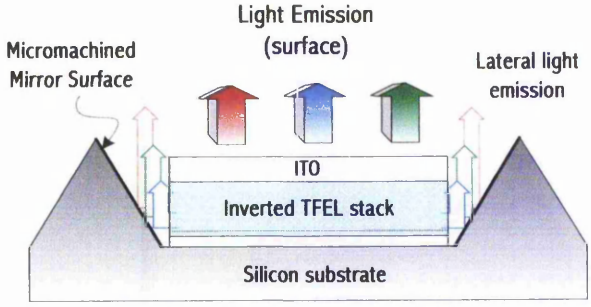
Figure 2-19 Visualized physical processes of light emission within ACTFEL devices[68]

Figure 2-20 shows three additional types of EL devices that have been investigated at NTU research team. There are typically four types of EL device structure. One of them is the conventional device structure shown in Figure 2-16 and the other is an interlayer structure that has generally one or more interlayer(s) between the bottom insulating layer and the phosphor layer in order to increase the brightness of the device. In fact, this device works like a series connection circuit of additional interlayer. Total capacitance can be lower than the individual capacitance of the layers, but if an appropriate high-κ dielectric could be selected, the structure can show better performance in terms of available charges at the interfaces. This effect will be

discussed later in this chapter. Figure 2-20 (b) shows a novel structure used to collect laterally emitted light using an "inverted EL device structure"[91,92] and the micromachining technology on silicon substrates. As mentioned previously, EL devices are formed by depositing multiple stacked thin film layers, which have the optical structure of a microcavity, due to the refractive index profile difference between phosphor and insulating layers. Because of this structure, EL has another difficult problem in increasing light output of the device. Generally, the active layer materials - ZnS, SrS - have a relatively large refractive index, around 2.2 (See Table 2-4). So EL devices show a strong optical lightguide (ie, waveguide) effect, where the majority (90%) of output of light is confined laterally due to total internal reflection. Hence, to utilise this property, the inverted structure has been developed by the group at Nottingham Trent University (NTU). By using this inverted structure, it is possible to use opaque substrates such as silicon wafers. At Nottingham Trent University, Prof Thomas, Dr Stevens and Dr Cranton demonstrated the pioneering work on laterally emitting TFEL (LETFEL) devices.[91] In addition, the NTU research group demonstrated later by inserting the thin barrier layers within phosphor layer(Fig. 2-20(c)) can increase the stability and brightness of the EL device. This is called a barrier layer structure.

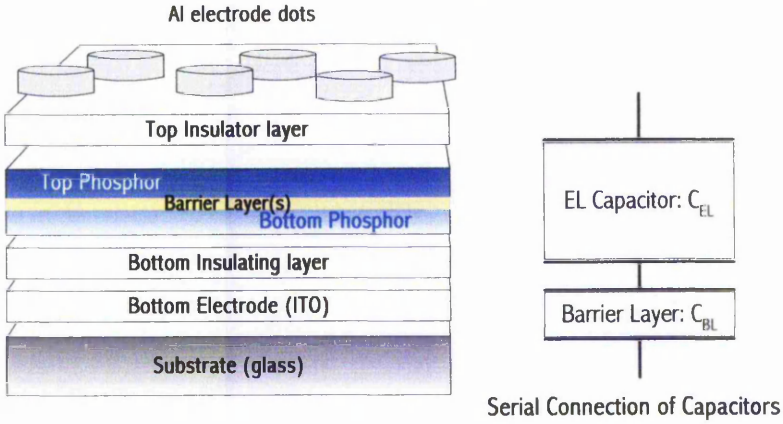


(a)



(b)

*Light colours depend on phosphor materials and activators



(c)

Figure 2-20 ACTFEL device structures used in investigations: (a) an interlayer structure, (b) an inverted structure on silicon and (c) a barrier layer structure

2.4 Dielectrics and Ferroelectrics

The function of dielectric materials, or insulators depends on their applications. In microelectronic circuit and semiconductor application fields, there are two different dielectric materials in use - low-κ and high-κ. Generally, insulating materials are used for supporting and isolating some components of an electrical circuits from each other and from the earth(i.e., ground). For this case, their capacitance should be as small as possible. In addition, they have suitable mechanical, chemical and heat-resistance requirements. In microelectronic circuits, many active attempts of scaling down the size of the components in integrated circuits (ICs) have shown improved performance efficiency, yield of the devices and much more cost-effective in manufacturing. As the device dimensions go down to submicron scale, the resistance-capacitance time constant (or RC delay time, τ) is the major factor to impact performance of ICs. The RC delay time is controlled by two parameters: the resistance of the metal lines in the interconnect structure of the ICs and the capacitance between the metal interconnection lines. To reduce the resistance and the capacitance, respectively, many means to find other new materials have been investigated. Therefore, instead of aluminium (Al), the copper (Cu) interconnection technology was introduced because the copper has 37% lower resistivity than aluminium. For the capacitance, SiO_2 (κ =3.9 ~ 4.1) was replaced by fluorinated silica (FSG, κ= 3.7) in the mid-90s to reduce the capacitance, but attempts of reducing capacitance still continue. As a result, low-κ dielectric materials are necessary to reduce the capacitance.

On the other hand, if the insulating materials act as a dielectric in a capacitor, high-κ dielectric materials are more advantageous and effective in terms of realising a capacitor for charge storage. According to the International Technology Roadmap for Semiconductors (ITRS) report[93], the equivalent oxide thickness(EOT) of classical and non-classical complementary metal-oxide-semiconductor(CMOS) IC technology and dynamic random access memories(DRAMs) will be 1.0 nm requirement (for physical thickness; 1.7 nm for electrical EOT[93]) by 2006. As the physical dimensions of the electronic devices are decreasing, the dielectric material of the capacitor in the device should have high dielectric constant. For under 15-Å-thick SiO_2 layers, the direct tunnelling of electrons and holes between layers increases and will be a dominant transport mechanism. As a result, the leakage current increases exponentially and finally it causes a failure or breakdown of the device. Hence, suitable high

dielectric constant materials need to be implemented fully compatible with Si wafers and its process. If the high-κ dielectric materials are applied and the capacitance of SiO_2 should be maintained at least, a simple equation for the thickness of high-κ dielectric material can be obtained from the parallel-plate capacitance equation:

$$C = \frac{\kappa' \varepsilon_0 A}{d} \quad (F) \qquad \text{Equation 2-1}$$
$$\varepsilon = \varepsilon' \varepsilon_0 = \kappa' \varepsilon_0$$

where C, d, $\kappa(=\varepsilon_r)$, ε_0 and A indicate capacitance, thickness, relative dielectric constant, permittivity of vacuum and the area of the capacitor, respectively. The permittivity of vacuum(ε_0) is 8.8542×10^{14} F/cm.

$$d_{high-\kappa} = \frac{\kappa_{high-\kappa} \cdot d_{SiO_2}}{3.9} \qquad \text{Equation 2-2}$$

where $d_{high-\kappa}$, $\kappa_{high-\kappa}$ *and* d_{SiO2} means the equivalent thickness of the high-κ dielectric material, dielectric constant(of high-κ dielectric) and the equivalent oxide thickness(EOT) of SiO_2, respectively.

Equation 2-2 means that 10 nm high-κ dielectric materials can replace 10 Å-thick SiO_2 layer effectively if the dielectric constant of the high-κ dielectric material are 39, for an example. So it can prevent the dielectric material and device's critical failure and breakdown from the quantum mechanical tunnelling effect which easily takes place in under 15 Å-thick SiO_2 dielectrics.

In terms of electroluminescent (EL) devices, a high-κ dielectric constant of the insulating material is one of the most important issues to improve device performance and operational stability. Under the capacitor structure, the relationship between dielectric thickness, dielectric constant and capacitance is based on Equation 2-1. As mentioned previously, the driving voltage of the EL device is high. Assuming that the same amount of charge is sustained, the capacitance of the EL device needs to be large in order to reduce its driving voltage (from Q =

$C \cdot V$). The capacitance and the dielectric constant are proportional from Equation 2-1. In other words, use of an appropriate high-κ dielectric material can reduce the applied voltage directly. In addition, as with CMOS and DRAM applications, by using the high-κ dielectric material the thickness of individual insulating layers can be reduced, if necessary.

From the theory of the capacitor, when a sinusoidal voltage source is applied across a loss-free (i.e., ideal) capacitor, a charging current (i_c) will be drawn. And the current leads the voltage signal by an angle of 90° in the phase relationship (Fig. 2-21).

$$v = v_o e^{j\omega t} \qquad \textbf{Equation 2-3}$$

where ω is the angular frequency (= $2\pi f$), j is the imaginary number ($j^2 = -1$), v_o is the maximum amplitude of the signal. The value of instantaneous capacitor current(i_c) directly relates to the amount of capacitance and the rate of change of voltage:

$$i_c = \frac{dQ}{dt} = C\frac{dv}{dt} = j\omega Cv \qquad \textbf{Equation 2-4}$$

In a real capacitor, there may exist loss current component (i_r)

$$i_r = Gv \qquad \textbf{Equation 2-5}$$

in phase with the voltage. G represents the conductance of the capacitor. Therefore, the total current traversing the real capacitor is

$$i_t = i_c + i_r = (j\omega C + G)v \qquad \textbf{Equation 2-6}$$

which is inclined by a *power factor angle* < 90° against the applied voltage, v. The electrical properties of the capacitor can be understood by a parallel connection between a capacitor and a resistor (See Fig. 2-21).

The dissipation factor, ***D*** (or loss tangent, tan δ) which is one of the important factors to evaluate dielectric materials is defined by the ratio of loss current (i_r)to the capacitor current (i_c):

$$D \equiv \tan\delta = \frac{i_r}{i_c} = \frac{1}{\omega RC} \qquad \textbf{Equation 2-7}^{[94,95]}$$

The loss tangent may not at all agree with that actually observed due to the conduction term which does not stem from a migration of charge carriers, but can represent any other energy-consuming process. It is customary to introduce a *complex permittivity* for understanding the existence of a loss current in addition to a capacitor current;

$$\varepsilon^* = \varepsilon' - j\varepsilon'' \qquad \textbf{Equation 2-8}$$

where ε' is real dielectric constant and ε'' is imaginary counterpart. By substituting the equation 2-7, the total current may be rewritten as

$$i_t = (\omega\frac{\varepsilon''}{\varepsilon_0} + j\omega\frac{\varepsilon'}{\varepsilon_0})C_0 v = j\omega C_0 \kappa^* v \qquad \textbf{Equation 2-9}$$

where $\kappa^* \equiv \frac{\varepsilon^*}{\varepsilon_0} = \kappa' - j\kappa''$ **Equation 2-10**

From equation 2-8, the loss tangent component can be obtained:

$$\tan\delta = \frac{\varepsilon''}{\varepsilon_0} = \frac{\kappa''}{\kappa'} \qquad \textbf{Equation 2-11}$$

The product of angular frequency and loss factor is equivalent to a *dielectric conductivity*, σ,

$$\sigma = \omega\varepsilon'' \qquad \textbf{Equation 2-12}$$

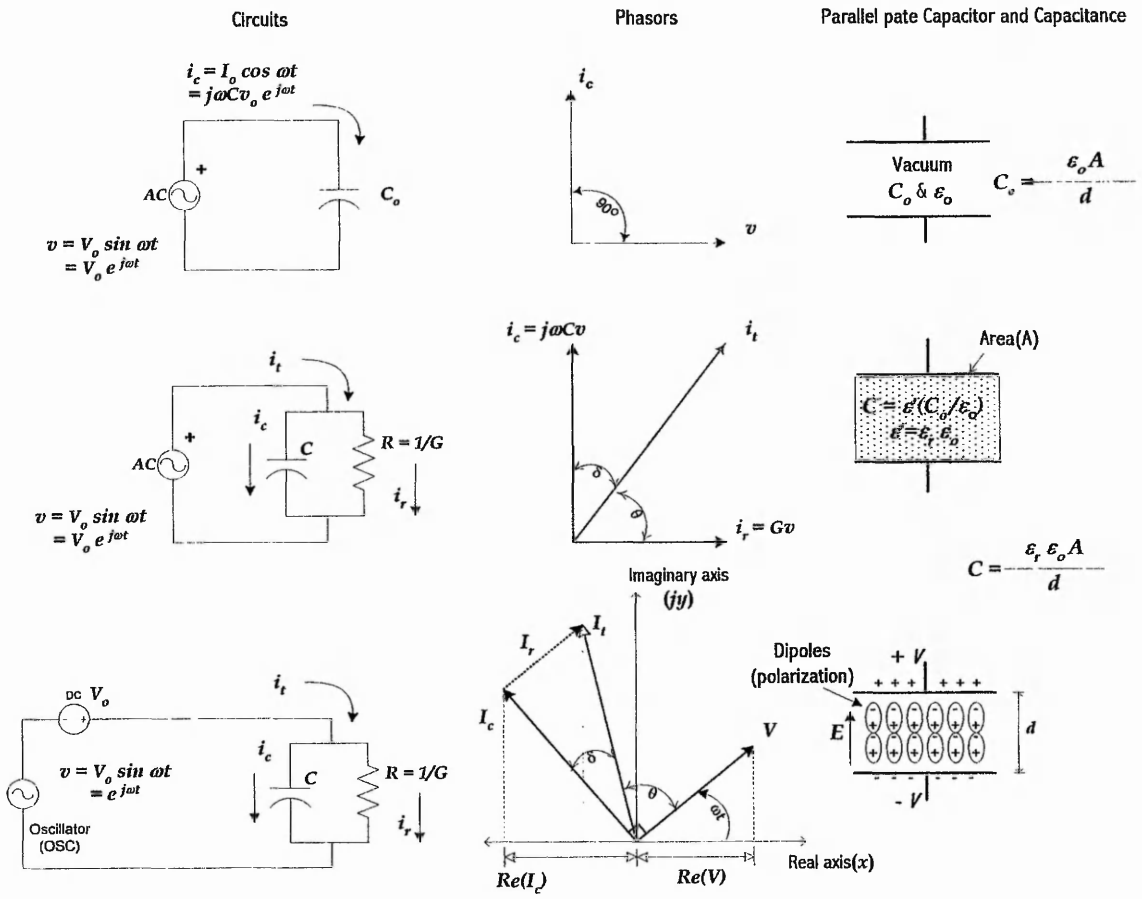


Figure 2-21 An ideal and real capacitor circuits, their phasor diagrams(impedance components), dipole polarization and geometrical capacitance relationship[95,] (Blue lines shows ac total impedance or total current.)[94,95]

In linear and isotropic dielectrics, the vector quantity - the dipole moment per unit volume ($\boldsymbol{P}$, C/m²), is obtained from the average vector dipole moment per molecule ($\boldsymbol{p}$): $\boldsymbol{P} = N\boldsymbol{p}$, where N shows the number of molecule per cubic meter. The dipole moment ($\boldsymbol{P}$) is proportional to $\boldsymbol{E}$ and in the same direction:

$$\boldsymbol{P} = \varepsilon_o \chi_e \boldsymbol{E} \qquad \textbf{Equation 2-13}$$

where χ_e is the *electric susceptibility* of the material.

In addition, total surface charges consist of bound charges and free charges. The free charges are induced by the electric field ($\boldsymbol{E}$) and the bounded charges on the surface induce dipole polarization ($\boldsymbol{P}$). The electric flux density, or electric displacement density ($\boldsymbol{D}$) is equal to charge density by electric field ($\boldsymbol{E}$) and polarization($\boldsymbol{P}$), respectively[96,97,98].

Thus, a general equation of the electric flux density ($\boldsymbol{D}$, electric displacement density) with polarization ($\boldsymbol{P}$) component is written as

$$\boldsymbol{D} = \varepsilon_o \boldsymbol{E} + \boldsymbol{P} = \varepsilon_o (1 + \chi_e)\boldsymbol{E} = \kappa' \varepsilon_o \boldsymbol{E} = \varepsilon' \boldsymbol{E} \qquad \textbf{Equation 2-14}$$

$$\text{or } \boldsymbol{P} = \boldsymbol{D} - \varepsilon_o \boldsymbol{E} = \varepsilon' \boldsymbol{E} - \varepsilon_o \boldsymbol{E} = (\varepsilon' - \varepsilon_o)\boldsymbol{E} = \varepsilon_o \chi_e \boldsymbol{E} \qquad \textbf{Equation 2-15}$$

where,

$$\chi_e = \frac{\varepsilon'}{\varepsilon_o} - 1 = \kappa' - 1$$

$$\kappa' = 1 + \chi_e = \frac{\varepsilon'}{\varepsilon_o} \qquad \textbf{Equation 2-16}$$

From Equation 2-14, when there is no polarization($\boldsymbol{P}$ = 0) ideally in the material, the equation can be rewritten as

$$\boldsymbol{D} = \varepsilon_o \boldsymbol{E} \quad \left(\because \varepsilon_o = \frac{\boldsymbol{D}}{\boldsymbol{E}}\right) \quad (\kappa' = 1 \text{ or } \chi_e = 0) \qquad \textbf{Equation 2-17}$$

Equation 2-17 is the definition of the electric displacement density ($\boldsymbol{D}$) when a material does not have any polarization. Meanwhile, Equation 2-14 means a general form when a material is polarized: $\boldsymbol{D} = \varepsilon' \boldsymbol{E}$.

Two electric charges with opposite polarity (± q) separated by a distance d represent the electric dipole moment;

$$\mu = qd \qquad \text{(from negative to positive)} \qquad \textbf{Equation 2-18}$$

The polarization vector $\boldsymbol{P}$ is identical with the *electric dipole moment* per unit volume of the dielectric material. Dielectric polarization is shown schematically in Figure 2-22.

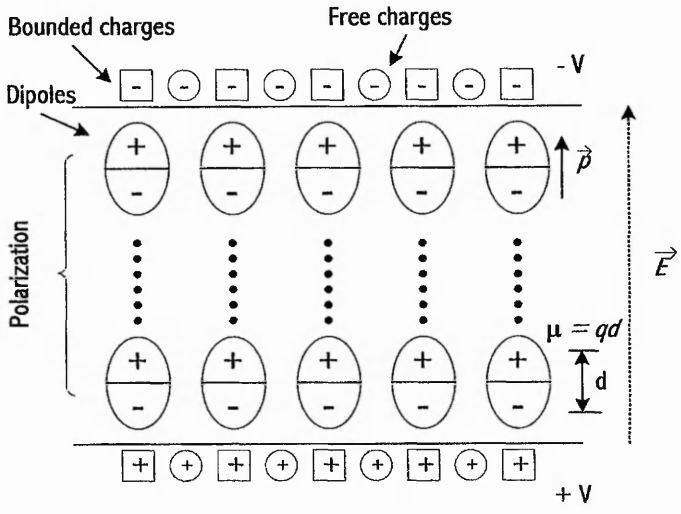


Figure 2-22 Schematic diagram of dielectric polarization and the electric dipole moment[97]

As with magnetism, the microscopic electric properties of dielectric materials can be categorized into three subdivisions: ① (simple) dielectrics, ② paraelectrics and ③ ferroelectrics. Simple dielectrics can be explained as materials where an applied field can create dipole polarization inside the dielectrics, but in the absence of the applied field the induced dipole polarization by the applied field disappears and returns to its original free random states. Some dielectrics have permanent dipoles without any external field. This is the class of material called paraelectrics. Finally, ferroelectrics have nonlinear dipole polarization/orientation whether an external field exists or not. The term, ferroelectric or ferroelectrics, has a reason for this denomination and was coined due to a similarity of the ferroelectric behaviours of the materials with that of ferromagnetism. In ferromagnetism, the *prefix*, ferro-, means a material containing iron(Fe) elements. However, ferroelectric materials have nothing to do with iron practically. Simply, due to the similarities in relationship between ***M***(magnetization) vs ***H***(magnetic field) and ***P***(polarization) vs ***E***(electric field), the ferromagnetic materials exhibit a spontaneous magnetization and hysteresis effect and the ferroelectric materials show a spontaneous (electric) polarization (P_s) and hysteresis effect, too. Usually, the spontaneous polarization and hysteresis phenomena are observed in a specific temperature (i.e., critical temperature) region that depends on the materials and is called *Curie temperature* (T_c). The Curie temperature is considered as the transition point between the

ferroelectric and paraelectric region[96]. At temperatures well below the *Curie temperature*, electric dipoles are well oriented, but at temperature above T_c, the ferroelectric nature will be lost, so the materials no longer have ferroelectric properties above the Curie *temperature* and show just normal dielectric behaviour[99]. Due to temperature-dependence, the dielectric constant of a ferroelectric obeys the Curie-Weiss law[100] near the transition:

$$\varepsilon = \varepsilon_o + \frac{C}{T - T_o} \cong \frac{C}{T - T_o} \qquad \text{Equation 2-19}$$

where C is the *Curie* constant and T_o the Curie-Weiss temperature. T_c and T_o is different, but in certain ferroelectrics they are coincident.

Unlike a dielectric, the ferroelectric materials have multiple domains which are regions that have their own different dipole orientations. As an energy barrier exists in semiconductor devices, a small energy difference(ΔE) between domains normally exists. Besides, the energy level of each domain in ferroelectric material is considered the lowest stable energy level if there is no external applied stress, such as heat or electric field.

As mentioned above, the spontaneous polarization is the most important factor in ferroelectric phenomenon. Unlike simple dielectric materials, the ferroelectric materials have the tendency of holding the polarization after removing applied electric field. Of course, the magnitude of the polarization can be a different value. In ferroelectric materials, the relationship between the polarization and the applied electric field has non-linear characteristics. In other words, the characteristic pattern of the relationship between the polarization and the electric field is not reversible even though a short term electric field scale the ferroelectric materials can show linear behaviours. That is called the hysteresis property of ferroelectric materials which is shown in Figure 2-23. In the figure, it shows a polycrystalline and single crystal ferroelectric hysteresis, respectively. At the highest electric field intensity, the polarization is saturated and at this moment all the domains are aligned in the direction of the applied electric field. The saturated polarization(P_s) can be obtained by extrapolation of the hysteresis curve to y axis (polarization axis). When the applied electric field is removed, the remaining polarization is called the remanent polarization(P_r). This can take place when induced oriented domains do

not return to their previous random positions fully after removing the electric field. By applying additional negative or positive electric field, the domains can be returned to zero polarization state. This additional opposite electric field is known as the coercive field(E_c). These three parameters, P_r, P_s and E_c, are commonly used in the hysteresis curve.

The crystal symmetry, particularly the point group, is another important parameter to identify certain materials which have ferroelectric properties or not. According to the crystallographic crystal symmetry by the point group, there are a total of 32 different crystal symmetry classes in a 2 dimensional point of view. In order to have ferroelectric properties within certain materials, the materials should have non-centrosymmetric property fundamentally and the ferroelectric material must have pyroelectric and piezoelectric properties, respectively, as prerequisites. Logically, to become a pyroelectric or piezoelectric material, the ferroelectric material/property is a sufficient condition. Figure 2-24 shows the hierarchical classification of the ferroelectric materials in the 32 crystallographic symmetry crystals by the point group.[101]

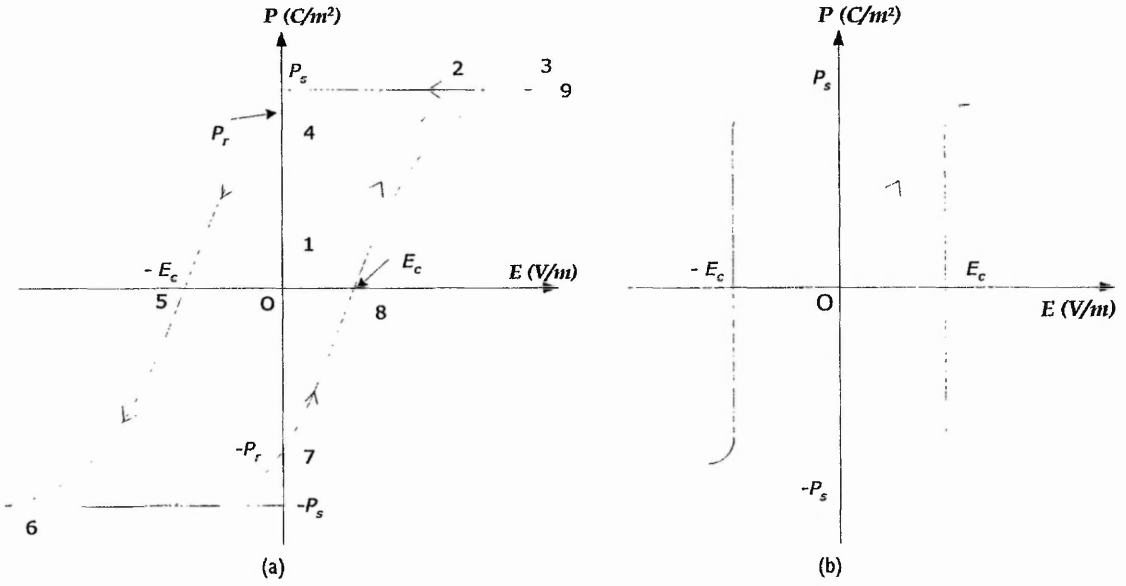


Figure 2-23 Typical hysteresis curves of poly- and single crystalline ferroelectric materials[100]

It will be good to discuss unique differences between piezoelectric and pyroelectric basic properties for understanding ferroelectric materials better. In 1824, Brewster[101] coined the term 'pyroelectricity' for the first time after his various experiments and then Lord Kelvin[101] mentioned pyroelectricity resulted from permanent polarization. In fact, the pyroelectric effect is related to the temperature coefficient of this polarization. Therefore, the pyroelectric effect has a close relationship with an interaction between electrical and thermal systems. While the piezoelectric effect was discovered by Pierre and Jacques Curie[101] in 1880, Hankel suggested the name 'piezoelectricity.' Piezoelectricity comes from an interaction between electrical and mechanical stress(i.e., pressure). The direct piezoelectric phenomenon is the electric polarization by mechanical stress. On the contrary, when the electric field applied, a crystal becomes possibly strained. The prefixes, *pyro-* and *piezo-* mean "fire" and "press", respectively and are derived from the Greek words.

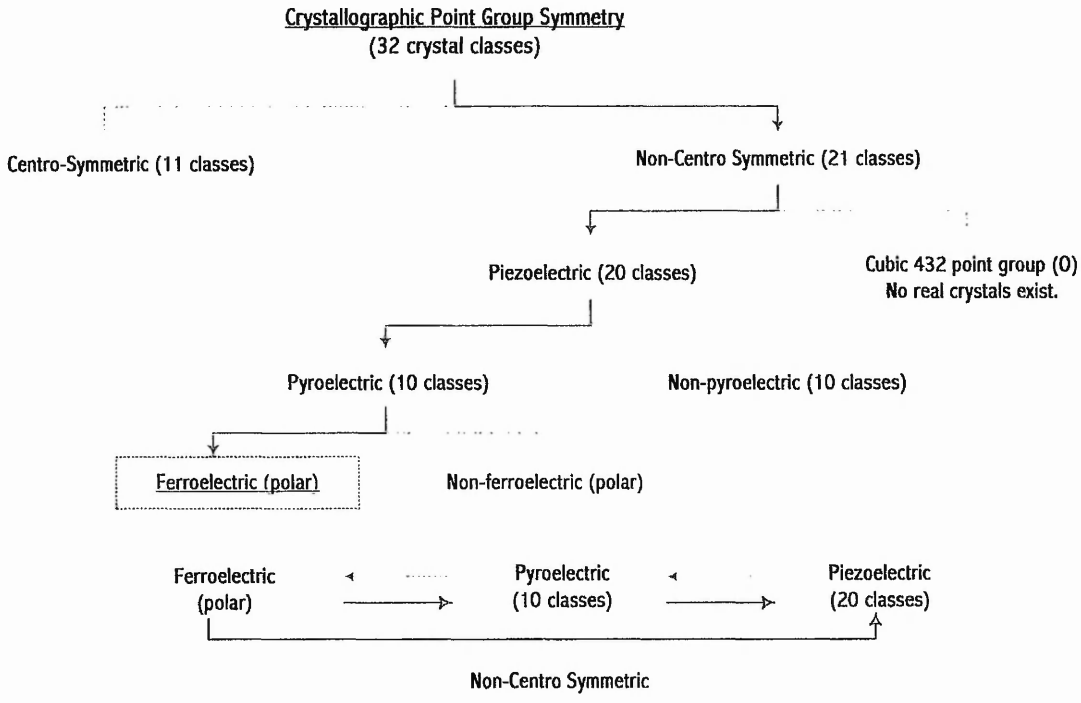


Figure 2-24 Ferroelectric classification by 32-crystallographic crystal symmetry
(Black solid arrows indicate a possible subset relationship from left onto right, but purple dotted arrows show a case-dependent subset) [101]

There are many types of ferroelectric materials classified according to various specific conditions such as structure, elements and others. Generally the ferroelectric materials include

electro-ceramics†, polymers and ceramic-polymer composites, but in this section of the chapter, only the structure containing repeated oxygen octahedral surrounding another type of ion - usually transition metals like Zr or Ti, are considered. This is the well known perovskite structure with the general formula ABO_3 (A = Ba, Ca, Pb, or Sr; B = Zr or Ti) format. The typical perovskite-type ferroelectric material structures (2D and 3D) are shown in Figure 2-25. The movement of Ti^{4+} ions (see Fig. 2-25 (a)) within the oxygen octahedral structure (i.e., TiO_6 from BO_6) normally causes ferroelectricity in ABO_3 format perovskite materials due to the created structural transformation (orientation) by the movement.

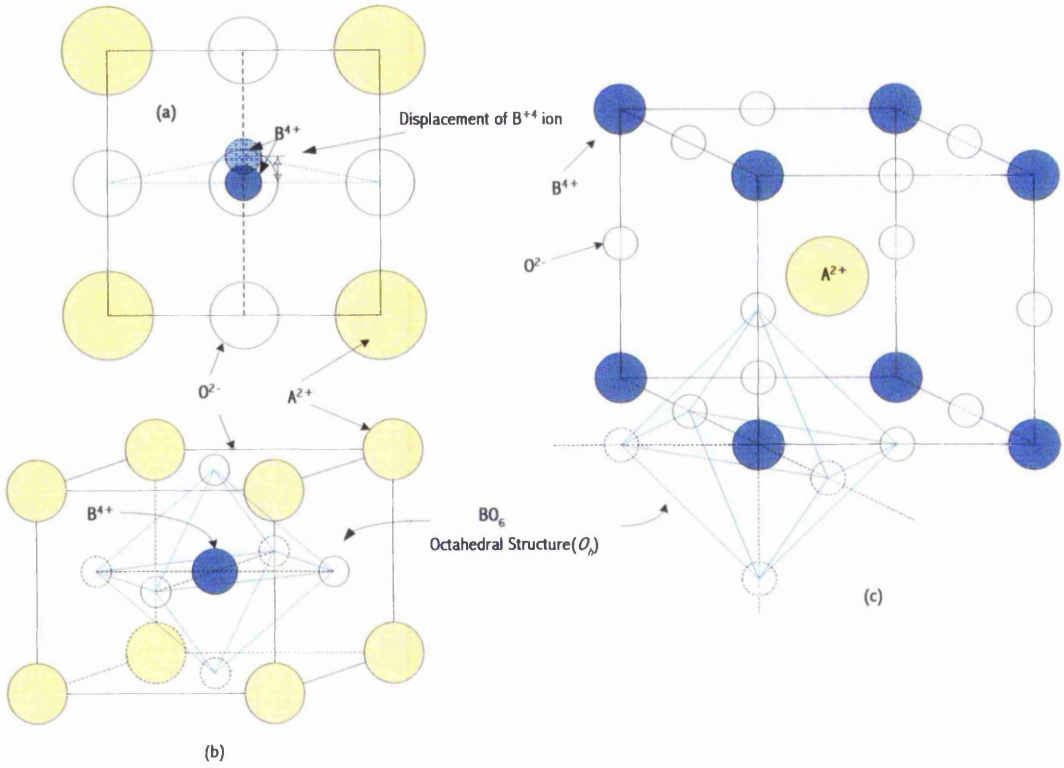


Figure 2-25 ABO_3 formula perovskite-type structures: (a) Schematic displacement of B^{4+} ion (on projection of (001) plane, (b) structural elements with octahedral coordination (BO_6) and (c) cubic structure of ABO_3 showing oxygen octahedron, BO_6 (12-fold coordination of A atom by O^{2-}) [100,101,102]

† The word, ceramic or ceramics, means non-metal generic dielectric materials. So it could be used as a generic term for dielectrics. In this thesis, it means simply dielectric material for electric devices or components. Source: Britannica Encyclopaedia

2.4.1. Role of insulating layers in TFEL devices

In terms of the operation mechanism of the EL device, the bottom (lower) and top (upper) insulating layers play a very important role. First, these insulating layers act as cladding materials and can protect the degradation (i.e. breakdown) of the phosphor layer. Secondly, they can act as a current controller. Thirdly, they are holding charges as a carrier provider so they can enhance the internal electric field and efficiency in luminescence. And finally, when the EL device emits light in the laterally emitting TFEL (LETFEL) device, the cladding layers (or insulating layers) can help laterally emitted light in the phosphor layer transfer more easily as a form of optical waveguide (see Figure 2-5). Hence, the optical characteristics, particularly the refractive index of the dielectric (or insulating) layer has important significance. To propagate the emitted light laterally in the phosphor layer without loss of light intensity or with minimum loss, generally the index of the cladding (insulating layer) is lower than that of the phosphor layer[103].

From the fundamental relationship of a capacitor, because capacitance and applied voltage has a reciprocal relationship ($Q = CV$), in order to get the constant amount of transferred charge density in the EL device, the applied voltage can be reduced if a higher capacitance could be used. In other words, the capacitance is in proportion to the dielectric constant, or dielectric permittivity. Therefore, high-κ dielectric materials[104,105,106] can reduce effectively the applied driving voltage to the EL device, which is a key issue with these devices, due to the cost and complexity of high voltage drive electronics.

In general, insulating layers between two materials are supposed to isolate these materials effectively. Similar to this, in EL devices, even when high voltages are applied to the device, both insulating layers should prevent current flowing between the electrodes. Considering the high electric field applied, the insulating layers are consequently required to have high dielectric breakdown strength (E_{bd}). The dielectric breakdown strength can be defined as the highest field that the dielectric (or insulating) materials can hold without internal and external breakdown of the materials.[96] The dielectric breakdown strength is thus the one of major parameters to be assessed for suitable insulating layers - along with the dielectric constant as already mentioned above.

To evaluate the overall dielectric thin films, a figure of merit (FOM), or charge storage capacity (C.S.C.) of the dielectric thin films is used. The figure of merit, or charge storage capacity is simply the product of the dielectric constant ($=\varepsilon_r \cdot \varepsilon_o$; F/m) and breakdown strength (= E_{bd}; *V/m*):

$$\text{FOM or CSC} = \varepsilon_r \cdot \varepsilon_o \cdot E_{bd} \ (\text{C/cm}^2 \text{ or C/m}^2) \qquad \textbf{Equation 2-20}$$

In fact, according to the unit of Equation 2-20, the equation determines the charge density per unit area(cm^2), which represents the maximum possible transferred charges or trapped charges that can contribute to the mechanism at the interface between the insulating and phosphor layer. Typically, the charge storage capacity of the dielectric thin films should be 3 ~ 4 $\mu C/cm^2$ and more[107] in order to withstand the typical operating fields used in TFEL devices. This condition is one of the criteria[108] for selecting dielectric materials for alternating-current thin-film electroluminescent devices.

In addition to these characteristics, the dielectric thin films used in EL devices should have good adhesion between neighbouring materials such as electrodes, substrate and phosphor materials. Good adhesion largely depends on the lattice constants between two materials. These thin film qualities also depend on deposition process parameters and methods used to each film in the device.

2.4.1.1 Yttrium Oxides (Y_2O_3) for TFEL devices

Yttrium oxide is one of the cubic bixbyte materials with Mn_2O_3 structure[109]. Historically, yttrium oxide materials are well known and have been used as very important electronic materials for a long time. Yttrium oxide materials have been known to have high dielectric constant (~ 20), high resistivity, high breakdown strength and chemical and thermal stability typical of rare earth oxides[110,111]. Yttrium oxides have been considered as interesting materials for optical coatings, storage dielectrics of DRAMs, gate dielectrics of MOSFETs, phosphor of CRT and EL devices (eg, Y_2O_3:Eu for red) and infrared laser materials of yttrium-compounds (eg. Yttrium-Aluminium-garnet). The basic properties of the yttrium oxides and other

important dielectric and ferroelectric thin films are shown in Table 2-4.

Table 2-4 Physical and electrical properties of insulating materials (thin films)[105,112]

Material	Refractive Index	Energy Bandgap (eV)	Breakdown Strength (MV/cm)	Dielectric constant	Ref
Y_2O_3	1.9	5.5	3.85	10 ~ 18	[113, 114]
SiO_xN_y	1.5 ~ 2.1	5.1	9 ~ 26	3.9 ~ 7	[115]
Al_2O_3	1.5	8.7	7	8.5 ~ 10	[116,, 117]
Ta_2O_5	2.2 ~ 2.5	4.2	4.5	25~6	[118]
Si_3N_4	2.1	5.1	10	7.5	[119]
$BaTiO_3$	2.4	2.5 ~ 3.9	0.42	300 ~ 2000	[120, 121, 122]
$SrTiO_3$	1.9 ~ 2.2	3.6	0.3 ~ 4	150 ~ 400	[120,122,123]
$(Ba,Sr)TiO_3$	2.1 ~ 2.4	3.2 ~ 4	4	160 ~ 870	[120,121,122,123]
SiO_2	1.4 ~ 1.5	8.9	10	3.9 ~ 6	[113]

To use within TFEL devices as the insulating layer, the thin film should ideally have a high dielectric constant (ε_r), high breakdown strength and low leakage current density[124]. For Y_2O_3 thin films deposited by the NTU group, the properties of $\varepsilon_r \approx 16$, $E_{bd} = 3.85$ MV/cm^{-1} and 2.52×10^{-12} A/cm^{-2} in rf magnetron deposition[107] have been demonstrated through capacitance vs voltage (*C-V*) and current vs voltage (*I-V*) measurements. Also, the refractive index of the yttrium oxide (Y_2O_3) thin film prepared by rf magnetron sputtering was 1.91. Results show that the dielectric constant (ε_r) was decreasing when the substrate temperature was increasing from room temperature to 190 °C. Generally, the dielectric constant of a medium is related to the electric susceptibility (χ_e), i.e., $\varepsilon_r = 1 + \chi_e$ (from Equation 2-16). The susceptibility is the ratio of the bound-charge density to the free charge density[125]. Therefore, decrease of the dielectric constant can be explained as the free charge density being increased due to the increased substrate temperature, and then the electric susceptibility decreases. However, fundamentally the dielectric constant and electric susceptibility depend on the properties of the medium and whether they are linear, isotropic or anisotropic[98,125].

Although the dielectric constant decreased, other parameters such as dielectric strength and leakage current density were improved with higher deposition temperature and the charge

storage capacity or figure or merit (FOM) of the yttrium oxide thin films was increased from 4.02 to 5.55 μC/cm².

In thin film deposition processes, the substrate temperature, deposition method and annealing time and temperature strongly affect the overall properties of the thin films. Without additional annealing process, Cranton, W. *et al.*[107] could have the yttrium oxide thin film with good stoichiometry at low temperature by rf magnetron sputtering deposition. Other yttrium oxide thin films grown by rf magnetron sputtering[114,126,127,] can be comparable to the above results. Similar results of the Y_2O_3 thin films can be seen in other papers although the films are prepared by different deposition techniques - resistive evaporation[111], or pulsed laser ablation[110]. The properties of the Y_2O_3 thin films prepared by e-beam show a lower dielectric constant than those of other-technique for depositing Y_2O_3 films[128,129]. But the quality in terms of the yttrium oxide thin films mentioned above is better than that of silicon oxides, so it shows the possibility of insulating layer in EL device and other electronic devices.

The crystalline orientation of the yttrium oxide thin films on a Si substrate is independent of the substrate orientation[109]. However, the orientation is dependent on the substrate temperature. If the substrate temperature is lower than 350 °C, the yttrium oxide thin films have amorphous and partially polycrystalline orientation. The yttrium oxide thin films grown in the range from 350 °C to 900 °C showed (111) dominating orientation polycrystalline[110,127,130]. At 800 °C, the films have only (111) orientation[109]. If the interfacial layer is inserted between silicon substrate and yttrium oxide films, the crystalline orientation of the yttrium oxide films depends on that of the interfacial layer.

An annealing process normally can improve the crystalline quality of the thin films. For example, by using the rapid thermal processing (RTP) at 850 °C in an oxygen atmosphere, the properties of Y_2O_3 thin films are improved[127]. For annealing the Y_2O_3 thin films, Ar or oxygen gas is used, the thin films in Ar or O_2 showing better characteristics than as-deposited thin films and *I-V* and *C-V* characteristics of the Y_2O_3 thin films annealed in O_2 are found to be better than in annealing in Ar[130].

In terms of lattice size difference between the substrate and the Y_2O_3 thin films, a silicon substrate is the best one for the Y_2O_3 thin films. The lattice constant of silicon is 5.43 Å, but 2 ×

a(Si) = 10.86 Å, while the lattice constant of yttrium oxide is 10.60 Å. Therefore, silicon and yttrium oxide can be closely matched (~ 2% mismatch) to each other[109,128,131].

The inherent crystalline nature of yttrium oxide can cause the EL device to be sensitive to moisture and ionic intrusion. Besides, yttrium oxides showed nonuniformity in the crystallinity when they were deposited on the top of the phosphor layer. This nonuniformity can lead to non-uniform luminance and stability in brightness of the EL device. In addition, yttrium oxide deposited on ITO has been reported to be a highly defective thin film. When post-annealing treatment was made, it showed sensitivity to the annealing temperature. Hence, it had low stability. So far, these characteristics are known as practical limitations[108,144] of yttrium oxide thin film for insulating layer of TFEL devices.

2.4.1.2 Barium Strontium Titanate(BST)

Ferroelectric materials have been investigated for various microelectronic applications due to their exceptional high dielectric constant, tunability and other feature. For example, $Ba_xSr_{1-x}TiO_3$(BST, or BSTO) thin films have been applied mainly for microwave, DRAMs and capacitor applications.[132] $Ba_xSr_{1-x}TiO_3$ are a solid solution with ABO_3-formula perovskite-type oxides, where A is a divalent(A^{2+}) metal and B a tetravalent(B^{4+}) element, respectively. In particular, barium titanate ($BaTiO_3$, BT) has been investigated extensively and is one of the most cited representative ferroelectric materials because of its high dielectric constant. Alternatively, strontium titanate ($SrTiO_3$, ST) has good structural stability in ABO_3 formula perovskite-type compounds. Therefore, to take advantage of individual merits of BT and ST, the study of a mixed system of $BaTiO_3$-$SrTiO_3$ has been started[101,105,112,133]. The solid solution (Ba,Sr)TiO_3 is usually based on doping of Sr in BaTiO. At room temperature, $BaTiO_3$ shows tetragonal structure and $SrTiO_3$ cubic structure, respectively as indicated in Table 2-5. After the addition of Sr (> 30 mol %), the BST system did not show tetragonal structure at room temperature. In addition, it is reported that the *Curie temperature*(T_c) decreases linearly with increasing concentration of Sr. [134]

As with other dielectrics, the structural, electrical and optical properties of high-κ ferroelectric thin film largely depend on deposition parameters. BST thin films are deposited by rf sputtering[134,135,136], sol-gel[136], pulsed laser deposition(PLD)[136], spin-on coat[136] and metal-organic CVD(MOCVD)[136, 137]. For the high-κ insulating thin film in capacitor-related applications, the thermodynamic stability feature is of great concern because unwanted silicate, low-κ thin (i.e. a dead layer) layer can be formed when the high-κ dielectric or ferroelectric materials are deposited on Si wafer or other material. The result is a kind of series connection in capacitor circuits with low capacitance and high capacitance:

$$\frac{1}{C_{total}} = \frac{1}{C_{high-\kappa}} + \frac{1}{C_{low-\kappa}}$$

$$C_{total} = \frac{C_{high-\kappa} \cdot C_{low-\kappa}}{C_{high-\kappa} + C_{low-\kappa}} \leq C_{low-\kappa}$$

Equation 2-21

In fact, the capacitance($C_{low-\kappa}$) of the newly grown low-κ thin layer is larger than the total capacitance(C_{total}). Ferroelectric thin films are electrode-sensitive, so electrode selection is very important and limited. Therefore, in order to use the BST thin film as insulating layers in EL devices and other electronic applications, electrically and chemically suitable bottom and top electrodes should be developed because the conventional aluminum electrode might react with oxygen and then a relatively low-κ thin layer(Al_xO_y) can be created at the interface between the electrode and BST thin film. Due to the reaction, the device performance and BST thin film properties would tend to be degraded severely. Currently, platinum(Pt) and palladium(Pd) are applied widely[138,139,140]. These precious metals do not react with oxygen easily, but the Pt electrode still has a problem that needs additional diffusion barrier layers between the substrate and bottom electrodes. Generally, conducting oxides electrodes such as IrO_2, RuO_x, $LaAlO_3$ and $La_xSr_{1-x}CoO_3$ have been used.[136,138,139,140] Basically, the properties of the BST capacitors show strong dependence[139] on the electrode selection, adhesion and the interface between the substrate and electrode. Ivanova, K *et al.*[141] showed that ultra-thin SiON thin film deposited on Si wafer without a Pt layer reduced the inter-diffusion Si atoms and pseudo-binary alloy or silicate formation effectively by sol-gel method. However, the dielectric constant of the BST thin film was approximately ~ 48. The value is quite low compared to the

dielectric constant of BST thin film grown on Pt or Pd metal layer (average 250 and above[136,139]).

The composition of the BST thin films is a critical factor. There are many different compositions of the BST thin film from $x = 0$ to 1. Unfortunately, there is no fixed composition ratio (Ba/Sr) of the BST thin films for universal applications. Among many different compositions, when $x =$ 0.5 or 0.8 the electrical, dielectric and optical properties of the BST thin films show better result - $\varepsilon_r \approx 210 \sim 250$ ($x = 0.75 \sim 0.5$; @ 100 kHz) and $tan\ \delta \approx 0.1$ (average)[142]. As previously mentioned, the increase of Sr addition shows improved stability so that the lower the concentration of Sr is, the leakier the BST thin film is and the increase of Sr leads to the increase of the breakdown field. The dielectric constant of BST thin film reported can be up to 870[121], but the value depends on device structure, electrode, thickness and deposition method. In display devices, particularly in EL devices, ITO transparent conducting oxides are a major dominant electrode. Hence, for this study, ITO electrode is the main interest for BST thin film in EL devices. On the ITO-glass, sputter grown BST thin films showed 238~249[134] of a dielectric constant range. When Si_3N_4 (ε_r=10) is deposited as a buffer layer, the dielectric constant of BST thin films showed approximately a sixth lower value (~ 40)[142].

Inter-diffusion and silicate formation also depends on high annealing temperature. Even though they have the SiON ultra-thin layer, 800 °C post-annealing accelerated the Si atom's interdiffusion effect. Particularly chemical vapour deposition, spin-on coat and sol-gel methods require high substrate and annealing temperature (> 600 °C). Sputtering at low temperature shows significant drawback in limiting the growth of BST grains, which cause lower dielectric constant and higher leakage current. SiO_x and Si_3N_4 double buffer layers suggested one of solutions to produce high-κ BST thin film in sputtering at low temperature. With elevated substrate and annealing temperature, generally both dielectric loss and dielectric constant increases possibly due to interdiffusion effects. At the same time, it shows leakage current increases and the breakdown voltage decreases.

For the response of frequency, dielectric anomalies around 100 kHz are attributed to the increase of electrode resistance due to the electrode oxidation. With dielectric loss, dielectric constant, leakage current and the breakdown voltage, this variation of electrical properties can

be explained by the increase of mobile carrier - oxygen vacancy in BST thin films (O^{2-} in BST → ITO)[143].

Table 2-5. Structural properties of several important perovskite-type materials§[100,101]

Material	Structure at 20 °C				Transition Temperature to cubic phase (°C)
	Symmetry	Lattice parameters			
		a=b	c/a	γ	
$BaTiO_3$	*T*	3.992	1.010		120 (F)
$SrTiO_3$	*C*	3.905	-		-220
$CaTiO_3$	*O*	3.827*	0.999	90° 40'	1260
$PbTiO_3$	*T*	3.905	1.063		490(F)
$PbZrO_3$	*O*	4.159*	0.988	90°	230
$CdTiO_3$	*O*	3.791*	1.004	91°10'	-

Table 2-6. Ionic radii of several A and B ions in ABO_3 family perovskite materials [100,101]

A ion	Radius (Å)	B ion	Radius(Å)
Ba^{2+}	1.34	Ti^{4+}	0.68
Sr^{2+}	1.12	Zr^{4+}	0.79
Pb^{2+}	1.20		
Ca^{2+}	0.99		
Cd^{2+}	0.97		

§ C (cubic); T(Tetragonal); O(Orthorhombic). * They have a multiple unit cell. (F) indicates the phase transition to the cubic phase with the ferroelectric Curie temperature.

2.5 TFEL Phosphors

Phosphors are defined as solid compound materials showing non-thermal electromagnetic radiation. Basically, phosphors for TFEL devices consist of host materials and impurities, which are called activators, or luminous centres. According to Ono, Y.[144,145], six requirements for ACTFEL phosphor matrix materials were reported: ① a wide bandgap, ② ability to withstand high electric fields (~ MV/cm), ③ to act like an insulator below the threshold voltage, ④ able to tolerate annealing temperature (up to 600 °C), ⑤ to deposit the phosphor in thin film form and ⑥ the host material can be doped with an activator. In addition, the luminescent centers should satisfy the following requirements[145]: ① they must be properly incorporated into the host lattice and emit the desired light, ② they should have a large cross section for impact ionization/excitation and ③ the material must be stable when the high electric field applied. II-VI compounds are one candidate group fulfilling these requirements. Most phosphors have localized luminescent centres and contain a far larger variety of ions and the principal localized centres can be classified by their electronic transitions[88]. For example, the activator elements can be transition metal (*d*-block in the period table) and the rare-earth (*f*-block in the period table) elements: (a) transition metal ions: ① $3d^{n10} \Leftrightarrow 3d^9\,4s$, ② $3d^n \Leftrightarrow 3d^n$ and $4d^n \Leftrightarrow 4d^n$ (b) rare-earth and actinide ions: $4f^n \Leftrightarrow 4f^n$ and $5f^n \Leftrightarrow 5f^n$. In particular, the various oxidation states (transition metals mainly; rare earths are normally +3) and ionic radii of these activators are of importance. Thus, there are two mismatches between host materials and luminescent centres: one is size mismatch (eg, ionic radii) and the other is valence mismatch (eg, oxidation state)[146]. Considering ionic radii of rare earth elements, it is difficult to substitute the place of Zn^{2+} ions in size mismatch. Hence, SrS-based phosphor is more suitable for the rare earth due to ionic radii difference. In valence mismatch, phosphors have an additional dopant that act as charge compensators and are called co-activators such as F^- or Cl^-. For example, in ZnS:PrF_3 phosphors, ZnS, Pr and F become host material, activator and co-activators, respectively.

As the requirements, phosphor materials should be wide bandgap ($E_g > 3$ eV) semiconducting materials which are II-VI (II_A-VI_B and II_B-VI_B) or III_B-V_B compounds. One of the reasons for using the wide bandgap semiconductor materials as phosphor materials is to obtain sufficient blue, green and red light emissions. To obtain blue light emission from phosphor materials, the

bandgap of the phosphor should be larger than at least 3 eV because energy of blue light wavelength (400 ~ 470 nm) is around 2.7 ~ 3 eV. Therefore, well-known ZnS(3.6 eV) and SrS(4.3 eV) phosphors satisfy the basic requirement. Currently, ZnS- and SrS-based phosphor materials - ZnS:Mn (yellow), SrS:Ce (greenish blue), SrS:Cu and SrS:Cu,Ag (blue) - have been widely used. Alkaline-earth sulphide-based phosphor materials are sensitive to moisture so it is mandatory to ensure proper encapsulation for reducing reaction between water in air and SrS phosphors[147].

Although the same activators are used, the emitted light colours might be different if host materials are different[145]. Therefore, proper selection of host and activator materials can be critical. In particular, the NaCl-structure phosphor materials form solid solutions so the emission colour can be changed by controlling the host material's composition, activator elements and their concentration[148]. Generally, transition metals, or rare-earth(RE) elements that have partially filled *d*- or *f*-blocks are used as activators. For Cu, Ag and Au, they are also transition metals, but they have full filled *d*- or *f*-shells[149, 150]. To obtain high electroluminescence efficiency, weak bonding, or coupling energy between host materials and activators (or luminous centres) is preferable[147,148]. That means easily impact excited electrons can get involved in luminescence due to weak coupling. Some important ionic radii of activators are summarized in Table 2-7[148]. As phosphor host materials, structure and physical properties of ZnS and SrS materials are given in Table 2-8[88,145] and various luminous centres and their emission colours for EL device are also given in Table 2-9[145,148]. Optical and EL emission properties of major blue emitting EL phosphors including ZnS:Mn phosphor are given in Table 2-10. In Table 2-11, the EL properties of blue phosphor materials and the electronic configurations of Sr, Zn, S, Mn, Cu and Ag elements are presented, respectively.

Table 2-7. Ionic radii of some luminous centers and sulphur[148]

Activators (ground state)	Ionic radii (Å)	Activators (ground state)	Ionic radii (Å)
Cu^{+}	0.73	Ce^{3+}	1.01
Ag^{+}	1.15	Mn^{2+}	0.83
S^{2-}	1.84		

Table 2-8. Structure and physical properties of well-known host materials - ZnS and SrS[88,145]

	SrS	ZnS	
Structure	Cubic, Rocksalt	Cubic,Zincblend	Hexagonal, Wurtzite
Lattice constant (Å) /Ionic radii (Å)	6.02 /1.13 (Sr^{2+})	5.41 /0.74 (Zn^{2+})	a = 3.81; c = 6.26/ -
Energy Bandgap (eV)	4.3 (indirect)	3.6 (direct)	3.8 (direct)
Dielectric Constant	9.4	8.3	8.6
Refractive Index	2.11	2.3	2.36 ~ 2.38
Thermal Expansion Coefficient at RT	14	6.6	5.0
Space Group	Fm3m	F43m	$P6_3mc$
Coordination Number	6	4	4
Meting point (°C)	> 2000	1020*	1700
Wavelength (transmittable) (nm)	390 ~ 14500	270	-

Table 2-9 Selected activators and their colour in phosphor materials[148]

ZnS		SrS		CaS	
Luminous Centre(s)	Colour	Luminous Centre(s)	Colour	Luminous Centre	Colour
Mn	Yellow	(Cu),Ag	Blue	Ce	Green
Pr	White	Sm, Eu	Orange	Eu	Red
Pr, Ce	White	Ce	Blue	Mn	Orange
Dy	Yellowish white	Dy	Yellow	Tb	Yellowish white
Sm	Red	Ho	White		
Tb	Green	Tm	Blue		
Tm	Blue	Tb, Er	Green		

Table 2-10 Optical and EL properties of EL phosphor materials[145]

EL phosphors	L_{40}(cd/m²) at 60 Hz	Efficiency (lm/W)	CIE_x	CIE_y	Emission Colour
ZnS:Mn	**300**	**5**	**0.53**	**0.47**	**Yellow**
SrS:Ce	100	0.8 - 1.6	0.30	0.50	Bluish Green
SrS:Ce,Mn,Ag,Cl	170	1.5	0.26	0.48	Green-blue
SrS:Cu	34	0.24	0.17	0.27	Blue
SrS:Cu,Ga,Ag	35	0.24	0.16	0.21	Blue
SrS:Pb	~ 2	-	0.26	0.33	Blue-green
CaS:Pb	80	-	0.15	0.15	Blue
$SrGa_2S_4$:Ce	5	0.02	0.15	0.10	Blue
$CaGa_2S_4$:Ce	10	0.04	0.15	0.19	Blue
ZnS:Tm, F	0.2	<0.01	0.110.09	0.09	Blue
ZnS/SrS:Ce	96	1.3	0.26	0.47	Blue-green
ZnS/SrS:Ce	14	0.2	0.10	0.26	Blue
SrS:Cu,Ag[151]	9.2	0.25	0.19	0.27	Blue

Table 2-11 Electronic configurations, their ground and excited states of Zn, Sr, S, Mn, Cu and Ag

Atoms/Ion	Electron configuration /Ground state Term/Excited state Term
^{30}Zn	$1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 4s^2\ 3d^{10}$ = [Ar] $4s^2\ 3d^{10}$
^{38}Sr	$1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 4s^2\ 3d^{10}\ 4p^6\ 5s^2$ = [Kr] $5s^2$
^{16}S	$1s^2\ 2s^2$ 2p6 $3s^2\ 3p^4$ = [Ne] $3s^2\ 3p^4$
$^{25}Mn//Mn^{2+}$	[Ar] $4s^2\ 3d^5$//[Ar]$3d^5(^6S\ [^6A_1])$/[Ar] $4s^1\ 3d^4(^4G[^4T_1])$*
$^{29}Cu//Cu^{+}$	[Ar] $3d^{10}\ 4s^1$ //[Ar] $3d^{10}$ ($^1S\ [^1A_{1g}]$) /[Ar] $3d^9\ 5s^1$ ($^3D\ [^3E_g]$)
$^{47}Ag//Ag^{+}$	[Kr] $4d^{10}\ 5s^1$ //[Kr] $4d^{10}$ ($^1S\ [^1A_{1g}]$) /[Kr] $4d^9\ 5s^1$ ($^3D\ [^3E_g]$)

* The subscript g usually drops in the tetrahedral(*Td*) symmetry condition.

2.6 Summary

In this literature review chapter, EL basics for structures and theory, EL-related development background, various other flat panel display technologies, insulating layer - Y_2O_3 and BST - roles and phosphors (ZnS and SrS) have been extensively discussed. This will be good opportunity for expanding the knowledge of EL and flat panel display technologies' materials and devices because a single display device or technology satisfying all the requirements is virtually impossible. Thus, this background and literature review can play a role as an important building block to investigate more promising devices in scientific, technical and social needs. Further investigation will be discussed in later chapters.

REFERENCES

[1] Matsumoto, Shoichi Electronics display devices, Ch. 2, John Wiley & Sons, 1984

[2] Tannas, Lawrence E. Jr (Ed.) Flat-panel Displays and CRTs, Ch. 11 (by Penz, P. Andrew), Van Nostrand Reinhold, New York, 1985

[3] Hornbeck, Larry J. From cathode rays to digital micromirrors: A history of electronic projection display technology, pp. 7 - 46, No. 3 Vol. 15, TI Technical Journal, July-September 1998

[4] Maiser, Eric and Winkler Joerg, European Technology: Flat Panel Displays, 4th ed. DFF/VDMA, 2004

[5] Logystyx UK Ltd. Flat panel displays in the UK - A guide to UK capability, 2005/6 edition, Department of Trade and Industry(dti), UK

[6] Vij, D.R.(Ed.) Luminescence of Solids - Ch. 1 and 3, Plenum Press, New York, 1998

[7] Technology Milestone Chart - Nurturing Progress in Plasma Technology(40 Years of SID Symposia), SID International Symposium, Baltimore, 2003; it is available on http://www.sid.org/archives

[8] Information and news on plasma display panel(PDP) are available on PDP manufactures official websites, respectively: LG(lge.com), Pioneer(pioneerelectronics.com), SamsungSDI(samsungsdi.com) and Sharp(sharp-world.com),

[9] Spindt, C.A. A Thin-Film Field Emission Cathode, Journal of Applied Physics 39 pp. 3504-3505, 1968

[10] Buck, D. A. and Shoulders, K. R. *Proc. Eastern Joint Computer Conf:* (New York: AIEE) pp 55-9, 1959

[11] Technology Milestone Chart - Nurturing Progress in CRT Technology(40 Years of SID Symposia), SID International Symposium, Baltimore, 2003; it is available on http://www.sid.org/archives

[12] Cannon Technology, Surface conduction Electron emitter display(SED) structure and information is available on http://www.canon.com/technology/display

[13] Uh, Hyung soo, Field Emission Display Lecture notes - Display Engineering Course, Seoul Nation University, Korea.

[14] Ju, B. K, FED R&D current situation, Nikkei Electronics Asia, January 2006 - (http://www.neakorea.co.kr) in Korean

[15] Burden, Adrian P. Field Emission Display lecture note (from Emissive Displays), DisplayMasters Program at Nottingham Trent University, UK, 2002

[16] Brennan, Kevin F. *The physics of semiconductors with applications to optoelectronic devices*, pp. 699-700 (from Ch. 13) Cambridge University Press, 1999

[17] Rai-Choudhury, P. (Ed.) *MEMS and MOEMS Technology and Application*, Ch. 1, SPIE, Washington, 2000

[18] Ju, B.K. FEDs: Flat Panel Display Seminar Lecture notes, KATS(www.ats.go.kr), Korea, July 2005

[19] Komoda, T. et al, *Invited Paper:* Fabrication of Ballistic Electron Surface-Emitting Display on Glass Substrate, 188, Vol. 32, SID Symposium Digest, San Francisco, 2001

[20] Pope, M. et al, Journal of Chemistry and Physics, Vol. 42, pp. 2540, 1965

[21] Helfrich, W and Schneider, W. G., Physical Review Letters, Vol. 14, pp. 229, 1965

[22] Tang, C.W and VanSlyke, S.A., Applied Physics Letters, Vol. 51, p.913, 1987; Tang, C.W. et al, Journal of Applied Physics, Vol. 65, p. 3610, 1989

[23] Friend, R.H. et al, *Nature*, p. 121, Vol. 397, 1999

[24] Williams, D. J. Organic LEDs - Get Brighter , Sharper, Photonic Spectra, pp. 116-20, January 2003

[25] Samsung SDI, OLED Overview, Structure and Mechanism on www.samsungsdi.com

[26] Cho, K.(Ed.) *Excitons*, pp. 1-77, Springer, 1979

[27] Knox, Robert S. *Theory of Excitons*, Ch 1, 2 and 4, Academic Press, 1963

[28] Lee, C. H. A mechanism of the organic LED devices(from OLEDs, Special Issue), Korea Information Display, pp. 14-23, 2(2) (in Korean) 2001

[29] Sheats, J. R. et al, Science, p. 884, Vol. 273, 1996

[30] Weiser, Mark Ubiquitous Computing website: www.ubiq.com/hypertext/weiser/weiser.html

[31] Joosse, Koen(ed.) Courting displays to spice up our lives (pp. 4-7), Polymer OLED displays(pp. 10-3), and Low-temperature polysilicon (pp. 14-5), Issue 20, Phillips Research Password, 2004

[32] Ritter, John The Promise of Electronic Ink, pp. 22 ~ 25, No. 12, Vol. 17, Information Display, Dec. 2001

[33] E ink official website: www.eink.com/technology/flexible.html

[34] Comiskey, B. et al., An electrophoretic ink for all-printed reflective electronic displays, pp. 253-55, No. 394, Nature, 1998

[35] Sheridon, N. K et al., Gyricon rotating ball display. Moreale, J. ed. Proceedings of the IEEE 1997 International Display Research Conference; 1997 September 15; Toronto, Canada.

[36] Sheridon, N. K. et al., The gyricon rotating ball display, pp. 141-143, Part 2, Vol. 7, Journal of the SID, 1999

[37] Crawford, Richard A bright new page in portable display, pp. 40-46, Spectrum, October, 2000

[38] Liang, R. C. et al., Microcup® displays: Electronic paper by roll-to-roll manufacturing processes, pp. 621-28, Part 4, Vol. 11, Journal of the SID, 2003

[39] Liang, R. C. et al., Microcup® Active and Passive Matrix Electrophoretic Displays by Roll-toRoll Manufacturing Processes, 20.1(pp. 838-841), SID Technical Digest, 2003

[40] SiPix Imaging Incorporation's official website: www.sipix.com

[41] Hayes, Robert A. and Feenstra, B.J. Video-speed electronic paper based on electrowetting, Vol. 425,

Nature, 2003

[42] Liquavista, Electroweeting Display Technology Backgrounder which is available on http://www.research.philips.com/technologies/display/electrowetdisp/index.html

[43] Heikenfeld, J. C. and Steckl, A. J. Liquid Light, pp. 26-31, No. 11, Vol. 20, Information Display, November, 2004

[44] Gelinck, G. et al., Making Rollable Displays, pp. 12-5, No. 11 Vol. 20, Information Display, 2004

[45] Gelinck, G. H. et al., A rollable, organic electrophoretic QVGA display with field-shielded pixel architecture, pp. 113-18, Part 2 Vol. 14, Journal of the SID, 2006

[46] Burns S.E. et al., A scalable manufacturing process for flexible active-matrix e-paper displays, J. SID, July 2005

[47] Rutherford, Nicole Flexible substrates and packaging for organic displays and electronics, pp. 20-5, No. 11 Vol. 21, Information Display, 2005

[48] Gehring, Frits C. et al., A slim CRT to compete with flat panes, pp. 22-25, No. 3&4, Vol. 20, Information Display, 2004

[49] Younse, Jack M. Mirrors on a chip, pp. 27-31, IEEE Spectrum, November 1993

[50] Yoder, Lars The digital display technology of the future, pp. 1-11, INFOCOMM, June 1997

[51] Fan-Chiang, K.-H. et al., fringing-Field Effects on High-Resolution Liquid Crystal Microdisplays, pp. 304-13, No. 2 Vol. 1, Journal of Display Technology, IEEE, 2005

[52] Gove, Robert J. DMD Display Systems: The impact of an All-Digital Display, SID International Symposium, 1994; The updated version of the same title is available at www.dlp.com/whitepapers

[53] Hsu, Rong and Liu, P-Y., New Challenges in LCoS Technologies (invited paper), pp. 106-7, IEEE, 2004

[54] Hornbeck, L.J. Deformable-Mirror Spatial Light Modulators, pp.86-102, Vol.1150, Spatial Light Modulators and Application III, SPIE Critical Reviews, 1989

[55] DLP/DMD technology official website; www.dlp.com

[56] Hornbeck, Larry J. Current Status and Future Applications for DMD-based Projection Displays, pp. 139-142, International Display Workshop(IDW), 1998

[57] Migl, Travis W. Interfacing to the digital micromirror device for home entertainment applications, pp. 1-8, Proceedings of IPACK: The Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition, Hawaii, 2001

[58] Bloom, David The Grating Light Valve: Revolutionizing Display Technology, Vol. 3013, Projection Diplays III Symposium, SPIE Proceedings, 1997

[59] Silicon Light Machines website: www.siliconlight.com

[60] Corbin, D. et al., Grating Light Valve and Vehicle Displays at www.siliconlight.com

[61] Bae, B. S. Microdisplays: High Temperature Polycrystalline Silicon(HTPS) TFT LCD, pp. 10-17, No. 5, Vol. 3 Information Display(in Korean), October 2002

[62] Allen, Kimberly "Microdisplay - Emerging Display Technologies-2003", Stanford Resources display insight report, November 2002

[63] Cranton, W. M et al., EL on the Edge, pp. 22-25, No. 4&5, Vol. 18, Information Display, 2002

[64] Atwood, Stephen P. Microdisplay at SID 2002: Causion Optimism, pp. 30-34, No. 9 Vol. 18, Information Display, September 2002

[65] Inoguchi T. *et al.* Digest of 1974 SID International Symposium, 84, 1974

[66] Destriau, G. Recherches sur les scintillations des sulfures de zinc aux rayons (*in English*, Study on scintilation of zinc sulphide by light), pp. 587-625, Vol. 33, J. Chim. Physique, 1936

[67] Destriau, G. Recherches Expérimentalses sur les actions du champ Électrique sur les Sulfures Phosphorescentsi(*in English*, Experimental research on the sulphur phosphorescent by the application of electric field), pp. 117-124, Vol. 34, J. Chim. Phys. 1937 (in French)

[68] Kitai, A. H. *Solid State Luminescence Theory, Materials and Devices*, Ch 5, 1993 Chapman and Hall

[69] Billmeyer and Saltzman, *Principles of Color Technology*, 3rd Ed. Ch 1, 2000 John Wiley and Sons,

[70] Mauch R. H. and Gumlich, H.-E.,(Eds.) *Inorganic and Organic Electroluminescence*: "Colour by White EL Displays" by Törnqvist, R., pp. 279-284, 1996, Berlin, Wissenschaft & Technik Verlag

[71] Tanaka, s. et al., pp.293- , SID 88 Digest, 1988

[72] King. C.N. Electroluminescence: an industry perspective, pp. 153-156, Vol. 4, J. SID, 1996

[73] Leskelä, M. et al., Electroluminescent calcium sulphide thin films doped with Tb^{+3} and Eu^{+2}, pp. 113-115, Vol. 3, Chemtrontics, 1998

[74] Barthou, C. et al., Ce^{3+} luminescent centers in ALE SrS TFEL devices, pp. 211-214, Extended Abstracts, The 9th International Workshop on Inorganic and Organic Electroluminescence, Oregon, 1998

[75] Sun, S. C. and Chen, T.F. Effects of electrode materials and annealing ambient on the electrical properties of TiO^2 thin films by metalorganic chemical vapor deposition, pp. 1346-1350, Vol. 36, Jpn. J. Appl. Phys. 1997

[76] Moehnke, S. et al., Improved white TFEL phosphors using SrS:Cu, pp. 203-206, Extended Abstracts, The 9th International Workshop on Inorganic and Organic Electroluminescence, Oregon, 1998

[77] Ohmi, K. et al., Blue-emitting SrS:Cu TFEL Devices prepared by hot-well deposition technique, pp. 219-222, Extended Abstracts, The 9th International Workshop on Inorganic and Organic Electroluminescence, Oregon, 1998

[78] Sun, S.-S. Blue emitting SrS:Ag, Cu TFEL devices, pp. 183-186, Extended Abstracts, The 9th International Workshop on Inorganic and Organic Electroluminescence, Oregon, 1998

[79] Park, W. et al., Luminescence properties of SrS:Cu,Ag TFEL phosphors, pp. 215-218, Extended Abstracts, The 9th International Workshop on Inorganic and Organic Electroluminescence, Oregon, 1998

[80] Velthaus, K.-O. et al., Low-temperature deposition for SrS:Cu,Ag EL phosphors(Late-new papar), pp.231-234, Extended Abstracts, The 9th International Workshop on Inorganic and Organic Electroluminescence, Oregon, 1998

[81] Heikenfeld, J. and Steckl, A.J. High contrast Thick Dielectric GaN Electroluminescent displays on glass substrates, 9.1, SID 02 Digest, 2002

[82] Xin, Yongbao, et al., Multi-Source Depostion of $BaAl_2S_4$:Eu Blue Phossphors, 36.2, SID 04 Digest, 2004

[83] Wasa, K. and Hayakawa, S. *Handbook of sputtering deposition technology*, 1992

[84] Stuart, R. V. *Vacuum Technology, thin films and sputtering*, Academic Press, 1983

[85] Seshan, Krishna (Ed.) *Handbook of thin-film deposition processes and techniques – principles, methods, equipments and application*, Ch 1 & 8, Noyes 2002

[86] Ohring, Milton *The materials science of thin films*, Academic Press 1992

[87] Atomic layer epitaxy/deposition -S.M. George, A.W. Ott, J.W. Klaus, J. Phys. Chem. 100 (1996) 13121.

[88] Shionoya, Shigeo and Yen William M, *Phosphor Handbook* Ch 3 - Sec 6 and 7, CRC Press 1999

[89] Hitt, J.C. et al., Thin-film Electroluminescent Device Physics Modeling, pp. 29-85, No. 1, Vol. 25, Critical Reviews in Solid State Materials Sciences, 2000

[90] Brennan, K. F. *The Physics of Semiconductors with applications to optoelectronic devices*, pp 701-3, 1999, Cambridge University Press

[91] Cranton, W, M. et al., Miniature transverse TFEL Devices (Invited paper),, I-20.4, Proceedings of IDMC, Seoul, 2002 (reference therein)

[92] Rack, Philips D. and Holloway, Pual H., The structure, device physics and material properties of thin film electroluminescent displays, Materials Science and Engineering, R21, p. 171, 1998

[93] The International Technology Roadmap for Semiconductors(ITRS) 2003 Edition – Process Integration, Devices and Structures (PIDS) and Emerging Research Devices sections; Critical Reliability Challenges for The International Technology Roadmap for Semiconductors (ITRS) – International SEMATECH Technology Transfer #03024377A-TR

[94] Agilent Tecchnologies, *Agilent Technologies Impedance Measurement Handbook*, DEC. 2003

[95] Bartnikas, R. (Ed.) *Electrical Properties of Solid Insulating Materials: Measurement Techniques* (Engineering Dielectrics Volume IIB), Ch. 2, American Society for Testing and Materials(ASTM), 1987

[96] Ksasap, S. O., *Principles of Electrical Engineering Materials and Devices*, Chap. 7, 1997, Boston, Irwin McGraw-Hill

[97] Von Hippel, Arthur R. (Ed.) *Dielectric Materials and Applications*, Ch 1 Theory, MIT 1954

[98] Cheng, David K. *Field and Wave Electromagnetics 2nd Ed.*, Section 3-8, Addison-Wesley, 1989

[99] Harrop, P. J. *Dielectrics*, pp. 1-80, 1972, London, Butterworths

[100] Jona, Franco and Shirane, G., *Ferroelectric Crystals*, Ch 1, 4 and 5, Dover 1993 (Orignally published in 1962 by Pergamon Press)

[101] Nalwa, Hari Singh *Handbook of Advanced Electronic and Photonic Materials and Devices – Vol. 4 Ferroelectrics and Dielectrics* (Pyroelectricity: Fundamentals and Applications by Lang, S. B. and Das-Gupta, D. K.), Academic Press, 2001 (references therein)

[102] Strukov, B.A. and Levanyuk, A.P., *Ferroelectric Phenomena in Crystals – Physical Foundations*, Ch.1, Springer 1998

[103] Hecht, Eugene, *Optics*, 2nd Edition, Ch 4, 1987, Addison-Wesley

[104] Wilk, G. D. et al, High-κ gate dielectrics: Current status and materials properties considerations, Journal of Applied Physics, 89(10), 5243, 2001

[105] Yoon, D-S. et al., Future direction for a diffusion barrier in future high density volatile and nonvolatile memory devices, pp. 143-226, No. 3 &4, Vol. 27, Critical reviews in Solid State and Materials Science, 2002

[106] Suehle, J. S. et al, Challenges of High-κ Gate Dielectrics for Future MOS Devices, American Vacuum Society, Plasma Process-Induced Damage International Symposium, 90, 2001

[107] Cranton, W. M, et al. Growth and dielectric characterization of yttrium oxide thin films deposited on Si by rf-magnetron sputtering, Thin Solid Films, 226, 156-160, 1993

[108] Krasnov, Alex N. Selection of dielectrics for alternating-current thin film electroluminescent device, pp. 1-13, Vol. 347, Thin Solid Films, 1999

[109] Fukumoto, H. et al. Heteroepitaxial growth of Y_2O_3 films on silicon, Applied Physics Letters, 55(4), 360, 1989

[110] Araiza, J. J. et al. Structural, optical and electrical characteristics of yttrium oxide films deposited by laser ablation, Journal of Vacuum Science and Technology A 16(6), 3305, 1998

[111] Rozhkov, V. A. et al. Electrical and Photoelectrical Properties of MIS structures with Rare Earth Oxide Films as Insulator, IEEE 5th International Conference on Conduction and Breakdown in Solid Dielectrics, 552, 1995

[112] Nalwa, Hari Singh(Ed.) Handbook of Thin Film Materials – Vol. 3 Ferroelectrics and Dielectric Thin Films (The electrical properties of high-dielectric-constant and ferroelectric thin films for very large scale integration circuits by Lee, J. Y-M, and Lai, B. C.), Academic Press, 2002 (references therein)

[113] Onisawa, Ken-ichi, et al. Dielectric properties of rf-sputtered Y_2O_3 thin films, Journal of Applied Physics, vol. 68(2), p. 719, 1990

[114] Manchanda, L. and Gurvitch, M., Yttrium Oxide/Silicon Dioxide: A New Dielectric Structure for VLSI/ULSI Circuits, pp. 180-182, No. 4, Vol. 9, IEEE Electron Device Letters, 1988

[115] Diniz, J. A. et al., High quality of ultra-thin silicon oxynitride films formed by low-energy nitrogen implantation into silicon with additional plasma or thermal oxidation, pp. 64-69, No. 166-167, Nuclear Instruments and Methods in Physics Research B, 2000

[116] Kolodzey, James et al. Electrical Conduction and Dielectric Breakdown in Aluminum Oxide Insulators on Silicon, IEEE Transaction on Electron Device 47(1), 121, 2000

[117] Chin, A. et al, Device and Reliability of High-κ Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it}, Technical Digest VLSI Technology Symposium, 135, 1999

[118] Lee, Myung Jae, et al, Effects of Post-annealing on Current-Voltage Characteristics of Metal-Insulator (Ta_2O_5)-Metal Type Thin-Film Diodes, J. KPS 39(4), 685-691, 2001

[119] Serikawa, T. and Okamoto, A. Properties of Magnetron-Sputtered Silicon Nitride Films, Journal of Electrochemistry Society: Solid-State Science and Technology, 2928, 1984

[120] Miyasaka, Yoichi and Matsubara, Shogo, Dielectric Properties of Sputter-Deposited $BaTiO_3$-$SrTiO_3$ Thin Films, IEEE, 121-124, 1998

[121] Manchanda, L. et al, High-κ Gate Dielectrics for the Silicon Industry, IEEE IWGI, 56, 2001

[122] Tsao, Bang-Hung, *et al.* Sputtered Barium Titanate and Barium Strontium Titanate Films for Capacitor Applications, 12th IEEE International Symposium on Application of Ferroelectrics(ISAF), vol 2. pp. 837-840, 2000

[123] Kotecki, David E, A review of high dielectric materials for DRAM capacitors, Integrated Ferroelectrics, vol. 16, pp. 1-19, 1997 (reference therein)

[124] Lee, Y.-H. et al, Comprehensive understandings on the high dielectric constant insulating layers for alternating-current thin film electroluminescent devices, IEEE Transactions on Electron Devices, 48(4), pp. 653 - 660, 2001

[125] Kingery, W. D. Introduction to Ceramics, Ch. 20, 1960, John Wiley and Sons

[126] Hudner, Jan. et al. Growth and characterization of yttrium oxide thin layers on silicon deposited by yttrium evaporation in atomic oxygen, Vacuum, 46(8-10), 967-970, 1995

[127] Horng, R. H. et al. Effects of rapid thermal process on structural and electrical characteristics of Y_2O_3 thin films by rf magnetron sputtering, Thin Solid Films, 289, 234-237, 1996

[128] Basak, D. and Sen, S. K. Electrical, dielectric and optical properties of M/Y_2O_3/M devices, Thin Solid Films, 254, (181-186), 1995

[129] Kalkur, T. S. et al. Yttrium Oxide Based Metal-Insulator-Semiconductor Structure on Silicon, Thin Solid Films, 170, 185-189, 1989

[130] Hunter, M. E. et al. Epitaxial Y_2O_3 films grown on Si (111) by pulsed-laser ablation, Applied Physics Letters, 76(14), 1935, 2000

[131] Jones, S. L. et al, Luminescence of pulsed laser deposited Eu doped yttrium oxide films, Applied Physics Letters, 71(3), 1997

[132] Samantaray, C.B. et al., Effect of post-deposition annealing on microstructural and optical properties of barium strontium titanate thin films deposited by r.f. magnetron sputtering, pp. 365-370, Vol. 12, Journal of Materials Science: Materials in Electronics, 2001 (references therein)

[133] Kingon A. I. et al., Alternative dielectrics to silicon dioxide for memory and logic devices, pp. 1032-38, Vol. 406, Nature, August 2000

[134] Kim, T.S., et al., Electrical properties of radio frequency magnetron-sputtered (BaSr)TiO_3 thin films on indium tin oxide-coated glass substrate, pp. 529-532, No. 2, Vol. 12, Journal of Vacuum Science and Technology, 1994

[135] Cramer, N.,et al., Leakage Current and Dielectric Properties of $Ba_{0.5}Sr_{0.5}TiO_3$ films deposited by RF sputtering at low substrate temperature, G.3.6.1, Vol. 768, Material Research Society Symposium Proceeding, 2003

[136] Nalwa, Hari Singh(Ed.) *Handbook of Thin Film Materials – Vol. 3 Ferroelectrics and Dielectric Thin Films*: Ch 2. High permittivity (Ba,Sr)TiO_3 Thin Films by Nayak, M. et al., Academic Press, 2002 (references therein)

[137] Koutsaroff, I.P. et al., Dielectric Properties of (Ba,Sr)TiO_3 Thin Film capacitors fabricated on Alumina substrates, U6.1.1, Vo. 748, Material Research Society Symposium Proceedings, 2003

[138] Ramesh R.(Ed.) *Thin Film Ferroelectric Materials and Devices*, Kluwer, 1977

[139] Araujo, C. Paz de, et al (Eds.), *Ferroelectric thin films: Synthesis and Basic Properties*, Gordon and Breach Science, 1996

[140] Araujo, C. Paz de, et al (Eds.)., *Science and Technology of Integrated Ferroelectrics*: Selected Papers from Eleven Years of the Proceedings of the International Symposium on Integrated Ferroelectrics, Gordon and Breach, 2000

[141] Ivanova, K. Et al., Application of impedance spectroscopy for the investigation of MIS structures with barium strontium titanate, pp.803-804, Vol. 14, Journal of Materials Science: Materials in Electronics, 2003

[142] Kim. T.S. *PhD thesis* (in Korean with English abstract), KAIST, Taejun, Korea (reference therein)

[143] Becker, Robert Jurgen, PhD thesis, Stanford University, US 2002

[144] Ono, A. *Electroluminescent Displays*, World Scientific Publishing Co., Singapore, 1995

[145] Mueller, Gerd *Electroluminescence II* (from Semiconductors and Semimetals, Vol. 65 by Willardson, R.K. and Weber, Eicke R.(Eds.)), Academic Press, 2000

[146] Nam, T. ***Master's thesis*** (in Korean with English abstract), KyungHee University, 1996, Seoul, Korea. (references therein)

[147] KIST/MOST, *Development of White-Light Emitting EL Display Devices* (in Korean), 1993, Seoul, Korea (references therein)

[148] Lee, Y. -H. ***Ph.D. Thesis***, Department of Physics, Korea University, Seoul, Korea (in Korean, but English Abstract), 1994

[149] Cotton, F.A., et al. *Basic Inorganic Chemistry 3rd Ed.*, Ch 4 and 23, 1995, John Wiley and Sons

[150] Shriver, D.F. and Atkins, P.W., *Inorganic Chemistry 3rd Ed.*, Ch 1,4,7,and 13, 1999, Oxford University Press

[151] Sun, S.-S., et al, Proceedings of 17th IDRC, Toronto, Canada, p. 201, 1997

Chapter 3 Experimental Methodology

Overview

This chapter describes thin film deposition technology and preparation, a pulsed laser annealing (PLA) system and process, the TFEL device fabrication processes, and various characterisation methods for thin films and a full device applied in this research. An rf-magnetron sputtering and an evaporation technique are used for preparation of thin films and the devices. The thin films and devices were analysed structurally, electrically and optically. The characterizations are carried out by using *C-V*, *I-V*, interferometric and spectral reflectance techniques, photo- and electro-luminescence (PL and EL), transient measurements and scanning electron microscopy (SEM) and X-ray diffraction(XRD) techniques.

3.1. Thin film Deposition Technology

For thin film deposition, there are usually two distinct methods used, divided by techniques and physics into: Physical Vapor Deposition (PVD), and Chemical Vapor Deposition(CVD). In the physical vapor deposition technique, its method is used to produce constituent particles and then deposit them on the substrates by physical mechanisms which include ①heating/melting a solid source until it can be vaporized - ***evaporation*** or ② energetic atomic particle bombardment with the surface of the solid target(source) in plasma environment - ***sputtering*** - after a physical collision-cascade process, constituent particles are removed, or ejected from the solid target and can be deposited onto the surface of a substrate. Generally, plasma means partially ionized gaseous phase by a glow discharge and is neutral electrically. The sputtering simply depends on the momentum (i.e., kinetic energy because of negligible atomic mass) transfer of atomic particles when the incident atomic particles impact the surface atoms on the substrate. While in CVD, in order to grow thin films on the substrate, volatile compounds of the materials to be formed are thermally decomposed and chemical reactions - such as pyrolysis* (thermally decomposition), reduction, oxidation, compound formation, and disproportionation (nonvolatile metal → volatile compounds) - with other reactant gases,

* Often chemical decomposition by high temperature

vapors or liquids take place in the deposition chamber at the substrate. After the chemical processes, non-volatile products can be grown on the substrate. Many CVD processes operate at high temperature (around 1000 °C)[1,2,3,4,5,6].

Though the basics of thin film deposition technologies are mentioned above, a full discussion of thin film preparation techniques is out of the scope of this experimental chapter, but the basic background of thin film deposition processes will be discussed. Further detail can be acquired through the given references.

With these basic concepts mentioned above, there are several variants in each thin film deposition process. In evaporation, thermal evaporation and electron beam evaporation have been used. Recently, pulsed laser deposition (PLD) has been developed and modified as a laser-assisted evaporation method of physical vapor deposition. Ion plating and Ion cluster beam deposition (ICBM) are categorized as hybrid and modified evaporation techniques[2]. For sputtering, direct current (DC-), radio-frequency (RF-), magnetron, reactive and rf-magnetron sputtering techniques have been utilised commonly with the terminology relating to the applied signal between target and substrate, sputtering gases used or the introduction of magnet on the target, respectively.

As the simplest form, the DC (bias) sputtering is known as diode or cathodic sputtering. A target material is often called the cathode and typically several kilovolts are applied to the target. The substrate is normally facing to the target and grounded, so potentially it can act as the anode. Generally, the mean-free path of electrons between collisions is large and after being collected by the anode, they can not be replaced by secondary ionization process. Therefore, ionization efficiencies, sputtering yield and deposition rate are low[2].

Unlike DC sputtering, rf sputtering was developed to grow insulator thin films directly by taking advantage of immobile ions in the high frequency regime. In other words, the rf-sputtering method allows insulators to be deposited without charge buildup on the target. Generally, over 50kHz, ion particles become relatively immobile compared to electrons due to their atomic mass difference. In addition, the electrons' excess oscillation can maintain a

discharge effectively by their ionization process. Therefore, rf sputtering can in principle open a door to deposit any material regardless of its conductivity.

The most important feature in reactive sputtering is that instead of inert gas like Ar, oxygen or nitrogen is introduced as the reactive gas to the chamber so that oxides or nitrides compounds can be deposited. This reactive sputtering is available in either DC or RF/RF-magnetron.

In magnetron sputtering, the introduction of a magnet or magnetic field can make use of the electrons and trap them near the target for increasing ionization probability. In a DC glow discharge (eg, DC sputtering), the electron loss takes place due to their recombination at the wall[1,2].

RF-magnetron sputtering means simply a magnetically assisted rf-sputtering method as a modification between the two different categories to utilise advantages in rf and magnetron sputtering more effectively. In general, sputtering has the following advantages: multi-component films can be deposited, good film adhesion can be realized, low-temperature deposition is possible, better reproducibility of thin films, relative simplicity in control of thin film thickness[1,2,6].

In the field of Chemical Vapour Deposition, Atmospheric Pressure (APCVD), Low Pressure (LPCVD), Plasma enhanced (PECVD), High Density Plasma (HDPCVD), or Metal Organic (MOCVD) chemical vapor deposition techniques are typical variants. They have been proposed and commercially used in various semiconductor device fabrication industries. Often, the CVD processes allow the growth of a reliable high degree of purity and good quality of thin films, with accurate stoichiometric composition and doping levels. In addition, it is not necessary to use high vacuum equipment. At the higher deposition temperatures, the process can improve defect-free crystals or thin films. However, the disadvantages in CVD are undesirable additional reactions at higher temperature, safety due to toxic materials and by-products, more complex apparatus and many variables to be controlled[1,2].

Finally, the Molecular Beam Epitaxy (MBE) method is one of the state-of-the-art and reliable deposition processing techniques in atomic layer epitaxy (ALE) or atomic layer deposition

(ALD). It can be treated as a part of *evaporation* in principle. It generally needs highly controlled evaporation in an ultra high vacuum (~ 10^{-10} Torr) system and other supporting *in-situ* analytical systems to monitor deposition process. A summary of the general thin film deposition technology discussed is summarised in Figure 3-1.

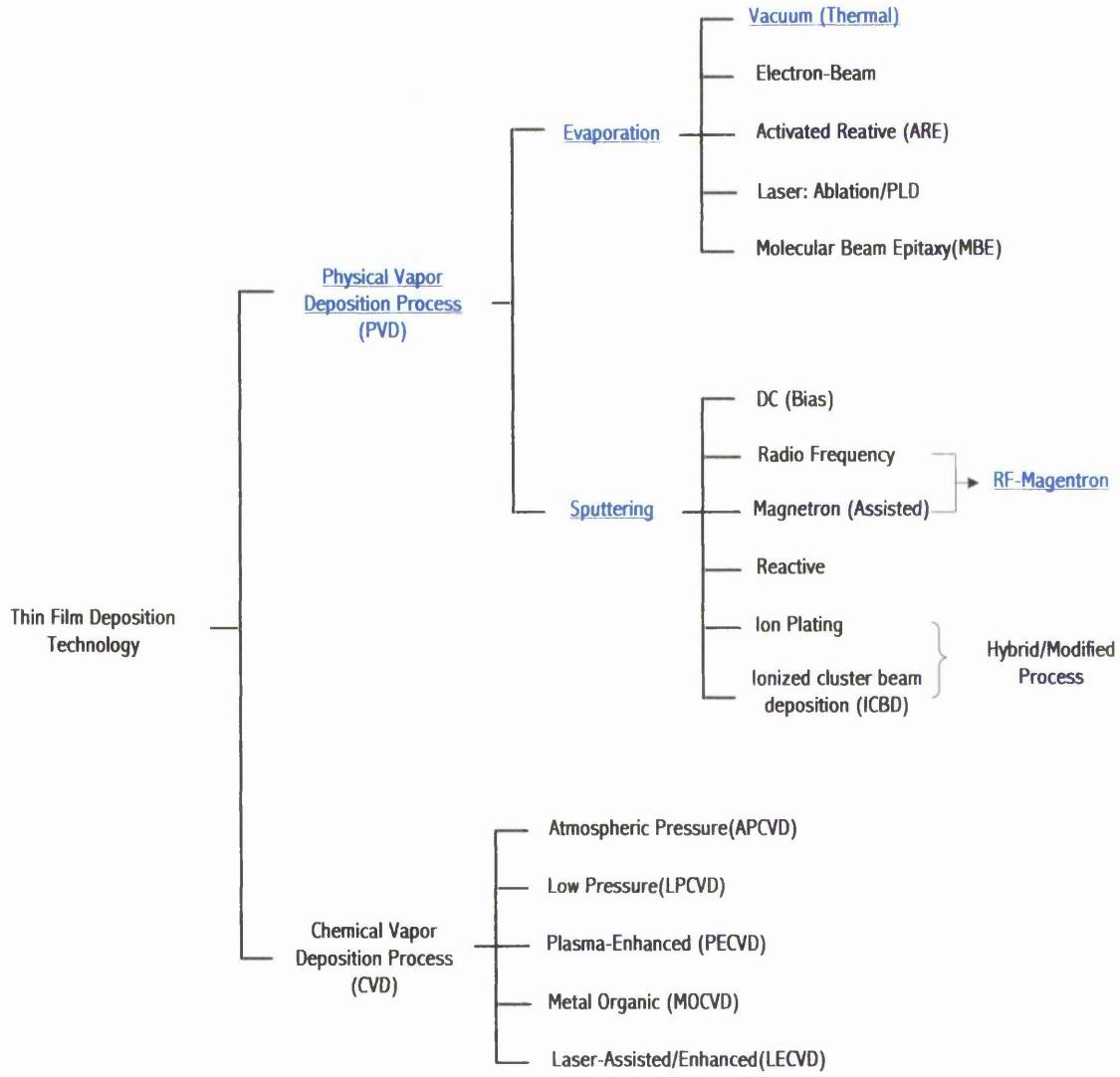


Figure 3-1 Thin film Deposition Technology[1,2]
(The processes employed in this research are highlighted.)

Each individual deposition process, either PVD or CVD, has its own intrinsic strong and weak points. The preference of technique depends on the property requirements of thin film to be grown, and feasibility of the process in regard to cost, uniformity and other factors[7]. For the thin film electroluminescent display (TFEL) device applications investigated here, rf magnetron sputtering technique is preferred for deposition of the various thin films of the display devices. Therefore, transparent conducting oxide, insulating and phosphor thin films are prepared by three separate rf magnetron sputtering systems and a thermal evaporator as a metal coater for Al electrodes was utilised for this research. The general schematic diagram and picture of the sputter systems and the evaporator are illustrated in the following subsections.

3.2. Preparation of thin films

In order to grow thin film layers, 100 mm diameter custom-made glasses, HOYA quartz wafers(4W55, Japan) and n-type silicon wafers (Virginia Semiconductor Inc. USA) with (100) orientation were used as substrates.

In the case of sputtering deposition, there are several important processing parameters to be controlled and monitored: a main chamber base pressure before sputtering, sputtering gas mixture, a working/plasma pressure, a substrate temperature, a rf-power/density and thickness (i.e., deposition period). Each thin film layer was deposited by the rf-magnetron sputtering technique. The basic schematic diagram of the rf magnetron sputter deposition systems used for ITO, phosphor and insulator is provided in Figure 3-2. Al electrode as a back-end process was deposited by thermal evaporation. The block diagram of the thermal evaporator used for the Al electrode is shown in Figure 3-3.

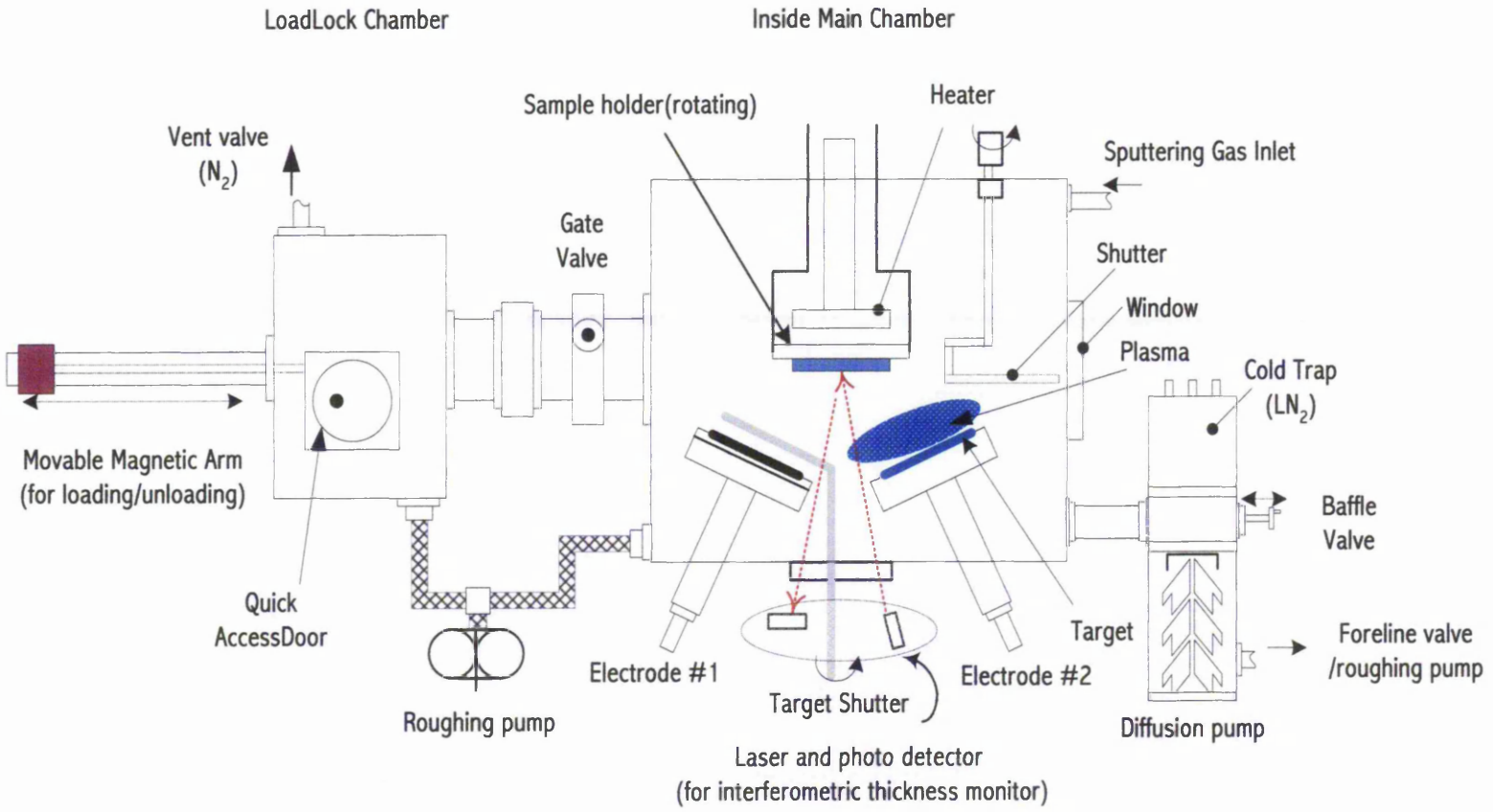


Figure 3-2 A schematic diagram of rf magnetron sputtering system used for ITO, phosphors, and dielectric materials

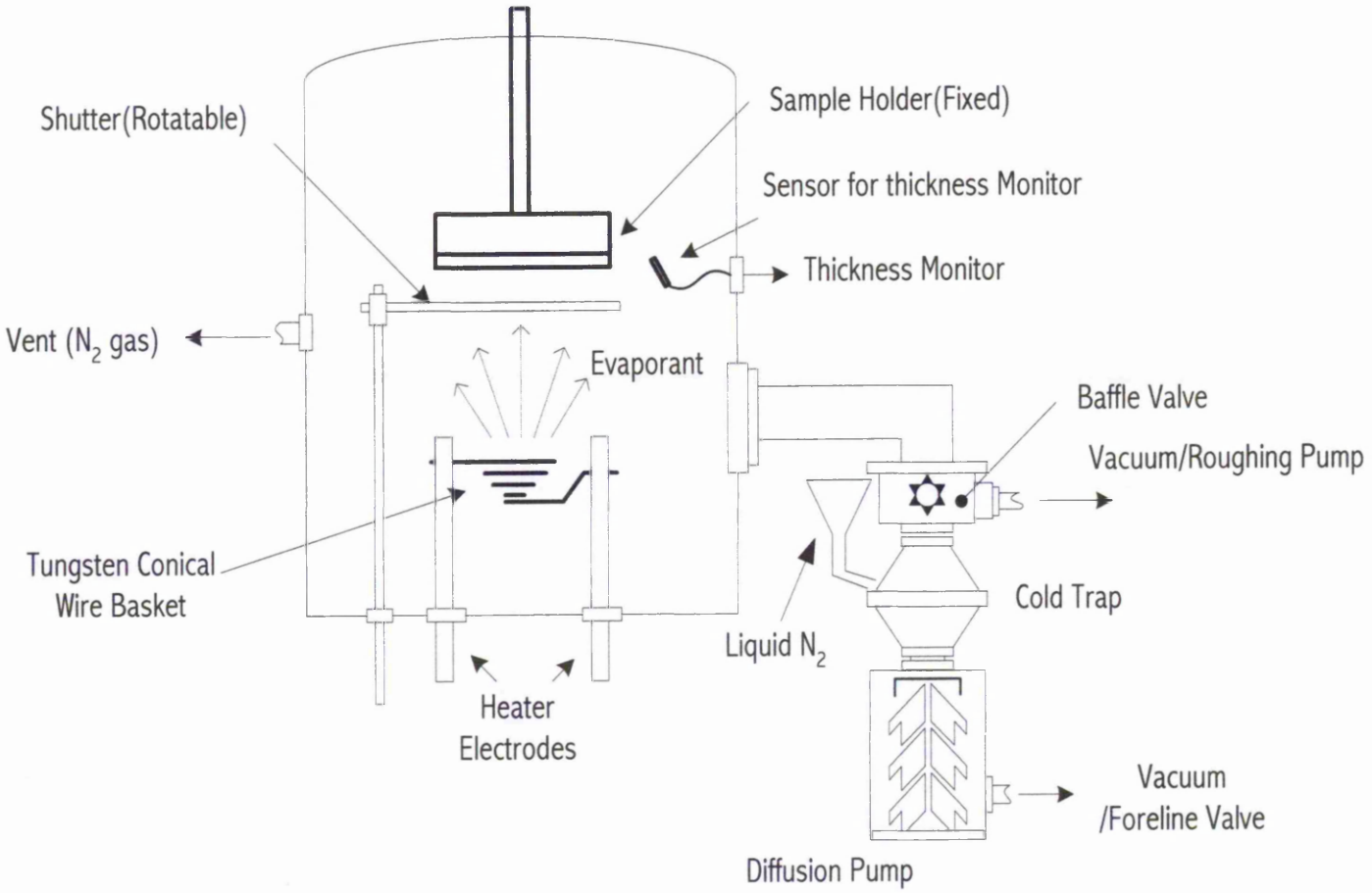


Figure 3-3 Thermal evaporator system for Al electrode deposition

The base chamber pressure is maintained commonly at normally < 1.85 x 10^{-7} Torr for the insulating, phosphor, and ITO layers. During the deposition, the sample holder in the chambers was rotated with a speed of 18 rpm for improving uniformity in temperature and growth. Before starting deposition, a 20~30 min warm-up time to reach the target temperature was provided. 100 W of rf-power was typically applied commonly for phosphor and ITO deposition.

During phosphor (ZnS:Mn, or SrS:Cu,Ag) and Y_2O_3 insulating layer deposition, inert argon(Ar) gas as sputtering gas was supplied to the main chamber via a mass flow controller(MFC) to control the partial pressure. The working pressure was fixed at 3 mTorr which was a previously optimized growth condition by the NTU optoelectronics and displays research group for alternating current thin film electroluminescent display (ACTFEL) device applications. The substrate temperature was maintained at 190 °C (glass substrate) or 200 °C (Si wafer) by using a built-in heater in the main chamber for Y_2O_3 insulating layer, and ZnS:Mn and SrS:Cu,Ag phosphor layers were grown at 200 °C, respectively. ZnS-based and SrS-based phosphor layers were 850 nm and 500 nm thick, respectively. For Y_2O_3, 300 nm-thick layers are applied throughout this study.

For ITO layer deposition, mixed gases of argon and oxygen are supplied. A 1~ 2% oxygen ratio was established by this research for optimum growth of ITO. When the ITO layer was growing, a working pressure of 5 mTorr was maintained and at a substrate temperature of 280 °C the ITO thin film deposition was carried out. The deposited Indium-tin-oxide (ITO, In_2O_3:Sn), as a bottom transparent conducting oxide layer, for metal-insulator-metal(MIM) structure capacitors and full EL devices, was shown to have good electrical properties with a sheet resistance of 3.8 Ω/□ and a transmittance of 93% under the visible light (400 ~ 750 nm) spectrum. The thickness of ITO layer was 1000 nm.

ABO_3 (A=Ca, Ba or/and Sr; B=Ti)-type ferroelectrics are called perovskite materials. BST materials are a solid solution and they are well known as high-κ (i.e., high dielectric constant) materials. In the case of BST deposition for this project, thin film deposition was carried out under various deposition parameters as one of the major research subjects in order to study

optimum deposition conditions for EL device applications. The base pressure of the chamber was less than 1 x 10^{-7} mbar (due to the limit of the system's penning gauge) and plasma pressure for deposition changed from 3 to 40 mTorr. Argon(Ar) and Oxygen(O_2) mixture gases were provided as sputtering gases and their quantities controlled by the mass flow controllers(MFCs) and a needle valve. Oxygen ratio of mixed sputtering gases was controlled from 10% to 40%. The substrate temperature (T_{sub}) of BST thin film deposition has the range of room temperature (RT) ~ 600 °C. RF power had several different conditions; 80, 100, 150 and 200W. Finally, BST thin films had thickness of average 80 ~ 350 nm. In this study, BST thin film grown by rf magnetron sputter were investigated as a function of substrate temperature, thermal/laser annealing, thickness, and other deposition parameters. The optimum conditions with the results of BST deposition will be discussed in Chapter 6.

By the thermal evaporation method, the upper Al electrodes were grown on dielectric layers for MIS/MIM structure capacitors. Al wire (around 20 cm) with purity of 99.99% was cleaned by acetone to remove contaminants on the surface and then folded to make it small for a tungsten conical wire basket. Normally, the base pressure of the evaporator was maintained around < 2.0 x 10^{-6} mbar (1.8 x 10^{-6} Torr). Evaporation was carried out at room temperature and in order to evaporate Al wire, a current source was applied to the tungsten wire basket, slowly increased up to 40 A. After overshooting suddenly, the Al wire started to be evaporated. Maintaining current of 40 A to evaporate Al material fully for a few minutes. Al was evaporated onto the substrate through a shadow mask. There were three different diameters of holes on the contact mask for electrodes with diameter 0.5, 1.0, and 2.0mm. Circular Al electrodes were used for *C-V*, *I-V* and surface light emission measurement and deposited through the metal contact mask. For lateral emission TFEL (LETFEL) devices, line-shaped (eg., interdigit form) Al electrodes were used to fabricate test EL devices. The deposition rate and thickness of the Al electrode was monitored by a built-in Caburn STM-100 system. The measured thickness of the top Al electrode was of 5000 (± 500) Å normally. For *C-V*, *I-V*, and lateral emission experiments, around 300 nm thick Al was deposited on the back of silicon wafer to improve back contact.

The barrier layers were deposited in between phosphor layers in order to increase brightness of EL light emission. Each quarter of the glass substrate had a different barrier layer thickness

from 10 to 30 nm including one non-barrier layer quarter. Using a contact mask, barrier layers of each quarter on the substrate had a thickness from non-barrier devices to 30 nm deposited by the rf-magnetron sputtering technique under the same deposition conditions. More details will be discussed later in TFEL device fabrication section of this chapter.

3.3. Pulsed Laser Annealing Treatment

As a technique for material engineering, the pulsed laser annealing process is investigated for phosphor layer and dielectric layer, respectively. In pulsed laser annealing (PLA or LA) treatment, the most important factors are the excimer laser's energy(or wavelength), the materials' energy bandgap and the pulse characteristics - fluence (energy/cm^2) and pulse duration.

3.3.1 Dielectric layer

For dielectric thin films, Y_2O_3 and BST have different energy bandgaps; Y_2O_3 (E_g = 5.5 ~ 6 eV) and BST(E_g = 3.2 ~ 4 eV). So KrF(λ = 248 nm) excimer laser is not effective on Y_2O_3 materials because the laser energy is just equivalent to only 5 eV while for BST materials, KrF excimer laser can meet this basic requirement. Therefore, higher energy laser system (> 6 eV) such as ArF(λ = 193 nm, 6.42 eV) excimer laser must be employed for laser annealing on yttrium oxide thin films.

Y_2O_3 and BST thin films have been reported to have oxygen deficiency[8] so laser annealing in an oxygen pressurized environment was thought to be desirable, so laser annealing treatments were carried out after depositing dielectric thin films on Si or glass wafers in Ar or O_2 pressurized environment with KrF or ArF excimer laser. The standard laser beam spot size for EL devices was 5 x 5 mm for this research. This basic spot size was employed for MIS capacitors, but the beam spot size could be controlled by modifying optical components for the excimer laser system to meet other specific conditions. In laser annealing, an important parameter is the laser energy density which is called fluence (J/cm^2). By using pyroelectric-type energy detector, the energy density was measured and then the actual absorbed energy on

the materials can be calculated. For dielectrics, the measured laser energy is 10 (±2) mJ which can be converted to average 300mJ/cm² on the materials. The measured calibration chart of the laser fluence as a function of voltage is given in Figure 3-4.

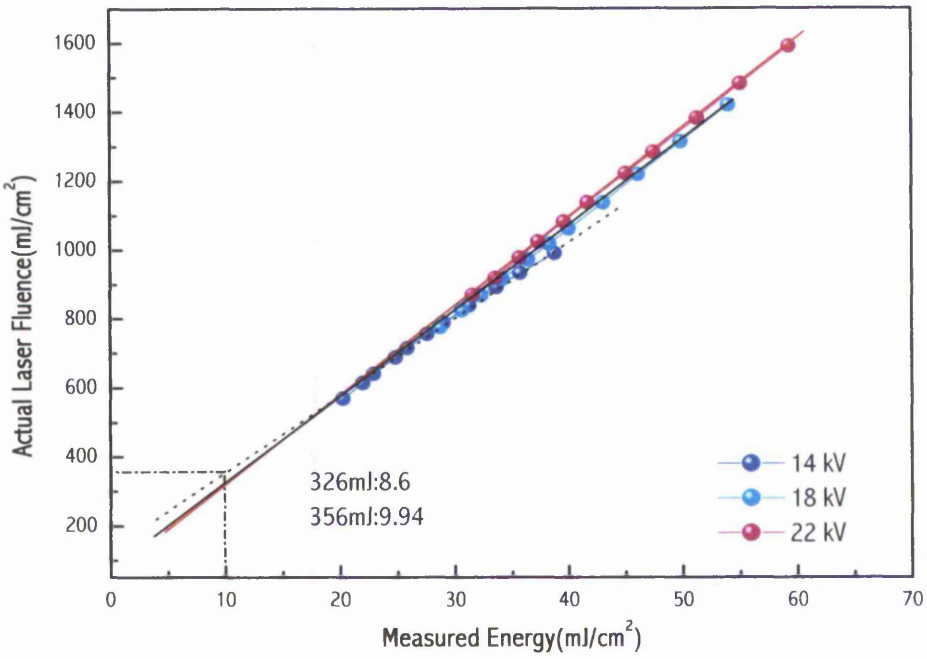


Figure 3-4 The calibration chart of laser fluence as a function of voltage

For the laser annealing process, a LPX® 305i excimer laser system (Lambda Physik GmbH, Germany) was utilized. The sample in the pressurized cell (100~ 150 psi) was controlled by a XZ step motor connected to a computer. HOYA fused silica was used as an attenuator to change the fluence of the laser pulse by adding or removing the glasses. The beam homogenizer consists of two crossed cylindrical lenslet arrays. Its purpose is to split and integrate the beam to convert a non-uniform UV Excimer laser to a homogenous beam so that it can generate homogenized profiles of high quality. In other words, the homogenized beam

has a top-hat (i.e., flat-top) distribution with sharp edges and high uniformity in the plateau area[8,9,10]. The general optic layout and laser system are shown in Figure 3-5.

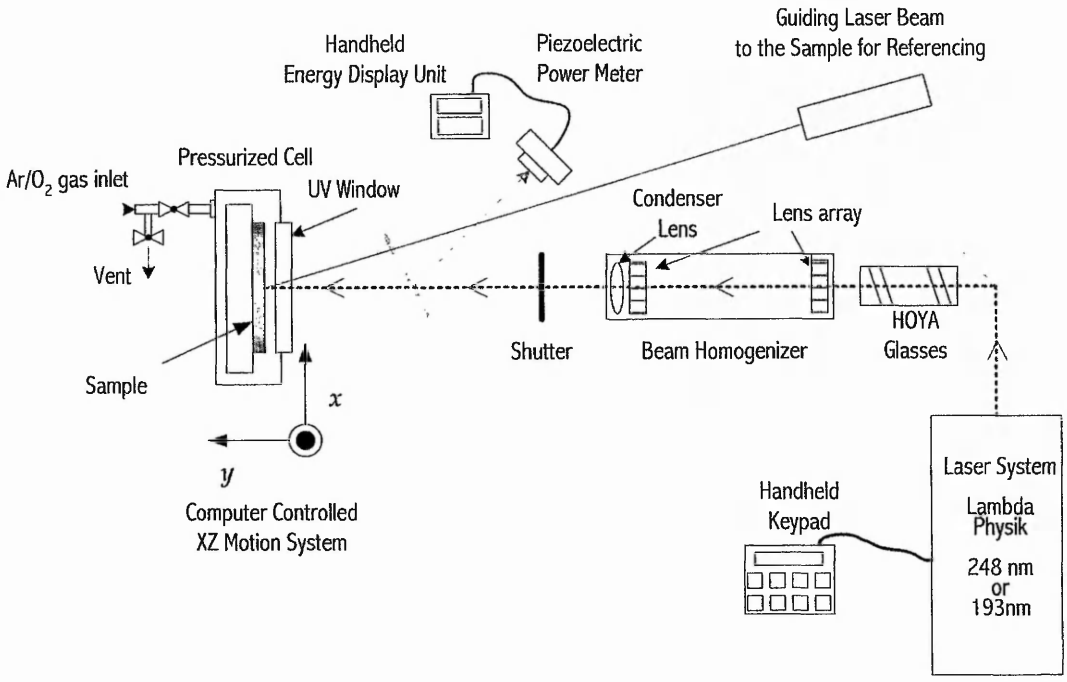


Figure 3-5 Pulsed laser annealing system setup diagram

3.3.2 Phosphor layer

After depositing the bottom phosphor layers, instead of traditional thermal annealing, the phosphor layer was subjected to a pulsed-laser annealing (PLA) treatment under pressure of 150psi in an Ar environment. The PLA experimental system for phosphor layers is fundamentally the same as the system layout used in the case of dielectric layers mentioned in previous section.

For the phosphor-layer-laser annealing, the same excimer laser system(248 nm KrF) was utilised. The energy bandgaps of strontium sulphide (SrS) and zinc sulphide(ZnS) host materials are around 4.3 and 3.6 eV, respectively. According to the relationship between

energy and wavelength (see Equation 3-1), the 248 nm KrF excimer laser pulse is equivalent to 5 eV.

$$E = h\nu = h\frac{c}{\lambda} \text{ (J or eV)} \qquad \textbf{Equation 3-1}$$

where c (light speed) = 2.998×10^8 m/sec, h (plank's constant) = 6.626×10^{-34} joule · sec and 1 joule = 6.242×10^{18} eV

If the laser energy is greater than the energy bandgap, the absorbed energy can be transformed to lattice vibration, i.e., phonon, to generate heat inside of the material. However, the laser energy is smaller than the band gap of the material and the material is optically transparent to the laser energy. Absorption of the energy results in annealing effect of the thin film surface. So the 248nm KrF excimer laser was applied to determine the dependence of laser fluence/energy under various fluence conditions.

3.4. Thin Film Electroluminescent (TFEL) Device Fabrication

The TFEL devices prepared for this study have the same sandwich structure with bottom and top insulating layers as the traditional EL devices[11] described in Chapter 2. Mainly two different types of TEFL devices are fabricated for this study depending on their substrates. TFEL devices fabricated on Si wafers are for lateral light emission, which is called edge emission, while full EL devices on glass wafers are fabricated for surface light emission. As mentioned in the previous section, top Al electrode shapes can be selected according to the EL devices' emission; for lateral emission, line-type Al top electrodes are grown, but circular Al electrodes are deposited for surface emission. These two different contact masks are used. The fabrication steps of TFEL and LETFEL devices are illustrated in Figure 3-6 and 3-8, respectively.

In the TFEL devices investigated here, there are several differences from traditional standard EL devices; the TFEL devices have ① perovskite ferroelectric layers(bottom layer, top layer or both) ② laser annealed layers(dielectric and phosphor layers) ③ barrier layers(Y_2O_3, BST, and both) within phosphor layers.

The barrier layers were deposited with various thicknesses from 10 to 30 nm under the same deposition conditions as the Y_2O_3 or BST's deposition parameters. In order to investigate performance between EL devices having barrier layers and non-barrier layer EL devices, normal TFEL devices without barrier layers were also prepared.

Figures 3-6 shows the steps in fabricating TFEL devices on glass substrates and at the same time illustrates the laser annealing process. Figure 3-7 also shows the top view of the fabricated TFEL devices with laser annealed areas, the Al top electrodes, and different barrier thicknesses on each quarter on ITO-coated glass wafer as a substrate in the experiments. The LETFEL fabrication processes are presented in Figure 3-8. Although the laser annealing process is not shown, laser annealing steps can be added without any difficulty if the laser annealing steps in fabricating TFEL devices of the Figure 3-6 are considered. In the illustrations, the scale of the layer that is growing in each step is exaggerated compared to other layers to identify the step easily.

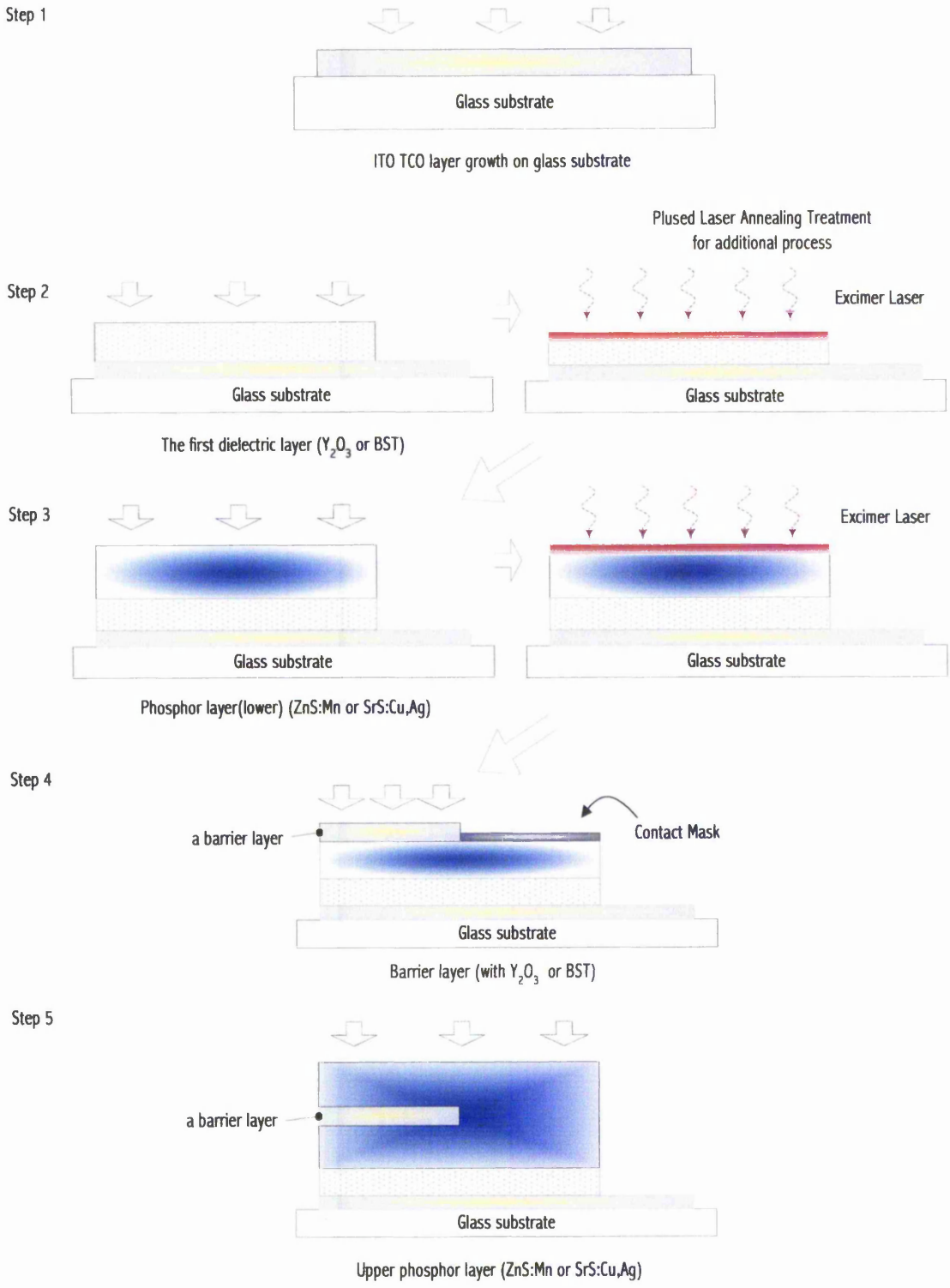


Figure 3-6 TFEL device fabrication Process including a conventional TFEL device, a TFEL device with barrier layer, and laser annealing process.

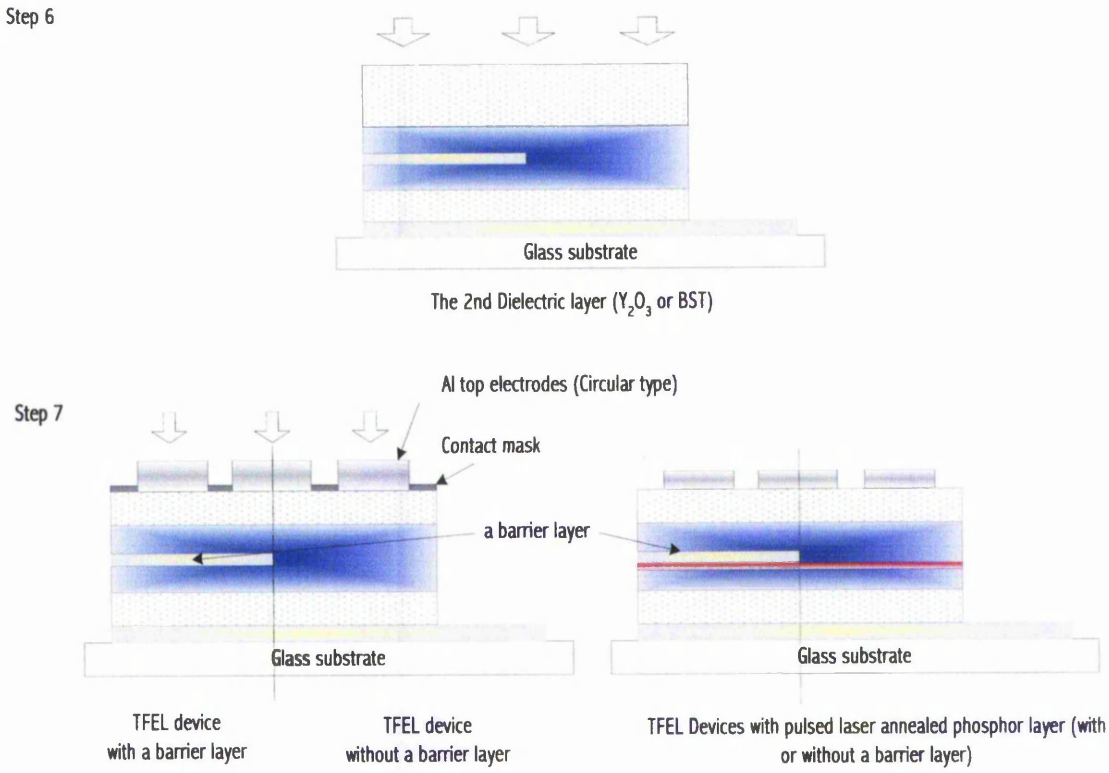


Figure 3-6 Continued: TFEL device fabrication Process

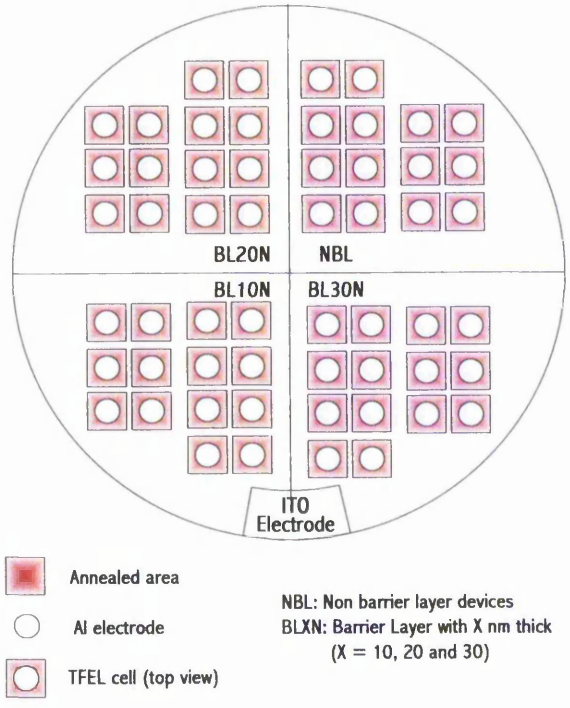


Figure 3-7 Top view of fabricated TFEL devices with various barrier layer thickness and laser annealed area

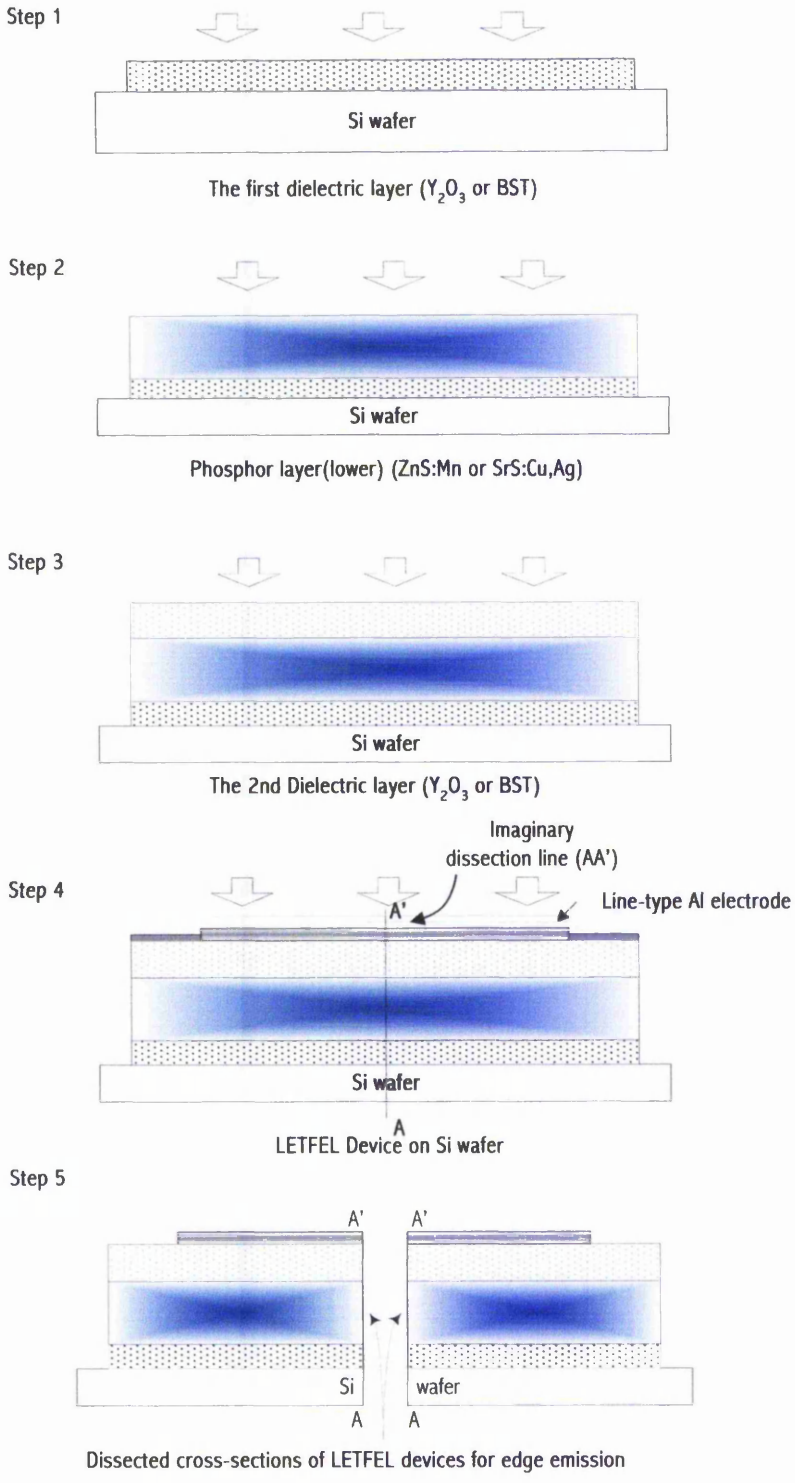


Figure 3-8 Typical fabrication process of LETFEL devices

3.5. Characterization

3.5.1. Electrical and dielectric properties(*C-V* and *I-V*)

Fundamentally, to investigate electrical and dielectric characterization of dielectric thin films including perovskite ferroelectric thin films, capacitance-voltage(*C-V*) and current/current density-voltage(*I/J-V*) measurements were carried out within a custom-made shield probe station using an Agilent(HP) LF impedance analyzer 4192A, and voltage source and pico-Ammeter 4140B. In addition, these *C-V* and *I-V* systems were semi-automatically controlled by a PC via GPIB interface connection. The schematic diagrams of *C-V* and *I-V* probe station and connections are shown in Figure 3-9. LabView™ (National Instrument, US) data acquisition (DAQ) program was used as a main remote controller, but it is not shown in *I-V* measurement setup.

Typical *C-V* curve patterns of MOS structure capacitors are illustrated in Figure 3-10 according to the type of a Si substrate and applied voltage (i.e., gate voltage (V_g)). There are three different regions which are called accumulation, depletion and inversion regions. A gray *C-V* curve (see Fig. 3-10) and letters show the general characteristics of p-type Si substrate. In the case of a p-type silicon, with a negative voltage applied to the metal side, an accumulation of majority carriers are near the semiconductor surface due to a band bending effect. This is the "accumulation" situation. As the polarity is reversed, the holes accumulated at the semiconductor surface go away from the surface so the majority of carriers are depleted (depletion case). As the stronger positive voltage is applied, at the surface of semiconductor the electrons concentration density is larger than that of the holes. Thus, the surface is inverted. It is called "inversion"[2,12]. At accumulation, the MIS capacitance is only due to the insulator. Therefore, the capacitance is calculated by the following equation[2]:

$$C_o = \frac{\varepsilon_o A_o}{d_o} \qquad \textbf{Equation 3-2}$$

where, ε_o, A_o, and d_o mean the insulator dielectric constant, area, and thickness, respectively.

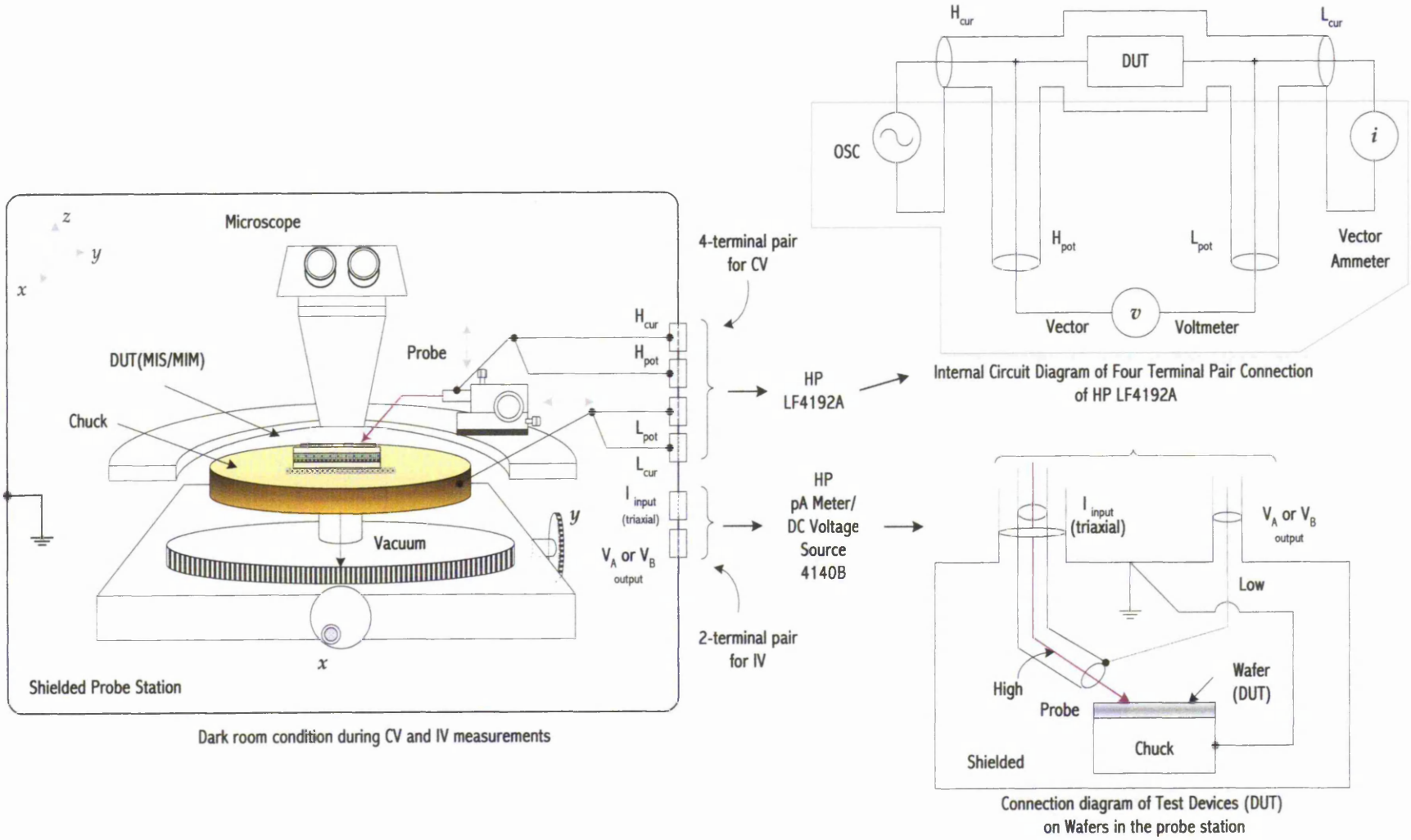


Figure 3-9 A shielded probe station of *C-V* and *I-V* measurements:4-terminal pair connection(*C-V*) and *I-V* setup for a DUT on a wafer

For *C-V* measurements, the MOS (or MIM, MIS) capacitors are connected to the analyzer using 4-terminal pair (4TP) connection technique[13]. The capacitance-voltage measurements are used for determining dielectric constant, capacitance, flatband voltage (a voltage at which there is no electric charge in the semiconductor and no voltage drop across it; (V_{FB}) and other important properties of unknown dielectric materials directly or indirectly(i.e., via simple calculations). *I-V* characterization, leakage current, breakdown voltage (E_{bd}) and figure of merit (FOM) or charge storage capacity (CSC) of the materials applied in EL devices can be obtained. Figure of merit or charge storage capacity (CSC) is used for one of the criteria for evaluating or selecting insulating materials for TFEL devices and expressed as a product of breakdown voltage (E_{bd}) and dielectric constant (ε_r):

$$\text{Figure of Merit (or CSC)} = E_{bd} \times \varepsilon_o \times \varepsilon_r \qquad \textbf{Equation 3-3}$$

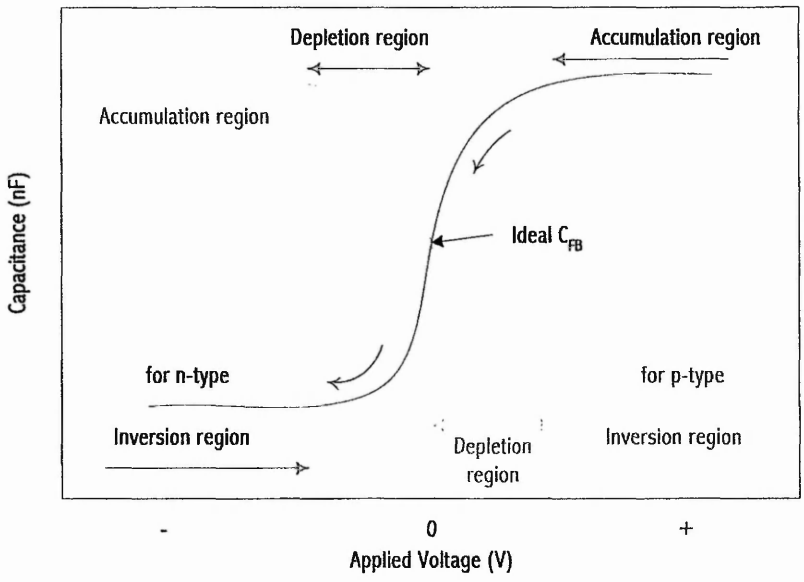


Figure 3-10 Typical *C-V* curve patterns of the MOS structure capacitors with n- or p-type (gray lines and texts, and regions) semiconductors

3.5.2 Thin film thickness measurement

In the previous section, it was explained how the dielectric constant can be obtained through the capacitance-voltage (*C-V*) measurement. The dielectric constant of the unknown test materials with a parallel capacitor structure significantly depends on its thickness. Therefore, theoretically and practically the measurement of thin film thickness has very important meaning.

For this measurement, three different thickness measurements are investigated for improving and confirming validity of the obtained thickness data of the test thin films: ① *in-situ* interferometric technique by using 670 nm laser beams when the thin films are deposited on the substrate (see Fig. 3-2), ② after deposition, the second thin film measurements are conducted by spectral reflectance technique with FILMETRICS F20 system (Fig. 3-11), ③ fine-tipped stylus based method (Fig. 3-12); stylus measurements can measure thickness and roughness of the materials by detecting the deflections of the stylus when it is dragged along the surface of the test thin films.

The thickness of each thin film grown was monitored in real-time by an *in-situ* interferometric system with 670 nm wavelength laser attached to the deposition chamber. The thickness of thin films deposited can be calculated by thin film interference theory according to the reflective index (n) of the material and wavelength used for the interferometric method. Deposition progress for thin film thickness is recorded on the computer system (Pico A-D Converter system, Pico technology). The equations of thin film interference are given in Equation 3-4 and 3-5.

$$2nd = (m + 1/2) \cdot \lambda \qquad \textit{(maxima), where } m = 0, 1, 2, \ldots \qquad \textbf{Equation 3-4}$$

$$2nd = m \cdot \lambda \qquad \textit{(minima), where } m = 0, 1, 2, \ldots \qquad \textbf{Equation 3-5}$$

where, n is refractive index, d film thickness and λ wavelength of laser beam (= 670 nm).

After deposition, each thin film thickness can be confirmed by using spectral interference system (F20 FILMETRICS™, US) and a stylus-type Dektek system (6M, Veeco), which are shown in Figures 3-11 and 3-12, respectively.

The mentioned three thin film measurements above can be categorized in two subgroups: optical and stylus based techniques. Actually, the first two methods have the same theory, but the only difference is the light beam and light incidence. In other words, one uses a coherent laser beam and the other one uses a white beam with wavelengths from 215 up to 1700 nm (near infrared (IR) to ultraviolet (UV)). In addition, like ellipsometry, the coherent laser beam is not normally incident while the white light beam should be normally incident on the thin film to obtain the spectral reflectance. The optical fiber has six sub-fiber optics as light sources and one detector for reflected light from the thin film. The schematic diagrams of these different thin film thickness measurements used in the study are given in Figure 3-2, 3-11, and 3-12.

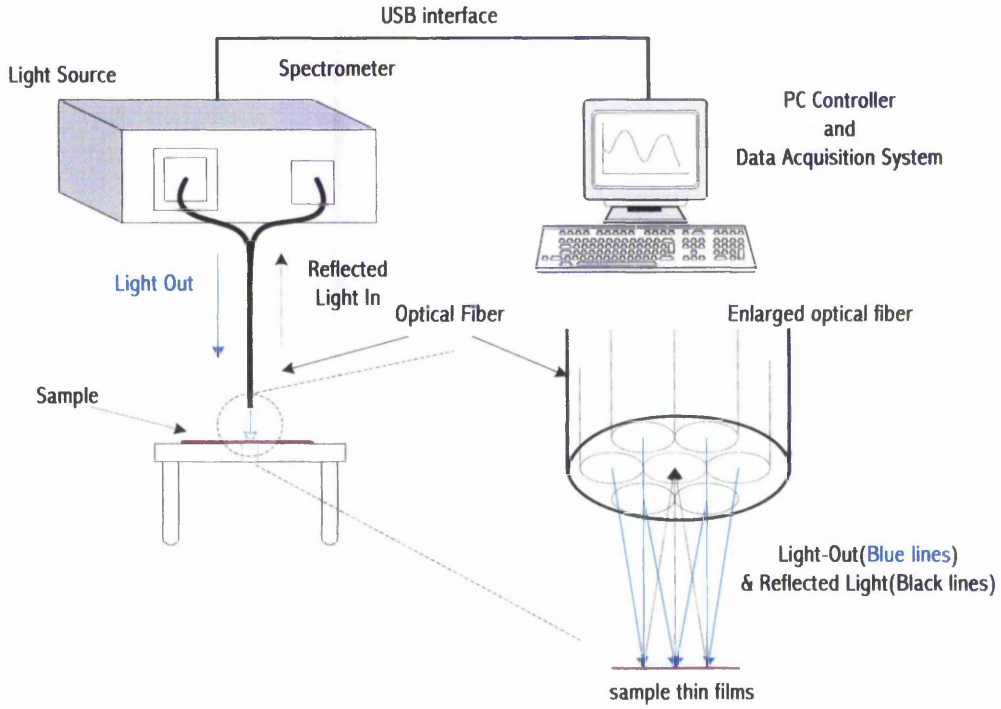


Figure 3-11 Spectral interference system and fiber optic cable diagrams (Filmetrics™)

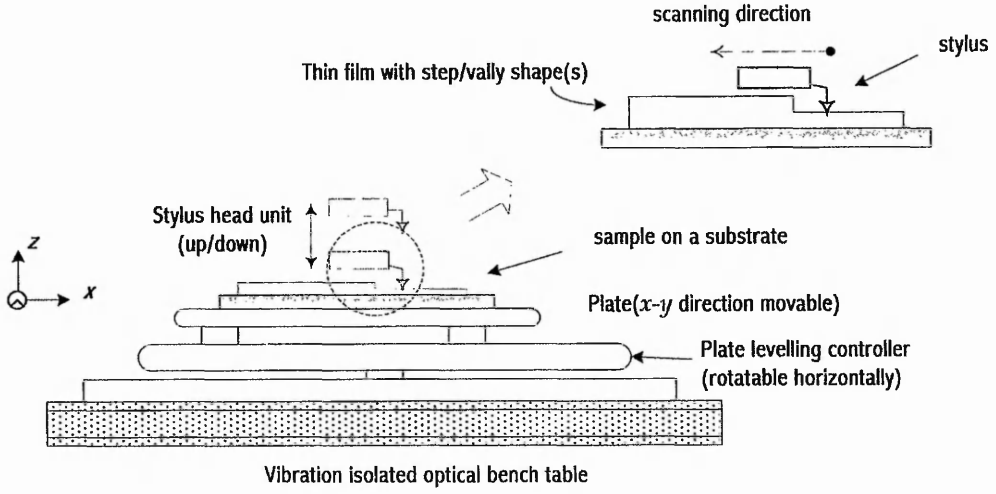


Figure 3-12 Dektak stylus thickness measurement system

3.5.3 Chemical, Physical and Structural Characterizations

In order to investigate structural properties of dielectric and phosphors thin films and particularly phase transitions and crystallinity of ferroelectric materials as a function of annealing temperature and annealing methods, X-ray diffraction(XRD)[14] experiments are performed on BST, Y_2O_3, SrS, and ZnS phosphor thin films. In this experiment, a Philips's X-ray diffractometric system is utilised and the x-ray source material is chromium (Cr, $\lambda = 2.2897$; Ka_1). The applied power was fixed at 20mA and 40kV. The step angle and speed were 0.02° and $1^\circ/\text{min}$, respectively.

The Bragg equation for X-ray diffraction is:

$$n\lambda = 2d\sin\theta \qquad \textbf{Equation 3-6}$$

where, n is integer which means the order of diffraction. The wavelength (λ) of X-ray is 2.2897 Å. From the equation, $\sin\theta = \lambda/2d$ can be rewritten and the magnitude of the sine function must be in $-1 \leq \sin\theta \leq +1$ so that $\lambda/2d$ has the same magnitude, but it basically can not be negative due to the value of sine function (eg, $0 \leq \sin\theta \leq 1$, $0 \leq \theta \leq 2\pi$). Therefore, $0 \leq \lambda/2d \leq 1$ is the important relationship between x-ray wavelength and the lattice interplanar spacing (d-spacing); the condition $2d \geq \lambda$ must hold. Compared to Cr and Cu's wavelength, the difference in the two sources could be understood easily. Therefore, when the chromium x-ray source is used, according to the test materials, the range of measurement angle (i.e., 2 theta) should be expanded up to 120° because of its longer wavelength.

A schematic diagram of the X-ray diffraction is shown in Figure 3-13. The X-ray diffractometric system (PW 1049/10, Phillips) used for this research consists of four components generally; ①X-ray source, sample holder and goniometer, ②Power(current and voltage) supplier, ③Counter and Controller(PC), and ④chiller.

A relationship that predicts the possible angle for any set of planes for diffraction directions and indexing patterns of crystals can be obtained by combination the Bragg law and the interplanar spacing (i.e., d spacing) equation which depends on a type of crystal systems. Figure 3-14 illustrates a visualization of the relationship between Bragg equation for x-ray diffraction and the d-spacing.

For an example, in a cubic system like Y_2O_3 and BST, Equation 3-9 can be obtained by manipulating two equations – Equations 3-7 and 3-8. According to Equation 3-8, possible diffraction angles and diffraction directions of the cubic crystal planes can be predicted. Similarly, possible diffraction angles and directions of the hexagonal crystal system such as ZnS can be determined by the following equations - 3-10 ~ 3-12. In X-ray diffraction, the lattice constant (unit cell size) and unit cell crystal system determine only the diffraction directions[15,16,17].

For the cubic crystal system,

$$\lambda = 2d\sin\theta \qquad \textbf{Equation 3-7}$$

$$\frac{1}{d^2} = \frac{(h^2 + k^2 + l^2)}{a^2} \qquad \textbf{Equation 3-8}$$

$$sin^2\theta = \frac{\lambda^2}{4a^2}(h^2 + k^2 + l^2) \qquad \textbf{Equation 3-9}$$

For the hexagonal crystal systems,

$$\frac{1}{d^2} = \frac{4}{3}\cdot\frac{(h^2 + hk + k^2)}{a^2} + \frac{l^2}{c^2} \qquad \textbf{Equation 3-10}$$

$$2logd = 2loga - log\left[\frac{4}{3}(h^2 + hk + k^2) + \frac{l^2}{(c/a)^2}\right] \qquad \textbf{Equation 3-11}$$

$$sin^2\theta = \frac{\lambda^2}{4}\left[\frac{4}{3}\cdot\frac{(h^2 + hk + k^2)}{a^2} + \frac{l^2}{c^2}\right] \qquad \textbf{Equation 3-12}$$

where, λ means the wavelength of x-ray source material employed, a and c are lattice constants for the cubic(a only) or hexagonal structures(a and c) , d is a distance of layers, θ is the incident angle of the x-ray on the surface and h, k, l are the miller indices.

Thin film surface morphology and interface between layers were characterised by a scanning electron microscopy (SEM) (JEOL JSM 5410) system at NTU. The general preparation of the sample for SEM characterisation was obtained elsewhere[18,19]. When dielectric thin films are characterised by SEM, it is necessary to coat a thin metal electrode layer on the dielectric material to avoid the electron charging problem. Therefore, a thin metal (eg, Au is commonly used) is deposited before SEM characterisation.

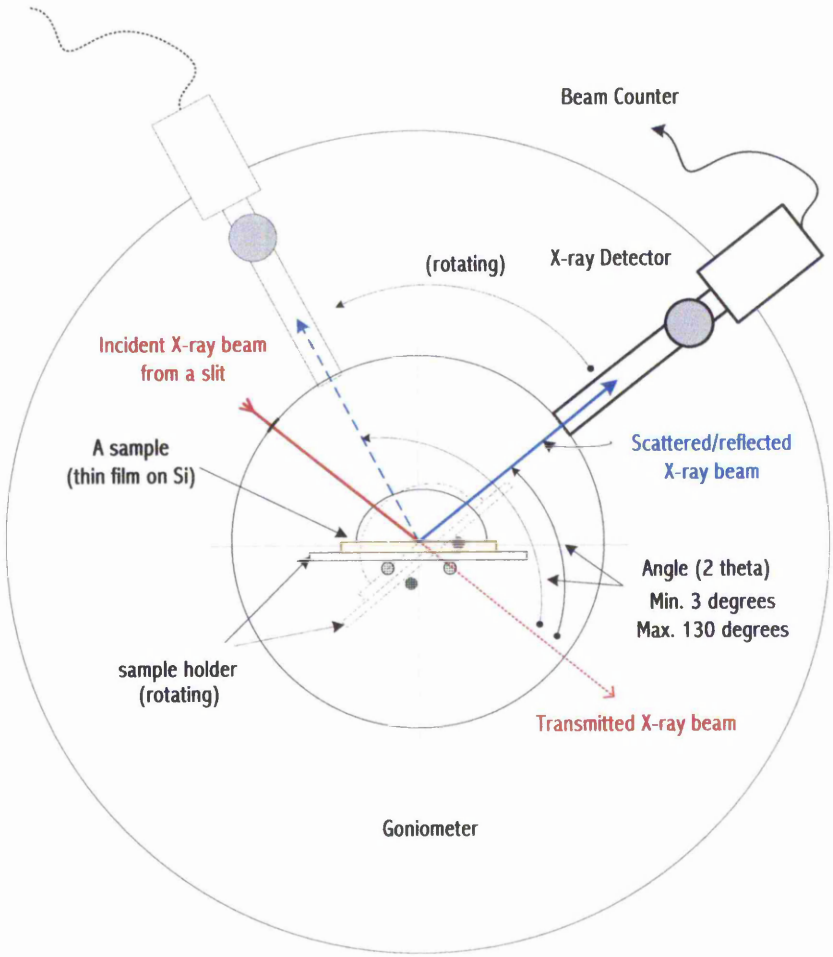


Figure 3-13 Diffracted X-ray and simplified goniometer diagram of X-ray diffractometer

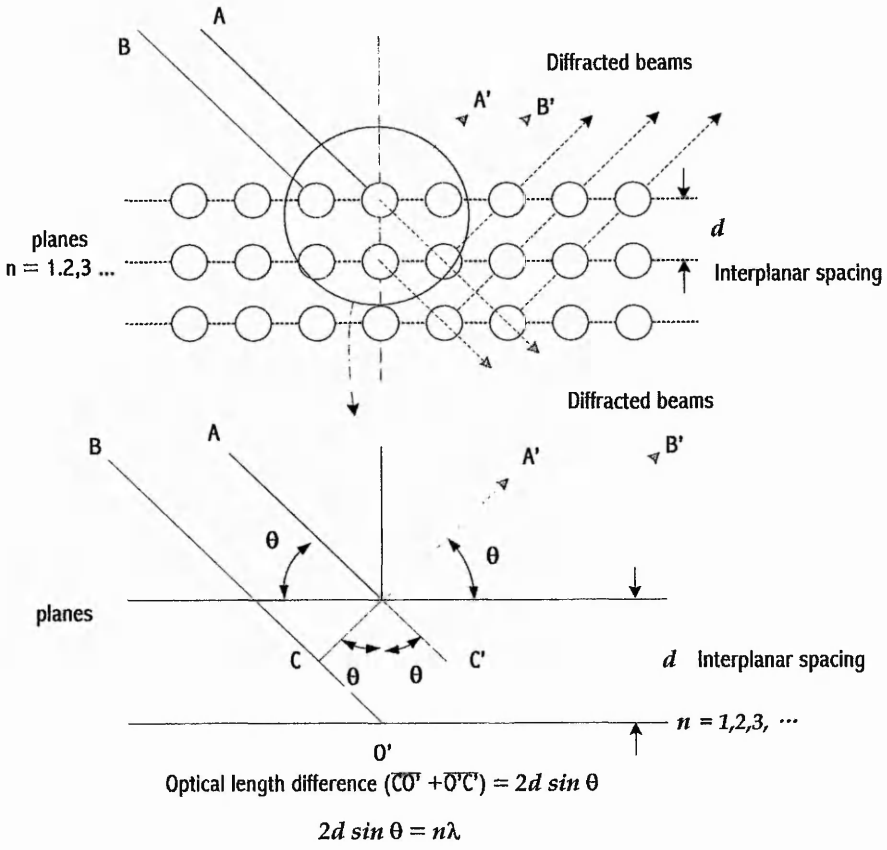


Figure 3-14 Illustration of Bragg condition and lattice interplanar spacing (eg, a cubic structure)

3.5.4 Operational characterization of TFEL devices

In this section, several characterizations for evaluating full TFEL device performance will be discussed. There are internal and external evaluations; i.e., luminescence-related measurements such as photo- and electro-luminescence can be external, and transient measurements of electroluminescence of the devices are an important method for understanding the internal mechanism.

3.5.4.1 Luminescence: Photo-(PL) and Electro-luminescence(EL)

Photoluminescence (PL) measurements are applied for laser-annealed and non-laser-annealed phosphor layers. PL experiments with an Omnichronme He-Cd laser system (Melles Griot, USA) as an external monochromatic light source was carried out at room temperature in a dark room environment. Photoluminescence is one of the characteristic properties of phosphor materials. Electrons of a valence band excited by the laser source jump to a conduction band. During the transition from excited energy levels to grounded energy states as a recombination process, the light emits from energy difference between two different energy levels - excited and ground energy levels. The light emissions from PL were fed into the fiber optic and measured and saved by a computer-controlled acquisition system (S2000 OOIBase, Ocean Optics). The He-Cd laser system can produce two different wavelengths - 325 and 442 nm, but the wavelength of 325 nm (= 3.81 eV) was used for PL experiments. The PL measurement setup is shown in Figure 3-15.

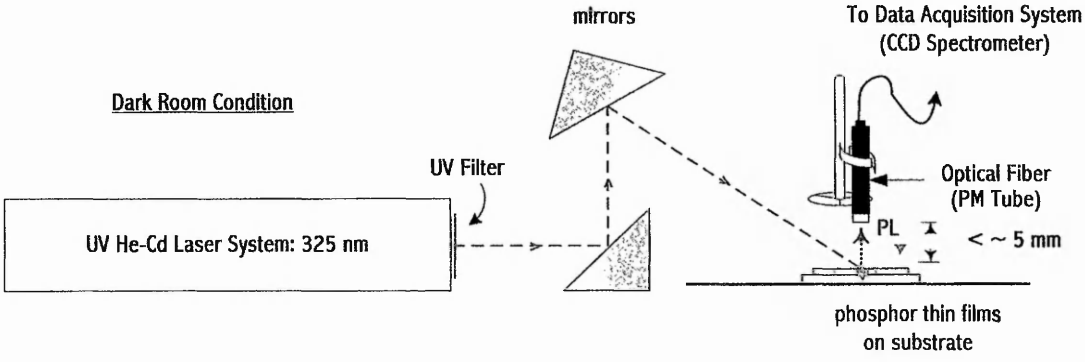


Figure 3-15 Photoluminescence (PL) Measurement System Setup

Electroluminescence (EL) characterization of EL devices is one of the important device characterization parameters along with PL. Before carrying out EL measurements, full TFEL devices were fabricated with the deposition parameters mentioned above. In order to measure EL properties of the devices, ac voltage using a sine wave function generator (5 kHz) and amplified voltage (up to 700 V pk-pk) was applied to EL devices and then by slowly increasing the voltage, at a certain threshold voltage the EL devices finally started to emit its native light, which depends on the phosphor material and activators (i.e. luminous centres).

There are two different EL measurement setups used; 1) lateral emission and 2) surface emission. For lateral emission, top and bottom dielectric layers act like a cladding of optical fibers so that according to the refractive index difference between phosphor and dielectric layers, the total internal reflection condition can be satisfied. Therefore, these three layers can be understood as an optical waveguide. For the total internal reflection condition, the critical angel for that can be obtained by the following equation:

$$sin\theta_c = \frac{n_i}{n_p} \qquad \text{Equation 3-13}$$

where, n_i and n_p mean the refractive index of the insulating layer and the phosphor layer, respectively. The angle θ_c is the critical angle for total internal reflection. Therefore, if the incidence angle is the larger than the critical angle, θ_c, total internal reflection always takes place.

The light emission should originate in an optically dense medium like the phosphor layer in terms of total internal reflection. For example, in a Y_2O_3 (n_i = 1.9) layer and in ZnS (n_p = 2.35), the critical angle will be 53.95°. The lateral emission by the optical waveguide effect is illustrated in Figure 3-16. Effectively, the luminescence efficiency is generally greater than that of the surface emission. The lateral emission measurement can be important in evaluating the EL device. The test devices for lateral emission measurement are prepared by simply cleaving the middle point of the line-type Al electrode of EL devices. The measurement is performed with a Minolta LS110 luminescence meter with a close-up lens (no. 122 and 1.1 mm measuring diameter). The test device and Minolta are aligned and the image of the cleaved EL cell is focused in the eyepiece to ensure that the object plane measured is at the cleaved facet of the device. The distance between the test device and Minolta luminance meter is approximately 25 cm. The schematic diagram of a lateral emission measurement, a top view of LETFEL device with line-type Al electrode and an alignment of a cleaved test cell with a circle in a viewfinder (the true circle is larger than that of a figure) are shown in Figure 3-17.

In the surface light emission measurement, the measurement system is similar to the PL measurement setup with electrical driving components consisting of a function generator, high

voltage amplifier, oscilloscopes, and remote PC controller instead of the He-Cd laser system to generate light emission of EL device. In addition, the photomultiplier tube (PMT) as a light detector contacts the whole EL cell in order to measure emitted light intensity (brightness) and light spectrum (wavelength). Measured data can be saved by a computer-controlled data acquisition CCD S2000 spectrometer (Ocean Optics, USA). The multi-purpose vacuum probe station and its block diagram of EL measurement is given in Figure 3-18 and 3-19. The circuit is well known as the Sawyer-Tower circuit[20,21], which is used to measure transferred charge density (ΔQ) and instantaneous current and then each capacitance of insulating and phosphor layer, a total capacitance of a whole EL cell(a pixel), luminous efficiency and threshold voltage are calculated from measured Q-V and I-V data and their waveforms on the electrical characteristics of the devices.

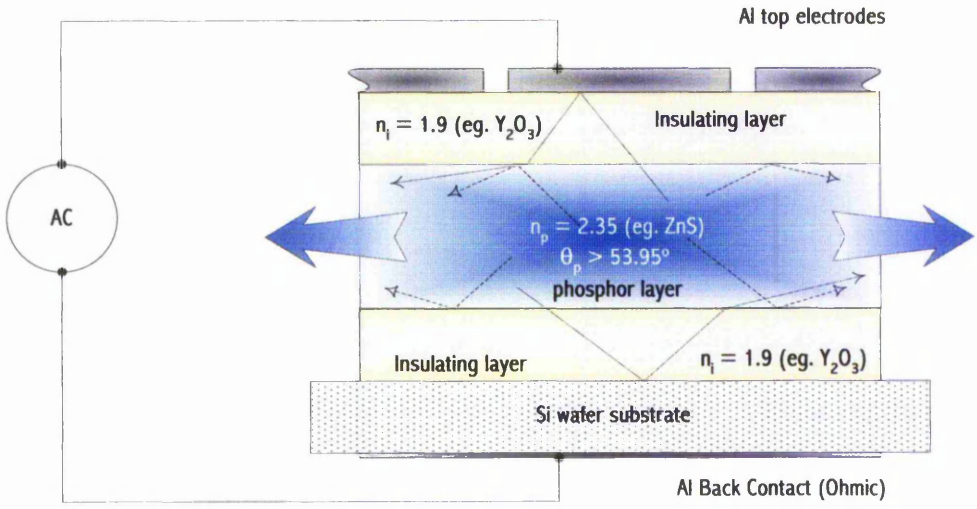


Figure 3-16 Optical waveguide effect under lateral emission of LETFEL device

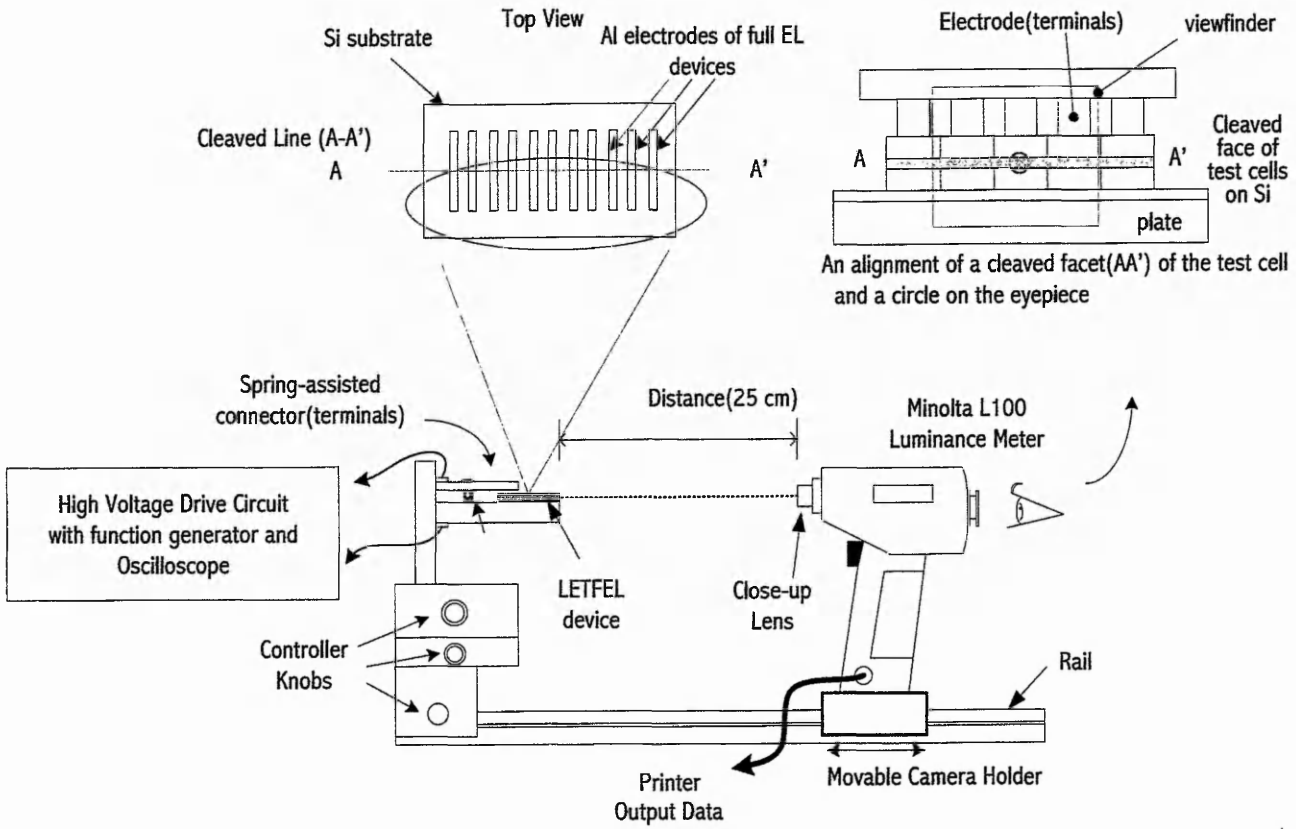


Figure 3-17 A schematic diagrams of lateral emission luminance measurement set up

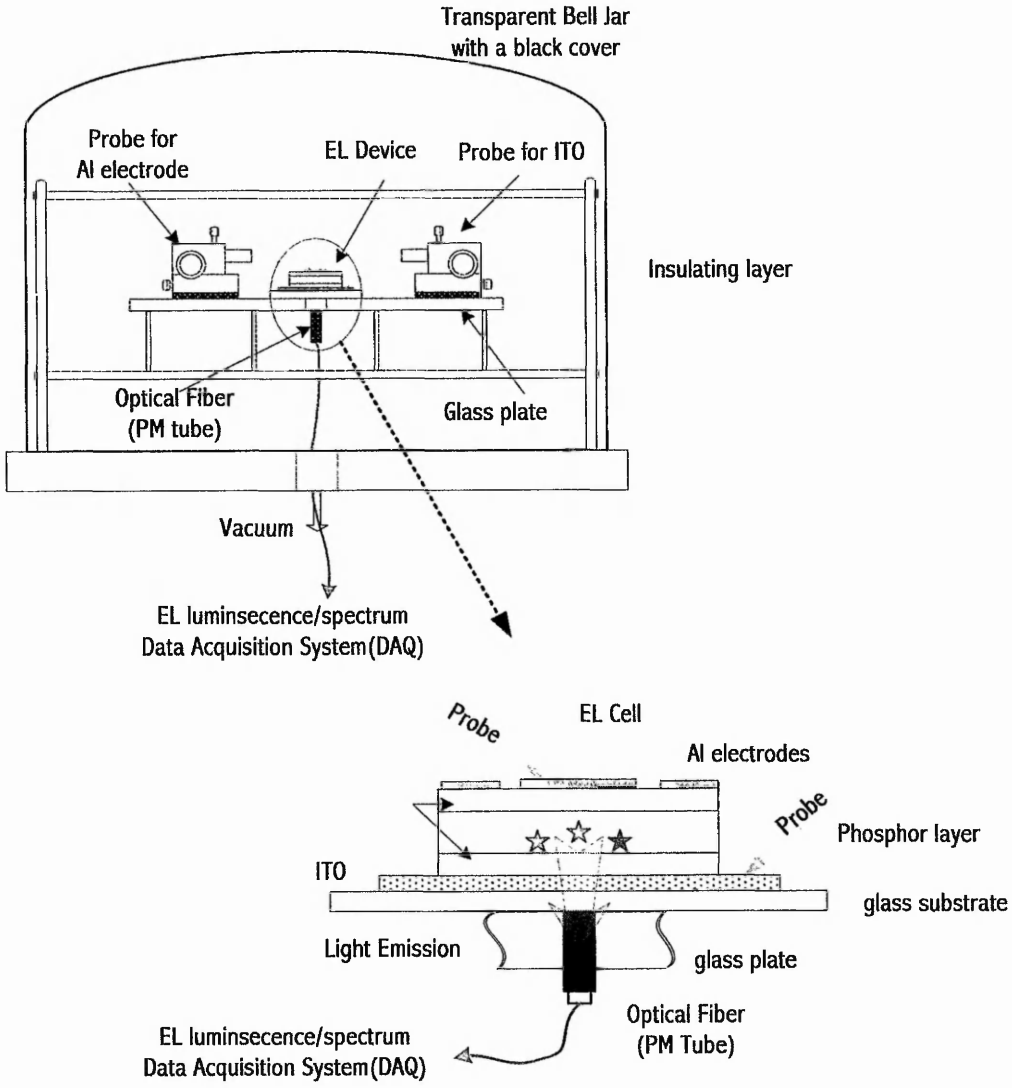
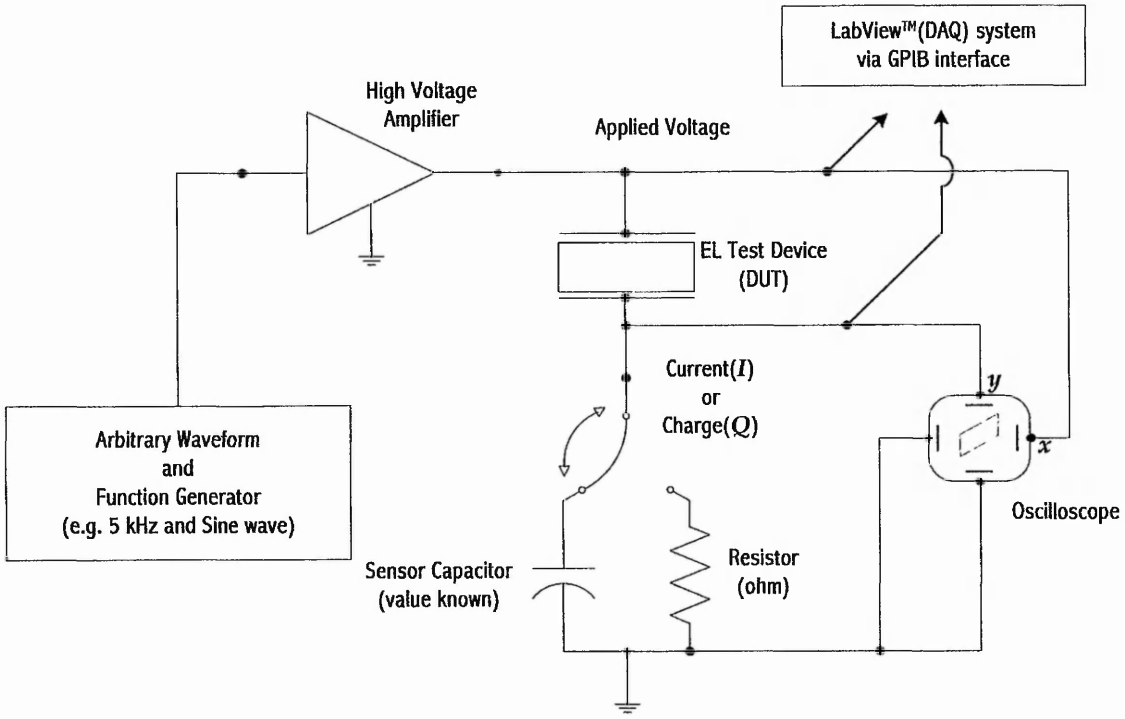


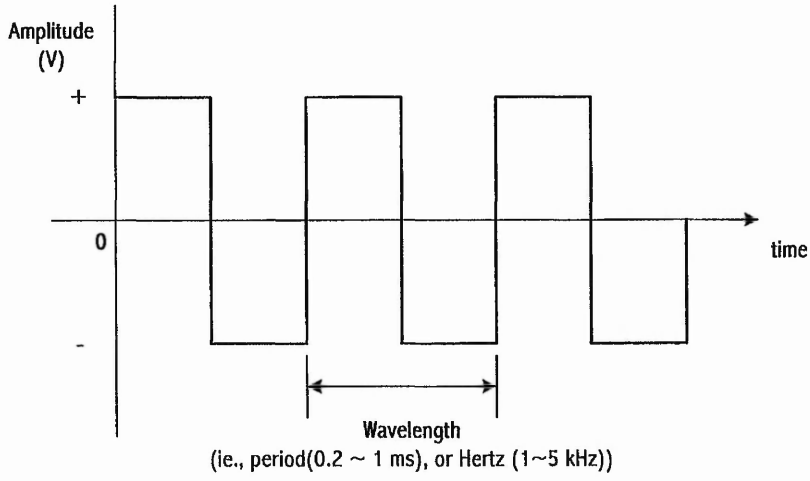
Figure 3-18 Multi-purpose vacuum probe station for EL measurement

3.5.4.2 Transient Measurement

Through a measurement of the transient light emission properties, it is possible to obtain information on the internal emission mechanism, the role of dielectric layers and an emission (PL and EL) decay time of the EL devices. From this transient measurement, the effect of perovskite ferroelectric layers within in EL devices will be discussed. In general, instead of a sine wave, a bipolar trapezoidal wave is used for transient measurement. However, a bipolar rectangular pulse without return-to-zero value for EL emission transient response was used in this experiment. In addition, for this experiment, the transient characteristic data were captured using the data acquisition system - LabView™. The system configuration for transient measurement was the same as for the EL spectrum measurement with the addition of the LabView program, waveform and minor settings (See Figure 3-19).



(a)



(b)

Figure 3-19 Block Diagram of EL measurement Setup for *I-V* and *Q-V* experiment: (a) Sawyer-Tower Circuit, (b) input waveform for transient measurements

REFERENCES

[1] Wasa, K. and Hayakawa, S, *Handbook of sputtering deposition technology*, 1992

[2] Ohring, Milton, *The materials science of thin films*, Academic Press, 1992

[3] Stuart, R. V. *Vacuum Technology, thin films, and sputtering*, Academic press, 1983

[4] O'Hanlon, J. F. *A User's Guide to Vacuum Technology*, John-Wiley Interscience, 1980

[5] Geroge, Joy, *Preparation of Thin films*, Marcel Dekker, 1992

[6] Hill, Russell J. *Physical vapour deposition*, Temescal, 1986

[7] Ditum, C. M. ***PhD thesis***, The University of Birmingham, 2002

[8] Koutsogeogis, D. C. ***PhD thesis***, Nottingham Trent University, 2003

[9] Basting, Dirk. *Excimer Laser Technology*, Lambda Physik, AG, 2001

[10] Ready, J. F. *LIA Handbook of laser materials processing*, LIA, 2001

[11] Inoguchi, T, et al, Proceedings of SID digest, p. 84, 1974

[12] Sze, S.M. *Physics of Semiconductor Devices 2nd Ed.* John-Wiley, 1981

[13] Agilent Technologies, *Agilent Technologies Impedance Measurement Handbook*, 2003

[14] Brundle, C. R. et al. (Eds.), *Encyclopedia of Materials Characterization: Surfaces, Interfaces, Thin Films*, Ch 4. Butterworth-Heinemann, 1992

[15] Cullity, B.D. *Elements of X-ray Diffraction*, 2nd Ed. Addison-Wesley, 1978

[16] Pecharsky, V. K. and Zavlij, P. Y. *Fundamentals of Powder Diffraction and Structural Characterization of Materials*, Kluwer Academic Publisher, 2004

[17] Hammond, Christopher *The Basics of Crystallography and Diffraction*, 2nd Ed. Oxford University Press, 2001

[18] Hearle, J.W.S. et al., *The Use of the Scanning Electron Microscope*, Pergamon Press, 1972

[19] Brundle, C. Richard, et al. (Eds.) *Encyclopedia of Materials Characterization – Surface, Interfaces, Thin Films*, pp. 70-85 (Sec. 2.2), Butterworth-Heinemann, 1992

[20] Jona, Franco and Shirane, G., *Ferroelectric Crystals*, Ch 1., Dover 1993 (Originally published in 1962 by Pergamon Press)

[21] Ono, Yoshimasa A. *Electroluminescent Displays*, p. 35, World Scientific, 1995 (reference therein)

Chapter 4 Y_2O_3 MIS Capacitors and Their Characterisation

Overview

Yttrium oxide (Y_2O_3) thin films are dealt with in this chapter. Yttrium oxide, or yttrium sesquioxide is known as one of the very important compound materials and has various applications in microelectronics such as a thin film (gate) insulator[1,2,3], phosphors[4,5,6], and lasers[7]. In order to evaluate the dielectric thin film, the background theory and measurements of general MIS devices are discussed in the first part of this chapter. In the second part, the characterisation of Y_2O_3 MIS devices will be discussed including the structural, electrical and dielectric properties of yttrium oxide thin films.

4.1 Fundamentals of Ideal MIS(Metal-Insulator-Semiconductor) Devices*

The metal-insulator-semiconductor or MIS§ structure has great importance in semiconducting devices of microelectronics. In this section, the two-terminal MIS capacitor with a dielectric thin film will be discussed as a part of evaluating electrical and dielectric properties. In order to investigate the MOS capacitors, the capacitance-voltage(*C-V*) characterisation which was explained in the previous chapter is utilised. From *C-V* measurement, several important properties of the dielectric materials can be obtained.

A typical MOS structure and its equivalent circuit are shown in Figure 4-1. The capacitance of MOS junction structure depends on the magnitude and polarity of the gate bias. In addition, the total capacitance consists of two capacitors with a series connection - C_{oxide} and C_{si}. Generally, the capacitance is measured through the superimposed small ac probe bias over a dc voltage[8,9].

It is very useful to visualise general phenomenon in energy and block charge diagram of MOS capacitor structure in response to an applied bias (V_G). Figure 4-2 shows the energy band diagrams and charge distribution of an ideal MIS capacitor when the gate voltage is applied.

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* For general MIS capacitor characterisation (eg., *C-V*), its theory, equations and additional notes are discussed in Appendix A and B sections
§ The term, MIS is more general, but MIS and MOS are used as the same meaning and interchangeable in this chapter.

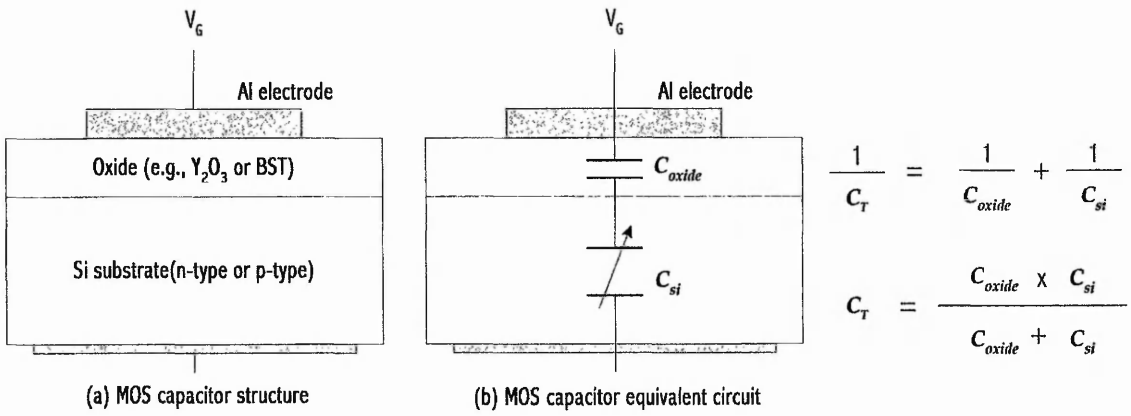


Figure 4-1 A simple metal-oxide-semiconductor (MOS) capacitor structure, its equivalent circuit, and total capacitance(C_T) equation. The capacitance of the Si substrate is a function of gate voltage.

When a MOS capacitor is biased with positive or negative voltage, the surface capacitance of the semiconductor changes. Therefore, the band bending effect takes place at the surface of the semiconductor. Figure 4-2 illustrates this band bending phenomenon at the n-type silicon semiconductor surface according to the applied bias polarity and its magnitude. To avoid ambiguity in sign convention, the sign convention for applied bias between the metal gate (Al) and silicon substrate will be the polarity on the metal gate with respect to the substrate, silicon. Practically, the silicon substrate is grounded at any time when *C-V* measurements are initiated.

There are important reference energy levels in solid state physics: vacuum and the Fermi level (E_F), and the electron affinity (χ). The electron affinity is the energy difference between the conduction band edge and the vacuum level in the semiconductor. The work function (ϕ)# which is the energy difference between the Fermi level and the vacuum level(ϕ_m for the metal and ϕ_{si} for the silicon semiconductor) is also shown in Figure 4-2(A). This is the minimum energy required for an electron escaping into vacuum from the surface of the solid. When the metal - oxide - semiconductor is in contact, the Fermi and vacuum levels must be continuous in thermal equilibrium condition. These requirements and graphical definitions of energy parameters for the ideal MOS device are shown in Figure 4-2(A).

Work function is energy (i.e., eV or J) in its unit so that $q\phi$ is correct. In calculation, the charge should be considered.

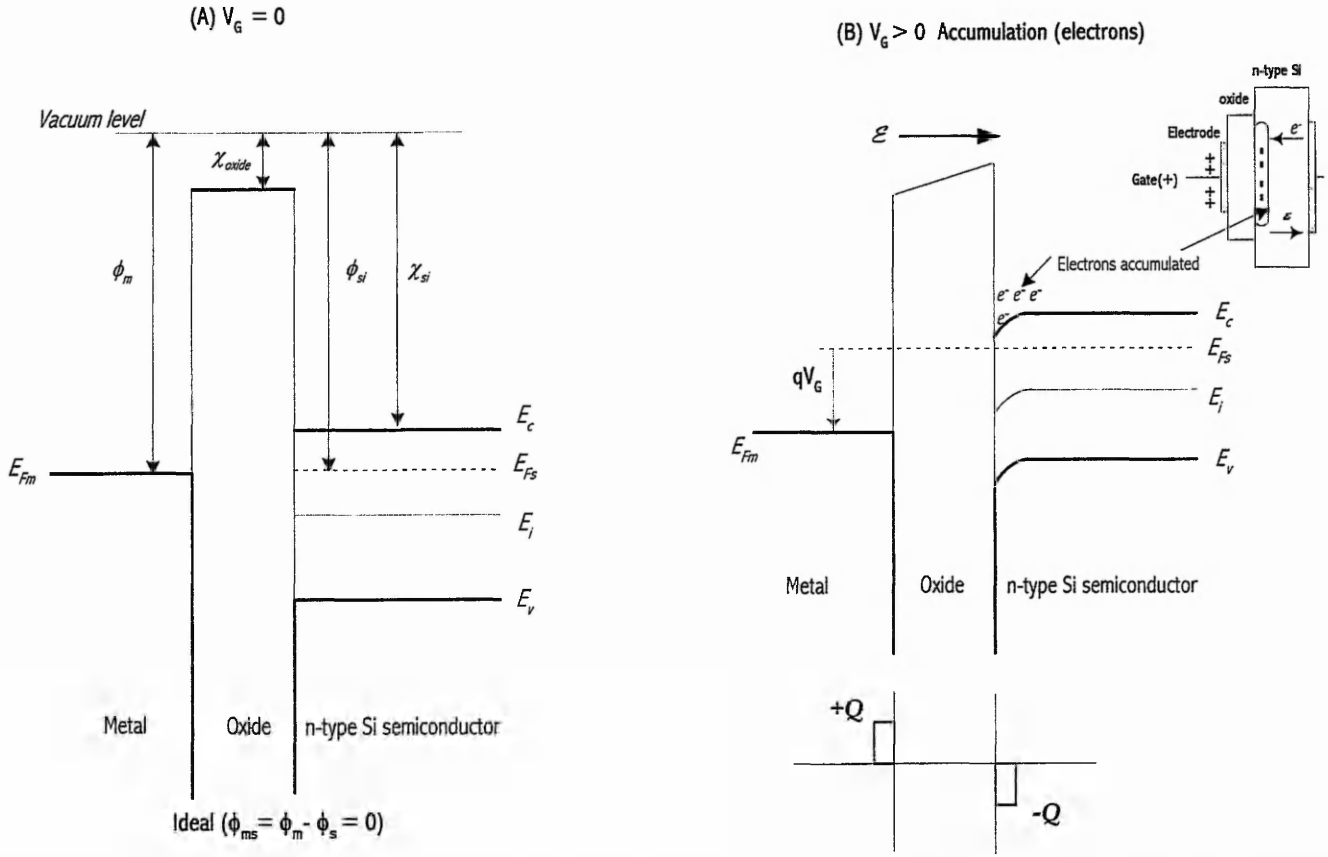
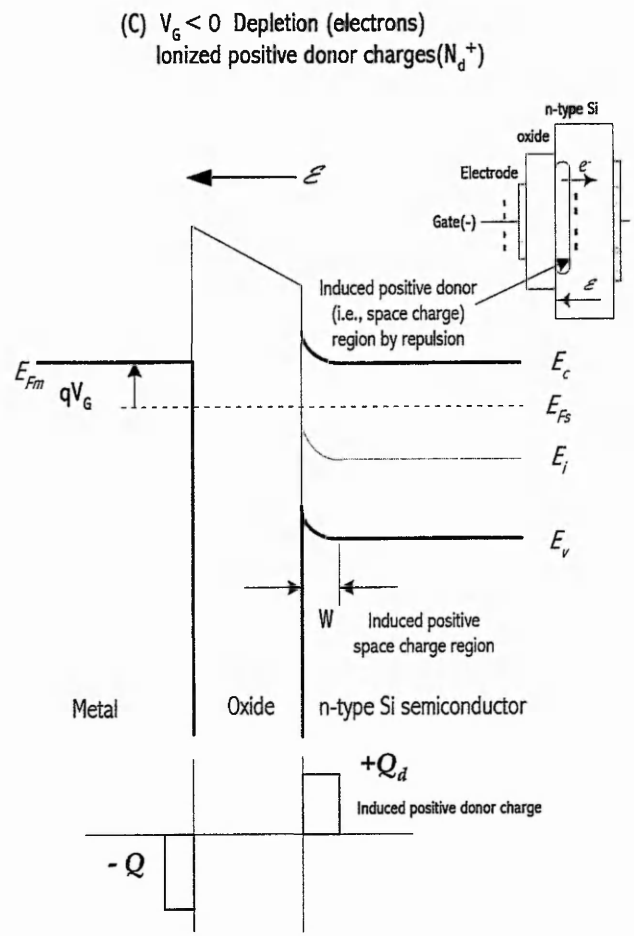


Figure 4-2 Energy band diagrams and charge distributions of an ideal metal-oxide-semiconductor(*n-type*) capacitor based on applied gate voltage conditions: (A) ideal MOS capacitor before contact, (B) accumulation($V_G > 0$), (C) depletion($V_G < 0$) and (D) inversion state($V_G << 0$). The inserts show only the polarity of the gate under the gate voltage applied and the grounded back ohmic contact is omitted.



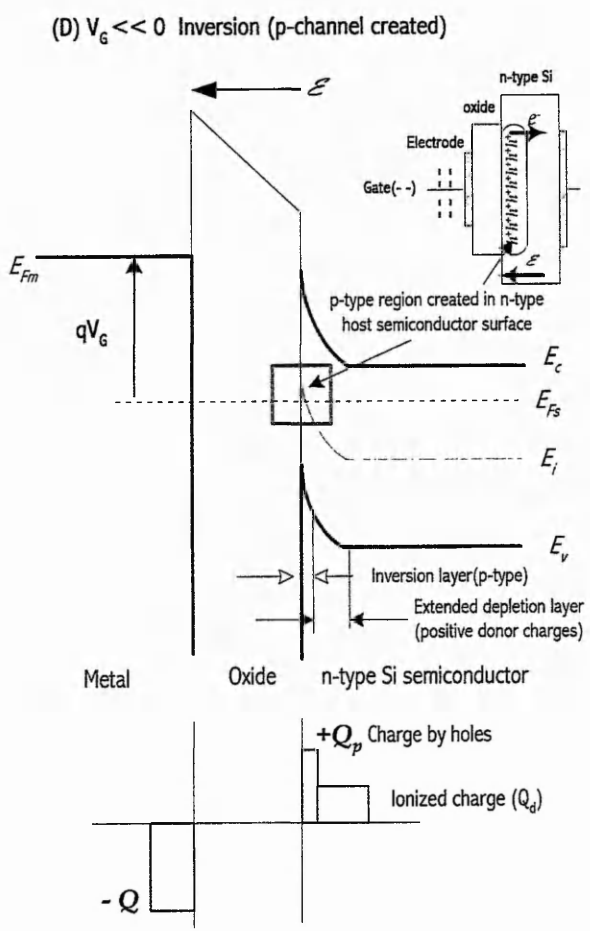


Figure 4-2 (Continued)

When a positive bias is applied with respect to silicon substrate, $V_G > 0$, the positive bias on the gate can attract electrons on the silicon semiconductor surface so that electrons can build up at the surface. As a result, the electron density at the surface will be higher than in the bulk. This is called the *accumulation condition* (which means the electrons on the silicon surface are accumulated). The electron energy in the silicon will be increased in an upward direction due to the applied bias. Thus, the band bends downward at the oxide-semiconductor interface as shown in Figure 5-2(B). At this accumulation condition, the total capacitance (C_{total}) of the MOS capacitor has the maximum capacitance (C_{max}) and the maximum capacitance means the capacitance of oxide (C_{oxide}) by the equation as given in Figure 4-1(b).

When a small negative bias is applied to the gate with respect to the silicon, the electrons at the surface of the silicon can be removed from the surface and then leave behind uncompensated positive donor charges, or ionized donor charges (N_d^+) at the surface. The mobile carriers - electrons - are removed so that this condition is called *depletion*. Therefore, the band bends upward. The intrinsic Fermi level (E_i) comes closer to the thermal equilibrium silicon Fermi level (E_{Fs}). At the thermal equilibrium, the semiconductor Fermi level must be constant throughout the entire device. The value of $E_{Fs} - E_i$ is a good indicator of determining or estimating the type condition of the semiconductor simply because $E_{Fs} - E_i$ must be a positive value in n-type semiconductor from the equations of hole and electron concentration (p or n) in p-n junction basics below:

$$n = n_i e^{(E_{Fs} - E_i)/kT} \quad (E_{Fs} > E_i)$$
$$p = n_i e^{(E_i - E_{Fs})/kT} \quad (E_{Fs} < E_i)$$

Equation 4-1

where n_i is the intrinsic concentration of electrons (cm^{-3}), k Boltzmann constant (1.38066×10^{-23} J/°K, or eV/°K), and T absolute temperature in Kevin (°K).

As the applied bias increases negatively, the width of the depletion layer will be expanded into the silicon. The depletion layer reduces the total capacitance of the MOS capacitor. If the negative bias increases sufficiently to the metal gate ($V_G << 0$), the band bending effect develops further in the upward direction so that the intrinsic Fermi level can cross the Fermi level ($E_i > E_{Fs}$) at the surface as shown in Figure 4-2(D). The sign of the Fermi level difference (E_{Fs}-E_i) shows a negative value, which means at the surface a p-type conducting region is

newly created (it is called p-channel) within the n-type host semiconductor. In other words, the semiconductor acts like a p-type material at the surface in the n-type semiconductor. The minority carriers (holes) attracted to the insulator-semiconductor interface so that the hole concentration becomes greater than electron concentration in n-type bulk region. Thus, the semiconductor surface doping profile is inverted and this is called the *inversion condition*. The total capacitance (C_{inv}) at the surface-inverted condition is the series capacitance of the depletion layer capacitance and the oxide capacitance.

In this inversion condition, a clear criterion is necessary to show evidence whether a true p-type conducting region exists at the semiconductor surface. The best condition for truly strong inversion is that the surface must be strong p-type in concentration like the n-type silicon semiconductor in terms of carrier concentration. $\phi(x)$ is defined as a measured potential relative to the intrinsic Fermi level(E_i) position at any given position, x, so that the potential $\phi(x)$ is defined by $[E_{i(bulk)} - E_i(x)]/q$. Figure 4-3 shows that the potential $\phi_F(x)$ is defined by $[E_F - E_i(x)]/q$ with its consistence with carrier concentration function in Equation 4-1. In fact, $\phi(x)$ is the total band bending in silicon, while $\phi_F(x)$ is a modified surface potential as a supporting parameter from the Fermi leve(E_{Fs}). Thus, ϕ_{Fs} and ϕ_B mean the potential difference from E_{Fs} *to* E_i at the surface($x = 0$) and in the bulk ($x \rightarrow \infty$), respectively, as also shown in Figure 4-3. As it mentioned above, E_i should lie as far above E_{Fs} at the surface as it is below E_{Fs} in the bulk in the strong-inversion condition. This condition occurs when the surface potential ($\phi(x)\,|_{x=0} = \phi_s$) should be equal to two times larger than the bulk potential($\phi(x)\,|_{x\rightarrow\infty} = \phi_B$):

$$|\phi_s(inversion)| = 2\cdot\phi_B = 2\frac{kT}{q}ln\frac{N_d}{n_i}$$ (on-set of strong inversion) **Equation 4-2**[10,11]

The Equation 4-2 can be used as an important indicator of the depletion-inversion transition point. In an n-type semiconductor, the bulk potential, ϕ_B is positive potential (ϕ_B is always positive value in a n-type semiconductor except the inversion condition due to the Fermi level as reference). Therefore, the direction of arrows in Figure 4-3 indicates negative or positive of the potential. It is easy to understand intuitively that a downward direction of the arrow means positive and upward arrows shows negative[11].

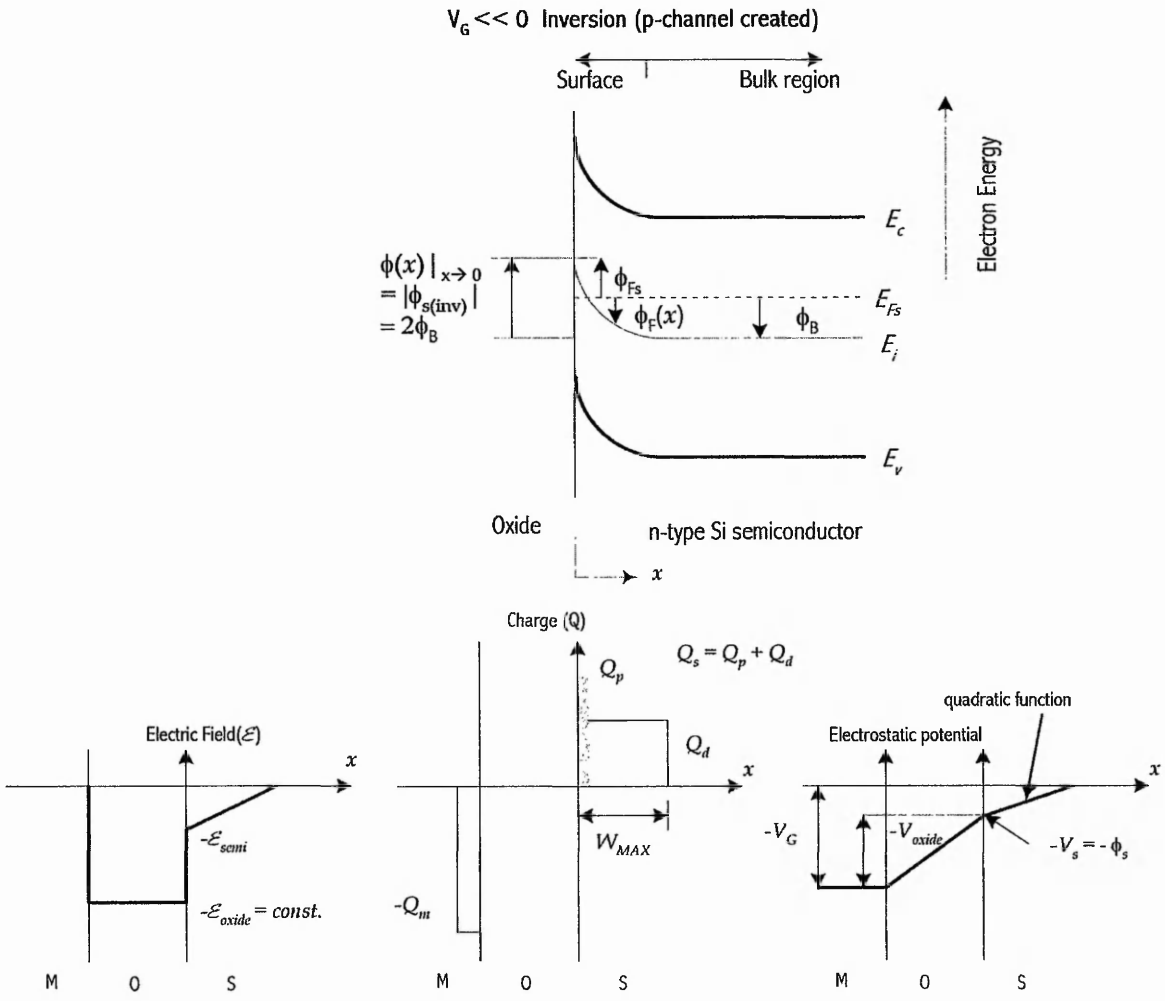


Figure 4-3 For a strong inversion, electric field, charge, and potentials ($\phi(x)$, $\phi_F(x)$,ϕ_s, ϕ_{Fs}, and ϕ_B) in n-type semiconductor. The sign convention of Nicollian E.H. *et al.*(see ref.11) is applied.

When ϕ_{Fs} is greater than ϕ_B ($\phi_{Fs} > 0$, and $\phi_{Fs} > \phi_B$), the surface of the semiconductor is in accumulated condition. By the definition above, the large positive surface potential ($\phi_{Fs} > \phi_B$) directly means that the band bending goes downward. While ϕ_{Fs} is negative, but $|\phi_{Fs}|$ is less than ϕ_B, the semiconductor is in the case of depletion condition until $|\phi_{Fs}|$ is equal to ϕ_B. The total potential difference (or total band bending) between $E_{i(bulk)}$ and E_i will be $|\phi_s| = 2\phi_B$ as shown in the Equation 4-2, which is the intrinsic Fermi level's total rate of change in magnitude from the bulk. ϕ_s is known as the surface potential of the semiconductor when the potential $\phi(x)$ is at $x = 0$. When ϕ_{Fs} (or ϕ_s) is still negative and $|\phi_{Fs}|$ is becoming greater than ϕ_B, the true inversion condition will occur (See Figures 4-2 and 4-3).

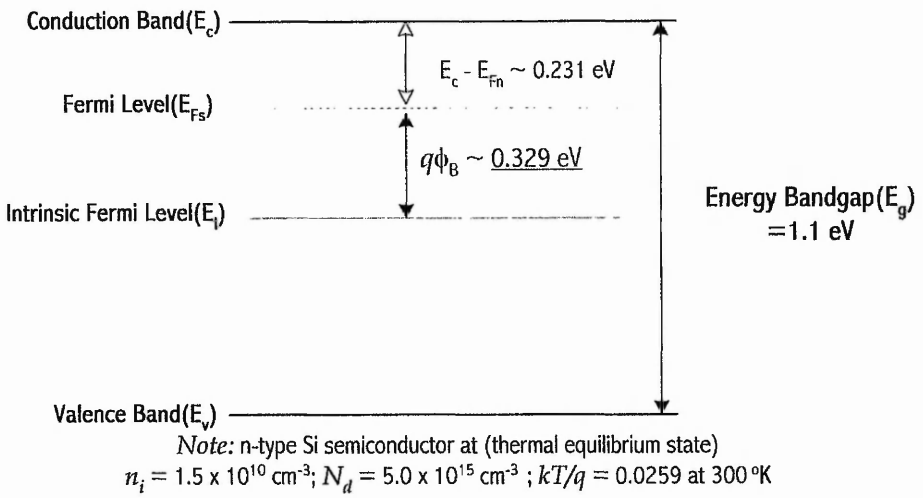


Figure 4-4 The real relationship of the extrinsic Fermi (E_{Fs}) and the intrinsic Fermi(E_i) in *n*-type silicon semiconductor which are used in this study.

ϕ_B is clearly related to the doping profile of the semiconductor by the definition. The calculated bulk potential difference ($\phi_B = E_{Fs}$-$E_{i(bulk)}$) is approximately 0.329 eV for the n-type Si substrates which are used in this experiment. In other words, this extrinsic Fermi level (E_{FS}) is located in higher energy level from the intrinsic Fermi level (E_i) by 0.329 eV. These energy levels are schematically illustrated in Figure 4-4 above.

In depletion condition, one of the important parameters is the depletion width like a *p-n* junction diode. The depletion width is calculated by using the one dimensional Poisson's equation. In this approximation, at a distance x = W, assume that the space charge region (i.e., depletion region) is terminated abruptly. A charge density (ρ) can be written as the equation 4-3:

$$\rho = q(p - n + N_d - N_a) \cong qN_d \quad (0 \le x \le W) \text{ for n-type semiconductor} \quad \textbf{Equation 4-3}$$

where N_a is the acceptor carrier density in the unit of numbers per unit volume (numbers/cm^3), N_d the donor carrier volume density (numbers/cm^3), p the hole concentration (cm^{-3}) and n the electron concentration (cm^{-3}) as the Equation 4-1.

The poisson equation can be employed to obtain the fundamental relationships in the

electrical field, the potential and charge. The one-dimensional poisson equation is expressed as Equation 4-4.

$$\frac{d^2\phi(x)}{dx^2} = -\frac{d\mathcal{E}(x)}{dx} = -\frac{\rho}{\varepsilon_s\kappa_o} = -\frac{qN_d}{\varepsilon_s\kappa_o} (o \le x \le W) \quad \textbf{Equation 4-4}^{\dagger}$$

where ε_s and κ_o are the semiconductor dielectric constants and permittivity of vacuum, respectively.

In order to obtain the electric field distribution within the depletion region, the 2nd term and 4th term from the Equation 4-4 (i.e., Gauss's Law) can be employed and then take the integration with respect to the distance, x, the electrical field ($\mathcal{E}$) is given in Equation 4-5 below after taking the boundary condition, $\mathcal{E} = 0$ at $x = W$.

$$\mathcal{E}(x) = \mathcal{E}_o + \frac{qN_d}{\varepsilon_s\kappa_o}x = -\frac{qN_d}{\varepsilon_s\kappa_o}(W - x) \quad (0 \le x \le W)$$
$$\mathcal{E}(0) = \mathcal{E}_o = -\frac{qN_d}{\varepsilon_s\kappa_o}W \qquad \textbf{Equation 4-5}$$

By the relationship between the electric field and the potential from the Equations 4-4 and 4-5, a second integration with respect to the distance, x gives

$$\phi(x) = -\frac{1}{2}\frac{qN_d}{\varepsilon_s\kappa_o}(W - x)^2 = -\frac{1}{2}\frac{qN_dW^2}{\varepsilon_s\kappa_o}(1 - \frac{x}{W})^2 \quad (0 \le x \le W) \quad \textbf{Equation 4-6}$$

From the boundary conditions, at x =W, the potential has zero value because there is no gradient in the electric field at any position $x \ge W$ (see Equation 4-6). In addition, at $x = 0$, the potential, $\phi(x)$ is equal to the surface potential ($\phi(x)_{x=0} = \phi_s$). Therefore, the surface potential and the depletion region width can be obtained:

$$\phi(x)_{x=0} = \phi(0) = \phi_s = -\frac{1}{2}\frac{qN_d}{\varepsilon_s\kappa_o}W^2 \quad \textbf{Equation 4-7}$$

$$W = \left[2\frac{\varepsilon_s\kappa_o}{qN_d}|\phi_s|\right]^{1/2} \qquad \textbf{Equation 4-8}^{\bullet}$$

† It simply means (i) $\rho = 0 \Leftrightarrow \mathcal{E}(x) = \text{const.} \Leftrightarrow \phi(x) \sim$ linear; (ii) $\rho = \text{const.} \Leftrightarrow \mathcal{E}(x) = \text{linear} \Leftrightarrow \phi(x) \sim$ quadratic (see. Fig. 4-3)

By using the Equation 4-7, the Equation 4-6 can be rewritten as

$$\phi(x) = \phi_s(1 - \frac{x}{W})^2 \qquad \textbf{Equation 4-9}$$

The maximum depletion width (W_{max}) will occur when $|\phi_S| = 2\phi_B$. Simply this condition substitutes into the Equation 4-8, then it gives the maximum depletion width (W_{max}) as the Equation 4-10 below;

$$W_{max} = \left[2\frac{\varepsilon_s \kappa_o}{qN_d}(2\phi_B)\right]^{1/2} = 2\left[\frac{\varepsilon_s \kappa_o kT}{q^2 N_d} ln(\frac{N_d}{n_i})\right]^{1/2} \quad (W = W_{max}) \qquad \textbf{Equation 4-10}$$

In Equation 4-10, the maximum depletion region width (W_{max}), only depends on the impurity concentration (N_d) like a zero-bias depletion region width of a one-sided step junction of the p-n devices when the temperature remains constant. From Equation 4-10, the maximum depletion region width (W_{max}) can be calculated. Thus, W_{max} = 0.42 μm and the surface potential (ϕ_s) is 0.658 (= 2* 0.329) V in practice for the onset of the strong inversion is obtained when the carrier concentration of the Si substrate is $N_d = 5 \times 10^{15}$ charges/cm^3. The depletion width (W) and their corresponding surface potentials (ϕ_s) are illustrated in Figure 4-5.

In Figure 4-5, the extrinsic *Debye length* (L_B) is given with intrinsic state, strong inversion condition and maximum depletion width (W_{max}). The intrinsic *Debye length* (L_D) is defined as a characteristic screening (or shielding) distance over which a charge imbalance is neutralized by majority carriers in plasma♣ physics[12, 13, 14]. Under the flat band condition, the semiconductor can be considered a type of plasma with equal number of ionized impurities and mobile carriers (electrons or holes), in which the plasma is electrically neutral. The *Debye length* can be introduced and has been used as a special length parameter for the band bending inside a semiconductor. The shielding distance or band bending region is of the order of the bulk or extrinsic *Debye length* (L_B), where

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♦ The depletion width means a distance, always a positive value. Thus, the absolute value of the surface potential is applied.

♣ A plasma is in general understood as a highly ionised gas containing an equal number of positive ions and negative electrons.[See Ref. 10]

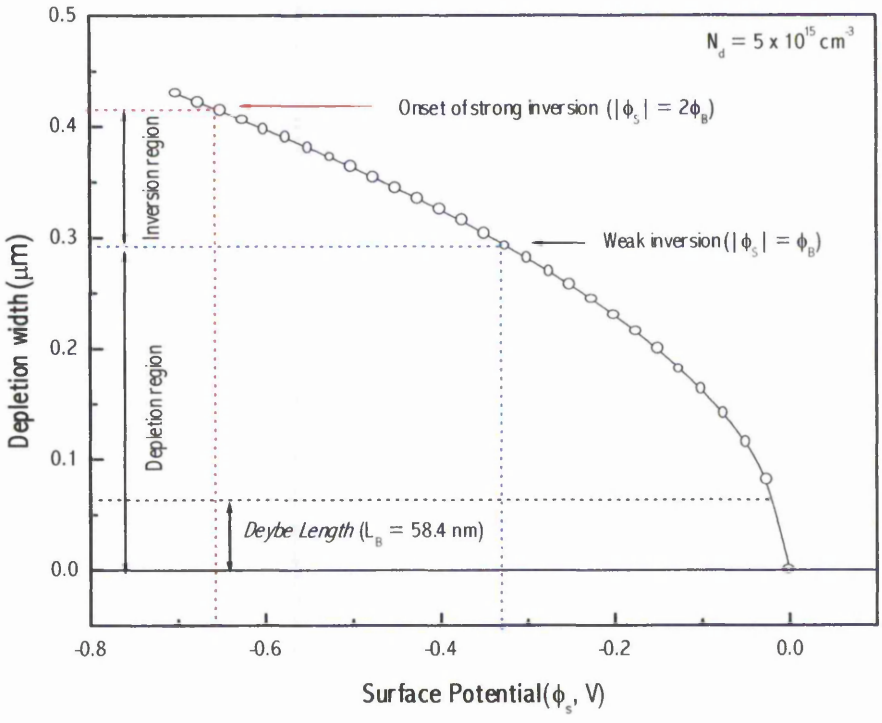

Figure 4-5 The plot of the surface potential (ϕ_S) as a function of the depletion width(W) with three different regions - depletion, weak inversion, and onset of the strong inversion.

$$L_B = \left[\frac{\kappa_o \varepsilon_s kT}{q^2(n_{bulk} + p_{bulk})}\right]^{1/2} = \left[\frac{\kappa_o \varepsilon_s kT}{q^2(N_x)}\right]^{1/2} \quad (N_x = N_d \text{ or } N_a) \quad \textbf{Equation 4-11}$$

The intrinsic *Debye length* is easily obtained from the extrinsic *Debye length* by $n_{bulk} = p_{bulk} = n_i$;

$$L_D = \left[\frac{\kappa_o \varepsilon_s kT}{2q^2 n_i}\right]^{1/2} \quad (n_{bulk} = p_{bulk} = n_i) \quad \textbf{Equation 4-12}^{\ddagger}$$

The MIS capacitor is controllable by two controllers - one internal and one external[15]. The internal controller is the surface potential discussed above and it essentially depends on the properties of the semiconductor such as the type of majority carriers (n or p), and carrier

concentration density. The other one is the gate voltage (i.e., bias). Now the MIS device is subject to the gate bias directly. In addition, it is confirmed that the surface potential can be controlled by the gate voltage in the different surface regions. Therefore, the equations related to the gate voltage and the surface potential should be established.

By Kirchhoff's voltage law, across the oxide layer and the semiconductor there are voltage drops in each layer. The relationship can be expressed as followed:

$$V_G = \Delta\phi_{oxide} + \Delta\phi_{semi} \quad (\Delta \text{ means a potential drop}) \quad \textbf{Equation 4-13}$$

In the bulk region of the semiconductor, the potential is zero ($\phi(x)|_{x\to\infty} = 0$). In addition, in an ideal insulator there are no mobile carriers or charges which means the electric field inside of the insulator (oxide layer) must remain constant by the Gauss's law (See Equation 4-4);

$$\frac{d\mathcal{E}_{oxide}}{dx} = 0 \quad (\leftarrow \rho = 0) \qquad \textbf{Equation 4-14}$$

By taking the integration and then the Equation 4-5 is applied. Therefore, the potential within the oxide (insulator) layer is

$$\Delta\phi_{oxide} = \int_{t_o}^{o} \mathcal{E}(x)_{oxide} dx = t_o \cdot \mathcal{E}_{oxide} \qquad \textbf{Equation 4-15}$$

where t_o is the thickness of the oxide layer. Usually the semiconductor-oxide interface is the reference point as an origin (x=0).

The boundary condition of the electric field normal to the interface between two different materials should be satisfied:

$$(\boldsymbol{D}_{semi} - \boldsymbol{D}_{oxide})|_{interface} = Q_{interface} \qquad \textbf{Equation 4-16}$$

‡ For reference, L_D = 23.8 μm and it is 407 times larger than the extrinsic Debye length, L_B = 0.0584 μm (=58.4 nm)

where $D_x = \kappa_o \varepsilon_x \mathcal{E}$ ($_{x=oxide}$, or $_{semi}$) is the dielectric displacement and $Q_{interface}$ is the charge per unit area at the interface between the oxide and the semiconductor. In the ideal case, the charge at the interface is zero ($Q = 0$). Therefore,

$$\mathcal{E}_{oxide} = \frac{\varepsilon_s}{\varepsilon_{ox}} \mathcal{E}_{semi} \quad [D_{semi}|_{x=0} = D_{oxide} \quad (\because Q_{interface} = 0)] \quad \textbf{Equation 4-17}$$

where ε_{ox} and ε_s are the dielectric constants of the oxide layer and the semiconductor, respectively.

As a result, there is a discontinuity in the electric field($\mathcal{E}$) at the interface[16] from Equation 4-17. The potential of the oxide layer can have an expression as a function of the electric field of semiconductor in Equation 4-18 below;

$$\phi_{oxide} = t_o \cdot \mathcal{E}_{oxide} = t_o \frac{\varepsilon_s}{\varepsilon_{ox}} \mathcal{E}_{semi} \qquad \textbf{Equation 4-18}$$

Finally, the gate voltage (V_G) can be rewritten as the function of the potential and electric field of the semiconductor. Therefore, the gate bias will be

$$V_G = \phi_s + t_o \frac{\varepsilon_s}{\varepsilon_{ox}} \mathcal{E}_{semi} \qquad \textbf{Equation 4-19}$$

The electric field of the semiconductor as a function of the semiconductor potential is easily derived from two equations 4-5 and 4-8. Thus, the complete equation of the relationship between the gate bias and the semiconductor potential is obtained as Equation 4-20.

$$V_G = |\phi_s| + t_o \frac{\varepsilon_s}{\varepsilon_{ox}} \left[2 \frac{qN_d}{\varepsilon_s \kappa_o} |\phi_s| \right]^{1/2} \quad (0 \le |\phi_s| \le 2\phi_B) \qquad \textbf{Equation 4-20}$$

4.2 Properties of Y_2O_3 thin films

4.2.1 Growth conditions and structure

The basic growth conditions for yttrium oxide thin film were optimized previously by our research team at NTU and the optimized growth parameters [17, 18] were applied in this study. More details can be obtained in the references. Even if the growth parameters were mentioned in experimental chapter in detail, the parameters are discussed again briefly. The main chamber base pressure before sputtering was typically at 2.0×10^{-7} Torr, and the chamber was pre-baked in vacuum at 700 °C in order to remove moisture and organic impurities on the surface of the substrate. Y_2O_3 thin films were deposited on n-type Si substrates at the pressure of 3 mTorr. The substrate temperature during the Y_2O_3 growth was sustained at 190 °C. After growth, a post-annealing process was generally performed at 400 °C in vacuum condition of 2.0×10^{-7} Torr pressure for 1 hour.

The thickness of the deposited yttrium oxide thin films was approximately 300 nm. The thin film was monitored and measured by laser interferometric system attached to the chamber during the deposition. Other thickness profilers - stylus (Vecco 6M) and optical (Filmetrics F20) methods - were performed after deposition, respectively.

The structure and crystallinity of the deposited yttrium oxide thin films were analyzed by X-ray diffraction (XRD). Figure 4-6 shows the XRD pattern of yttrium oxide thin film using a Cr X-ray source with 0.22897 nm wavelength. From the XRD pattern, the thermal-annealed yttrium oxide thin film showed a cubic structure with a (222) plane preference at 43.23°(2θ), which was confirmed by ICDD PDF catalogue(#25-1200i).

Other weak peaks are indexed and there are three unidentified peaks at 14.48°, 18.30° and 39.29°, respectively. The peak at 39.29° seems to result from yttrium silicate (Y-O-Si system) at the interface region between Y_2O_3 and Si substrate. It needs further study to identify the origin of the peaks. However, from the most significant peak, an average crystal size (or particle size, t) can be estimated by the Scherrer formula[19,20,21] as below:

$$t = \frac{K \cdot \lambda}{B_{FWHM}(2\theta) \cdot \cos(\theta_B)} \qquad \textbf{Equation 4-21}$$

where K is a shape factor and normally close to unity, but K= 0.9 or 0.94 is mainly used, λ means the wavelength of X-ray used, $B_{FWHM}(2\theta)$ (the breadth of the beam) is simply the full width of the diffraction peak at half maximum intensity, measured in radians, and θ_B is the angle of the maximum peak.

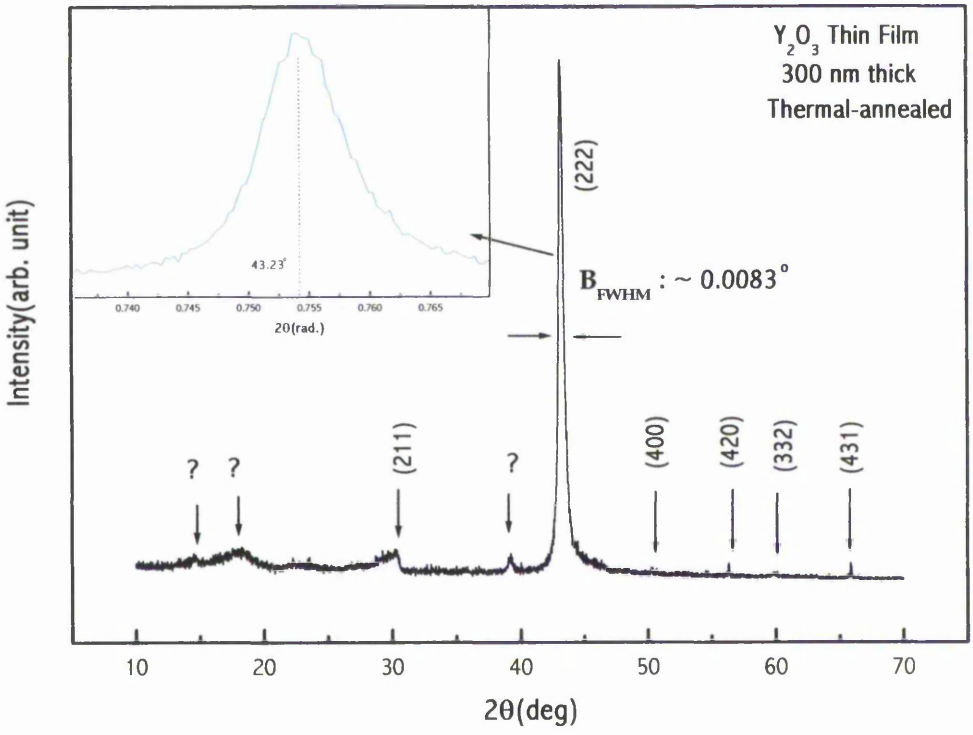

Figure 4-6 The X-ray Diffraction pattern of yttrium oxide thin film: it shows (222) plane preference and other relevant peaks. An inset shows enlarged (222) plane peak in radians.

According to the Equation 4-21, the average crystal size of the yttrium oxide thin film is approximately 26.7 nm (K= 0.9 is used). At the angle of the maximum peak, corresponding $d_{(222)}$-spacing is 0.306 nm. The value of 26.7 nm can be interpreted as the average crystal dimension perpendicular to the reflecting planes so that the particle of yttrium oxide thin film indicates there are more than 87 layers (planes) in phase. Other reported average crystal size

had a range of 15 to 20 nm, but it shows still good agreement under similar growth process conditions because the broadening of detected peaks can be attributed to the experimental setup and instrumentation. In addition, the larger crystal size means higher peak intensity and narrower peak shape.

Y_2O_3 crystallite structure stability and plane orientation are improved with a high thermal annealing temperature. The calculated *d*-spacing of a non-annealed sample is 0.462 nm and the other annealed samples at higher temperature more than 400 °C shows convergence to the standard *d*-spacing reference value of 0.306 nm. The reduced XRD patterns of thermal- and non-annealed Y_2O_3 thin film with 300 nm thick is shown in Figure 4-7. The non-annealed sample has approximately 6.2 nm crystal size (by Equation 4-1) and at the same time it shows a very broad peak as is expected and the peak-shifting effect by annealing temperature. Often, this peak-shifting phenomenon by post-annealing treatment is one of the typical properties when thin films are grown[29]. More details of Y_2O_3 thin film for post-annealing effect are explained in other reference[29]. Thus, post-thermal annealing treatment is demonstrated to improve the crystallinity of yttrium oxide thin films with annealing temperature.

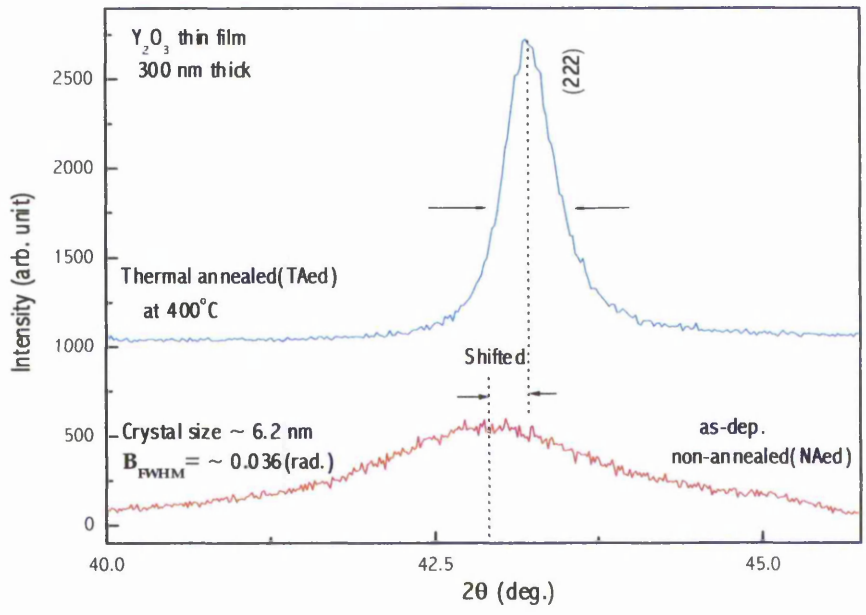

Figure 4-7 Reduced XRD patterns of thermal (TAed)- and non-annealed (NAed) 300 nm thick Y_2O_3 thin film with respect to post-annealing treatment

4.2.2 Capacitance - Voltage Characteristics

In order to evaluate dielectric properties, the capacitance-voltage(*C-V*) measurement is generally an essential technique in analysis. Much important information can be obtained from *C-V* analysis: the various capacitances of accumulation, depletion and inversion, dielectric constant, flatband voltage and others. Yttrium oxide thin films deposited on n-type silicon substrate shows typical capacitance curve as a function of applied gate voltage: accumulation, depletion and inversion regions are identified clearly in *C-V* measurements under a high frequency of 1 MHz. In addition, the effective charges in the oxide depend on the gate voltage history and, as a result, *C-V* curves with hysteresis are observed. The average capacitance and dielectric loss tangent (i.e., tan δ) of yttrium oxide thin films with a 1mm dia. Al electrode are shown in Figure 4-8 and 4-9, respectively.

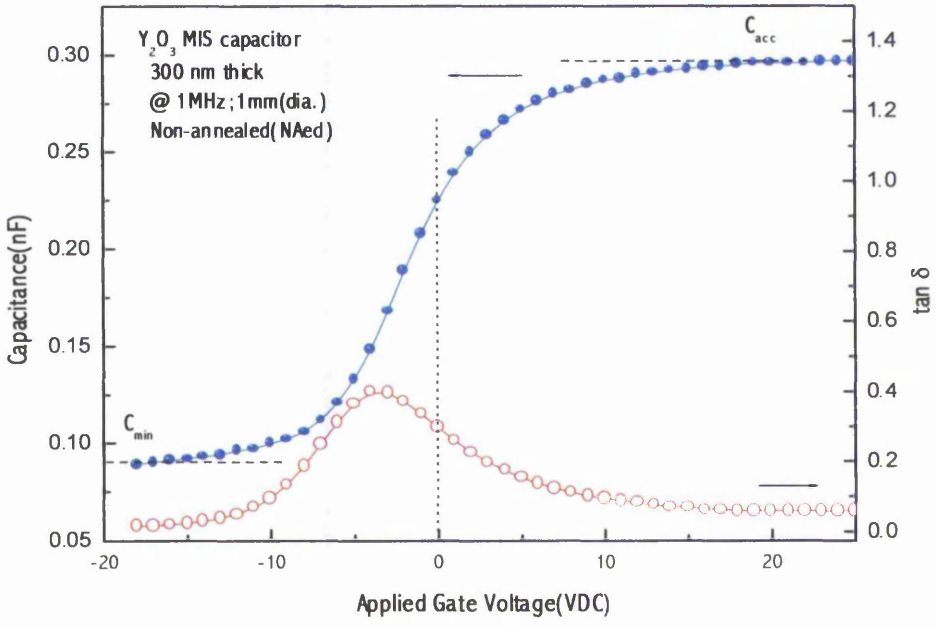

Figure 4-8 Dielectric properties of yttrium oxide with applied voltage by *C-V* characterization: Non-annealed (NAed) 300 nm thick Y_2O_3 thin film at 1 MHz (average capacitanace-loss tangent)

Using *C-V* characterisation, the maximum capacitance of Y_2O_3 thin film under accumulation condition was 0.3 nF (avg.) in Figure 4-8 and 4-9. Thus, the non-annealed Y_2O_3 thin film has

average dielectric constant (relative permittivity, ε_r) of 12.94 at the same condition. This value seems to be in good agreement because other reported dielectric constant of Y_2O_3 thin films has the range of 11.9 ~ 18 according to growth methods[3,22, 23, 24, 25,]. In addition, the dielectric constant of yttrium oxide material is known as being constant (approx. 10) at the range of frequency of 20 ~ 120 kHz[26].

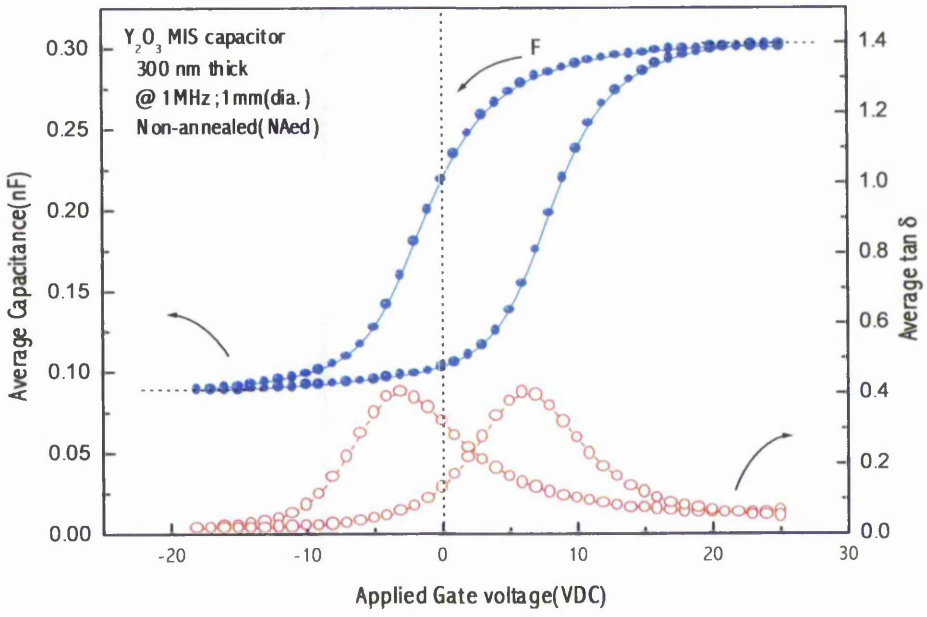

Figure 4-9 Dielectric hysteresis curve of non-annealed 300 nm thick Y_2O_3 thin film

The characteristic *C-V* curve of post-annealed Y_2O_3 thin films is shown in Figure 4-10. By the thermal annealing process, capacitance is slightly reduced about 5%, but in the case of dielectric loss, the annealed samples are improved dramatically. The dielectric loss reduced down by 50%. In addition to that, a dielectric hysteresis effect is relatively small, which means mobile charges at the interfaces (metal-oxide and/or oxide-semiconductor) and in the bulk possibly are reduced by the annealing process. Therefore, the post-annealing process has been shown to improve crystallinity of yttrium oxide thin films (by XRD analysis) and reduce both of dielectric loss (i.e., dissipation or loss factor, *D*) and hysteresis effect. The dielectric constant of post-annealed Y_2O_3 thin film MIS capacitors is calculated as of 12.3. Although dielectric

constant and capacitance of thermal annealed thin films are lower than those of non-annealed thin films as a trade-off, the differences are not significant, but negligible. Horng, R.H.[27] et al., reported the similar effect in the dielectric constant of yttrium oxide thin films after having a rapid thermal annealing process. However, higher dielectric constants of 16 ~ 19 has been reported[3,22,24]. As mentioned above, there is clearly the feasibility to obtain more improved yttrium oxide thin films in terms of structure, dissipation and hysteresis properties.

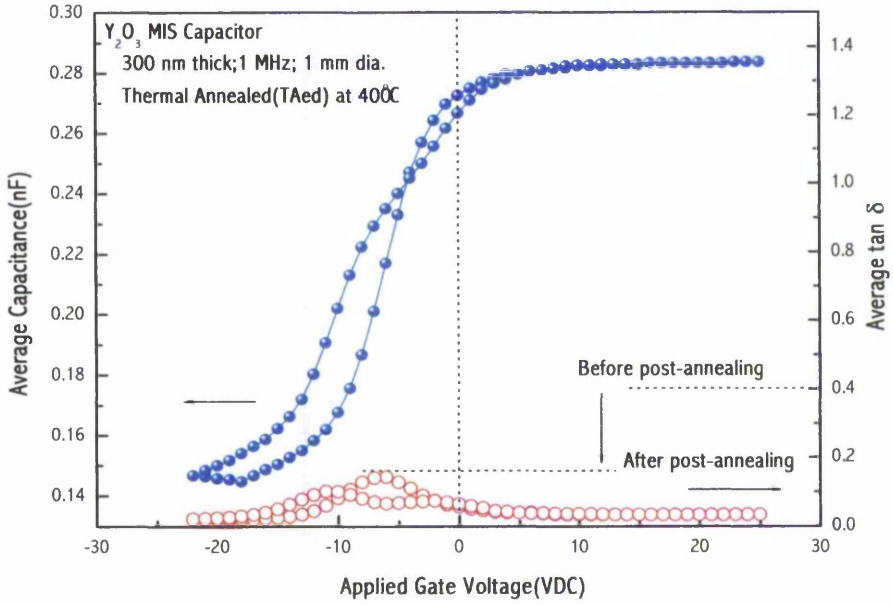

Figure 4-10 Characteristic *C-V* curve of post-thermal annealed Y_2O_3 thin films

4.2.3. Current - Voltage Characteristics

Leakage current and leakage current density

In order to obtain a leakage current (or density) and breakdown field of Y_2O_3 thin films, current (or density)-voltage (*I-V* or *J-E*) measurements were performed. Average leakage currents as a function of the applied gate voltage (V_G) are plotted, as shown in Figure 4-11. These leakage currents did exhibit a large difference between post- and non-annealed Y_2O_3 MIS capacitor devices. In particular, under the lower applied electric field (< 1 MV/cm), the current density-electric field (*J-E*) for both devices has a significantly different trend. First of all, the thermal-annealed devices maintained lower leakage current ($3.22 \sim 6.06 \times 10^{-8}$ A/cm^2) in average than that of the non-annealed ones ($1.22 \sim 3.53 \times 10^{-7}$ A/cm^2) by the order of 1.

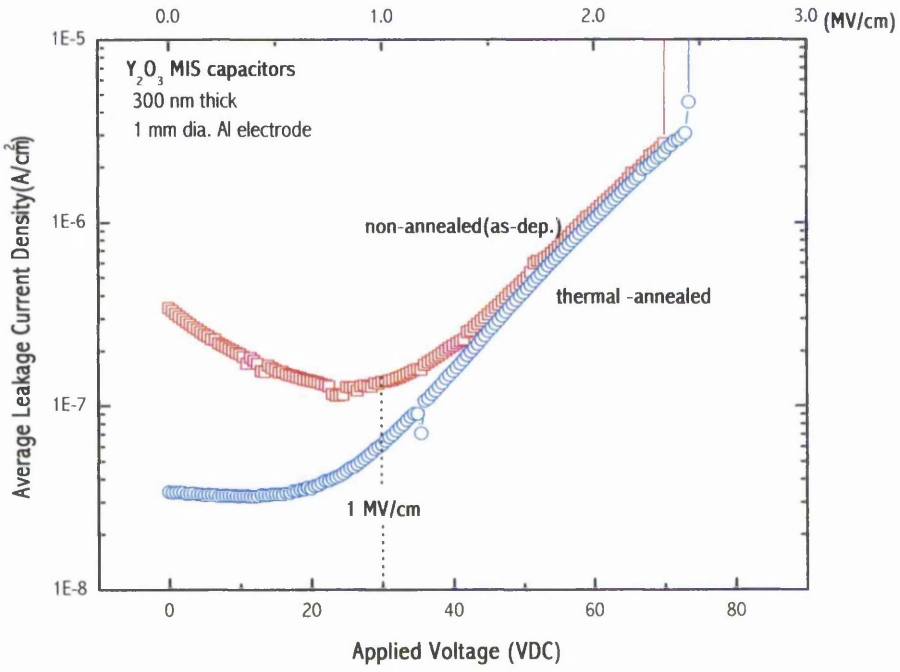

Figure 4-11 *I-V* characteristics of Al/Y_2O_3/Si MIS capacitors with 300 nm thick Y_2O_3 thin film.

It is believed that the non-annealed yttrium oxide has relatively many shallow traps at the interface or in the bulk of the oxide and that these traps easily contribute to this higher leakage current after a small field is applied. However, the average leakage current (or density) shows

a "negative resistance-like" characteristic within this lower field region. For this negative resistance-like phenomenon, it is not clear, but it is possible to think it about with the same hypothesis of the shallow traps, which exist mainly at the interfaces and in the vicinity. At this moment, it may be reasonable to understand these shallow traps or voids results from oxygen deficiency when it grows. The oxygen deficiency in yttrium oxide on silicon was reported by Hunter, M.E.[28]. As it mentioned from the XRD patterns, silicates (i.e., Y-O-Si)§ are possibly formed at the interface so that this interfacial layer accelerates oxygen deficiency (or O_2 vacancy) in yttrium oxide films and then finally, it can causes a large amount of traps at the interface. Most of the shallow traps can interact easily with the lower field and then a number of remaining shallow traps in the vicinity decrease as the applied field increases. Thus, the leakage current is decreasing with respect to the applied field under the lower field region (~ 1 MV/cm).

From the *C-V* characteristics in the previous section, the thermal-annealed devices showed improvement in hysteresis and dielectric loss due to removal of traps at the interface or vicinity effectively. This hypothesis can also explain the "negative resistance-like" phenomenon on *I-V* characterisation due to the very shallow traps at the vicinity of the interface. Meanwhile, the leakage current of the thermal-annealed device was constant and well maintained up to 1 MV/cm. In the higher field region, the two devices have linear characteristics with the same slope. Hence, it is confirmed that the thermal annealing process can be a critical factor in yttrium oxide thin film deposition to remove the shallow traps so that the lower leakage current and improved stability of yttrium oxide thin film can be achieved, in particular, in the lower field range. As a matter of fact, the negative-resistance phenomenon was not shown within some of test devices. At the same time, irregularities like the negative-resistance phenomenon can be noticed on the thermal-annealed devices, but the degree of this phenomenon was a quite small.

Breakdown field

For an average breakdown field (or breakdown strength), the devices showed almost the same degree in their magnitude (see Figure 4-11). Non-annealed devices started to breakdown at 2.3 MV/cm, but the post-annealed devices maintained integrity up to the limit of the measurement system. For the thermal-annealed devices, most of the test device started to

§ Silicate is a generic term for a compound that contains silicon, oxygen, and one or more metals, and it may contain hydrogen. [From Dictionary

breakdown at approximately 3 MV/cm (~ 90 V). This improved breakdown strength can be considered an important benefit from the post-thermal annealing treatment. Some devices showed a higher breakdown strength of more than 3.3 MV/cm (thermal annealed), but the lowest breakdown strength was approximately 2.29 MV/cm (non-annealed). Compared to Sethu, M[29], these breakdown fields of yttrium oxide thin film are smaller.

According to types of breakdown, there are two different modes: self-healing and propagating modes. Y_2O_3 dielectrics are known for having self-healing properties.[30] This self-healing mode breakdown inherently can isolate the localized breakdown and prevent catastrophic breakdown such as a whole device failure. Thus, this kind of dielectric thin films can provide improved device reliability in microelectronics and TFEL devices. Some yttrium oxide MIS capacitors showed rapid increase in leakage current with the applied gate voltage before the upper limit gate voltage (maximum DC voltage is 100 V on the system), but the leakage current at the given field (or voltage) was as low as a few 10^{-6} A. Actually, this is not a hard breakdown, but it does indicate possibly a soft breakdown due to the self-healing properties of yttrium oxide. The breakdown of dielectric materials is often defined by the leakage current of larger than ~ 10^{-2} A on a device under test (DUT). Thus, if considering this as a soft breakdown, the breakdown field might be larger.

Taking the soft breakdown into account in current-voltage analysis, the post-annealed MIS device showed 3.1 MV/cm (~ 93 V) breakdown strength (E_{BD}) and 2.65 μA/cm² leakage current density on average while the non-annealed device had 2.5 MV/cm(~ 74 V) of breakdown strength and 4.61 μA/cm² of leakage current density, respectively. As discussed previously, these breakdown fields and leakage currents (or current densities) are result from improvement of post-annealed Y_2O_3 thin films. Some results of breakdown strength and leakage current density of MIS capacitor with Y_2O_3 layer as a function of applied gate voltage are plotted in Figure 4-12, including the average values. Standard deviations (σ) for each parameter - breakdown voltage, breakdown field and leakage current density from Figure 4-12 are given in Table 4-1.

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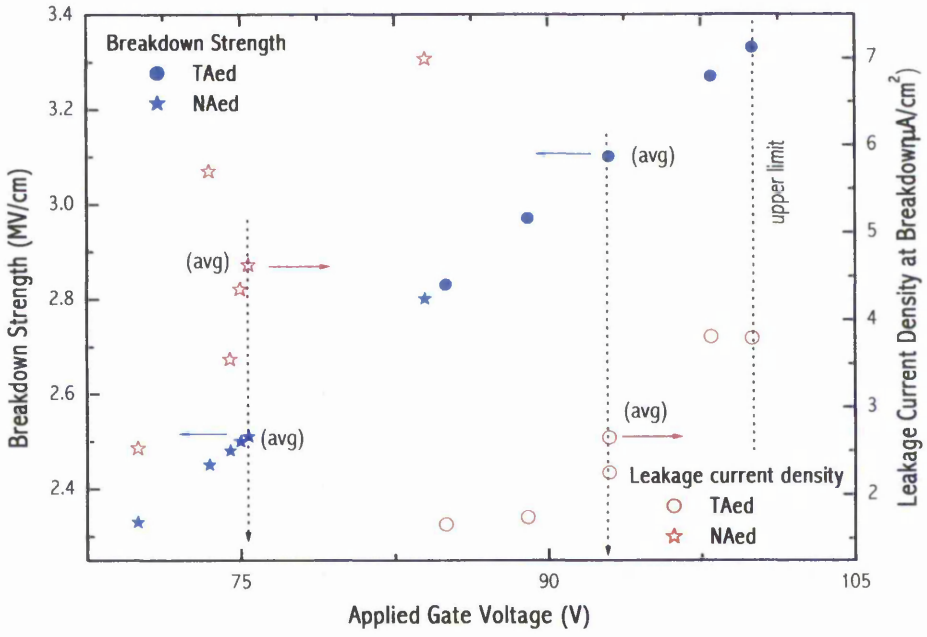


Figure 4-12 Breakdown strength(E_{BD}) and leakage current density as a function of applied voltage: (avg) means average value in breakdown strength and leakage current density, respectively. Standard deviations(σ) for breakdown voltage(V_{BD}), breakdown field(E_{BD}), leakage current density(J) are 6.2(5.2) V, 0.21(0.74) MV/cm, 1.1 (1.8) μA/cm², respectively. (numbers in parenthesis are the non-annealed devices)

Table 4-1 Standard deviations (σ) for breakdown voltage, field, and leakage current from Figure 4-12

		V_{BD}(V)	E_{BD}(MV/cm)	$I_{leakage}$(μA/cm²)
Standard deviation(σ)	TAed	6.2	0.21	1.1
	NAed	5.2	0.71	1.8

Standard deviation: $\sigma \equiv \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \bar{x})^2}$ (x is a mean value; N, total number of data)

Often, E_{BD} and ε_r are essential characteristic parameters of an insulating material for the dielectrics of TFEL devices so that the product (E_{BD} x ε_r ε_o) is used as a figure of merit (FOM), known as the charge storage capacity (CSC) and can be a very important indicator in selecting suitable dielectric material for ACTFEL devices. Therefore, the calculated charge storage

capacity exhibits values of over 3.81μC/cm², which is satisfied with the one of requirements: the charge storage capacity should be at least three times larger than that of the phosphor layer[31,32] for selecting potential dielectric materials in ACTFEL devices. Generally, a ZnS-based phosphor has the charge storage capacity of approximately 1 μC/cm².[29]

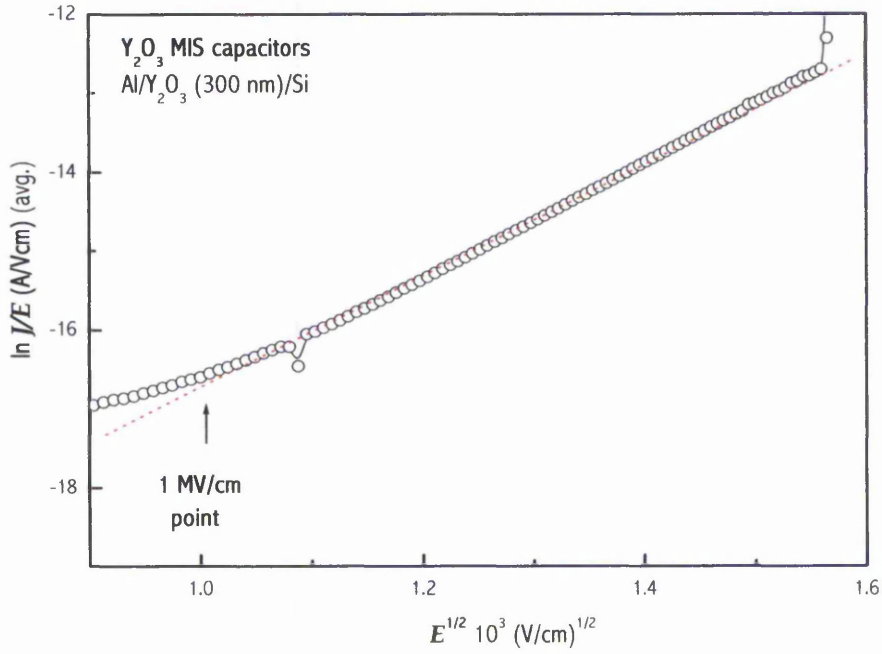


Figure 4-13 Conduction mechanism characteristics by Poole-Frenkel plot (ln (J/E) vs $\sqrt{E}$) in the high electric field region (> 1MV/cm)

Conduction Mechanism

A conduction mechanism in an insulating thin film device is a very important issue. The conduction mechanism can be identified from the current-voltage (***J-E***) characterisation. From Figure 4-11, at lower electric field, it is difficult to determine which mechanism is dominating, in particular, on the non-annealed devices and the thermal annealed device. As mentioned earlier, reduction of the shallow traps at lower fields is possibly done by carrier hopping between traps. In the region of high field (> 1 MV/cm) the dominating conduction mechanism is Poole-Frenkel emission because the slope of the current (*J* vs *E*) shows well defined

linearity[33]. Poole-Frenkel(P-F) conduction is a field-enhanced thermal emission and it was known as a dominating mechanism in the high field condition.[34] Regardless of annealing process, the carrier conduction mechanism in high electric field is based on Poole-Frenkel emission according to the linearity of ln(*J/E*) versus $\sqrt{E}$ plot[35] shown in Figure 4-13. In this case, the electronic conduction is limited by the bulk of the insulator, not by injection form the electrodes[35]. The Pool-Frenkel conduction mechanism of yttrium oxide MIS capacitor is in good agreement with other result[3].

From Figure 4-13, the linearity of the curve shows that the conduction mechanism in the high field region is Poole-Frenkel(P-F) emission. The dielectric constant can be obtained from the slope of J-E curve. The Poole-Frenkel emission equation is known as

$$J \sim E\exp\left[\frac{-q(\phi_B - \sqrt{(qE/\pi\varepsilon_o\varepsilon_i)})}{kT}\right] = E\exp\left[\frac{-q(\phi_B - \beta_{PF}\sqrt{E})}{kT}\right] \qquad \textbf{Equation 4-22}^{[34,35]}$$

where, ϕ_B = barrier height, E = electric field, ε_i = insulator dynamic permittivity, and $\beta_{PF} = \sqrt{\frac{q}{\pi\varepsilon_o\varepsilon_i}} (= 7.6\times10^{-4}/\sqrt{\varepsilon_i})$. According to Equation 4-22, the slope of ln(*J/E*) versus E plot can be β_{PF}/k_BT **. The measured slope of the ln(*J/E*) versus $\sqrt{E}$ plot is 6.25 × 10^{-3} from Figure 4-13 and then the obtained dielectric constant of yttrium oxide is approximately 5.51. Meanwhile, the calculated slope is 8.37 × 10^{-3} from β_{PF}/k_BT (for thin insulator) when the dielectric constant of yttrium oxide (ε_{oxide} =12.3) obtained from capacitance-voltage characterisation in the previous section is applied. The value of dielectric constant of yttrium oxide shows a large difference between the experimental and the equation.

The energy difference between conduction band (E_c) and Fermi level (E_F) depends on the properties of the bulk insulator when the insulator is thick. In the bulk-limited current, the current is limited by a bulk effect, which means it depends on the characteristics of the bulk

** $k_B = k/q = 8.619 \times 10^{-5}\ eV\ K^{-1}$ (Boltzmann constant)

insulator. In fact, according to Hesto, P[35] $\beta_{PF}/2k_BT$ is applied for the thick insulator even though he did not clearly define the criteria of thicker films. Regardless of existence of traps in the insulator, the concentration of free electrons in the thick insulator has a relationship as $n \propto N^{1/2} \exp[E_T/2k_BT]$ †† in the thick insulator. As a result, the current ($\ln(J/E)$) varies linearly with the field ($\sqrt{E}$) in all cases with a different slope according to thickness of the insulator. In addition, the conduction mechanism at the metal-insulator interface shows a strong dependence on the concentration of the carriers in the insulator. In particular, an intermediate carrier concentration is needed for the field-enhanced thermoionic emission[12]. The P-F equation is analogous to that of the Schottky barrier but with a barrier lowering twice as large due to the fact that the variations of the potential energy of an electron in a coulombic field is four times larger than those due to an image force effect. [35]

The value of the slope for the thick insulator is approximately 4.18×10^{-3}. There are still differences between measured and calculated slopes, but it shows possibility of insulator-thickness dependence in Poole-Frenkel emission. As mentioned above, relatively the large deviation seems to come from a low contributable carrier concentration within yttrium oxide thin film layer. However, at this moment, it is not clear for the major effect of the deviation between the slope of the plot (J-E) and the dielectric constant of yttrium oxide even though the plot shows a typical linearity of the Pool-Frenkel emission characteristics. Thus it needs to undertake a further study to investigate this matter.

†† $N^{1/2} = (N_C N_D)^{1/2}$ for insulator without traps or $(N_t N_D)^{1/2}$ for insulator with trap (N_x means concentration of donor($_D$) and trapped electrons($_t$). N_C is equivalent density of state in the conduction band); $E_T = (E_t - E_C)$ for insulator without traps or $2E_C + E_D - E_t$ for insulator with traps. E_C (energy of conduction band), E_D(energy level of donor), and E_t(energy level of a trap). [ref. 35]

4.3 Summary and Conclusions

The electric and dielectric properties of yttrium oxide thin film have been discussed in this chapter. These properties were investigated by XRD, *C-V* and *I-V* characterisations. Yttrium oxide thin film deposited on silicon for this study had (222) orientation (at 43.2°) and a cubic structure.

In order to obtain high quality yttrium oxide thin films for TFEL and other microelectronic applications, the post-annealing process was a critical point for improving dielectric hysteresis and dielectric loss. From *C-V* measurement, the dielectric constant was 12.3 and the dielectric loss was as low as 0.2. At the same time, that process improved better current-voltage characteristics. Thus, the higher breakdown field (3.1 MV/cm on average) and the lower leakage current (~ 2.65 $\mu A/cm^2$) can be achieved.

Carrier conduction mechanism in yttrium oxide thin films was Poole-Frenkel emission in the high field (> 1MV/cm). The P-F plot ($\ln(J/E)$ versus $\sqrt{E}$) showed linearity in the high field regime, which supports that the dominating conduction in the insulating layer is a Poole-Frenkel mechanism. However, there are some deviations between measure values and calculated ones, thus a further study is needed.

REFERENCES

[1] Rastogi, A.C. and Sharma, R.N. Structural and electrical characteristics of metal-insulator-semiconductor diodes based on Y_2O_3 dielectric thin films on silicon, Journal of Applied Physics, Vol. 71 No. 10, p. 5041, 1992

[2] Onisawa, Ken-ichi, et al., Dielectric properties of rf-sputtered Y_2O_3 thin films, Journal of Applied Physics, Vol. 68 No. 2, p. 791, 1990

[3] Nalwa, Hari Singh (ed.) Ferroelectric and dielectric thin films, (from Handbook of Thin Film Materials, Vol.3), Ch 1 (by Jospeph Ya-min Lee and Benjamin Chinming Lai), Academic Press, 2002

[4] Minami, Tadatsugu, et al., Mn-activated Y2O3-GeO2 Phosphor for Thin-Film Electroluminescent Devices, Japanese Journal of Applied Physics, Vol. 40, Part 2(8B), p. L864, 2001

[5] Lorenzelli, V.(ed.) A Special Issue to devoted New Luminescent Materials, Materials Chemistry and Physics, Vol. 16, No. 3-4, 1987, Elsevier Sequoia

[6] Shionoya, Shigeo, and Yen, William M.(Eds.) Phosphor Handbook (Part Three: Practical Phosphors) p.315, CRC Press

[7] Wilson, J. and Hawkes, J.F.B. Optoelectronics: An Introduction 2nd Ed. Chapter 5 and 6, Prentice-Hall 1989

[8] Agilent Technologies (HP), Agilent Technolgies Impedance Measurement Handbook, 2003

[9] Keithley Application Note 2239, Gate Dielectric Capacitance-Voltage Characterisation Using the Model 4200 Semiconductor Characterisation System

[10] Pierret, Robert F. *Semiconductor Fundamentals, 2nd Ed.* (Modular Series on Solid State Devices Vol. I) ch. 2 Addison-Wesley, 1989

[11] Nicollian, E.H. and Brews, J.R. *MOS(Metal Oxide Semiconductor) Physics and Technology*, ch. 2, John Wiley & Sons, 1982

[12] Schroder, Dieter K. *Semiconductor Material and Device Characterization, 2nd Ed.* p. 68, John Wiley and Sons, 1998

[13] Pierret, Robert F. *Field Effect Devices 2nd Ed.* (Modular Series on Solid State Devices Vol. IV), Addison-Wesley, 1990

[14] Ichimaru, S. *Plasma Physics - An Introduction to Statistical Physics of Charged Particles*, ch. 1-2, Addison-Wesley, 1986

[15] Neamen, Donald A. *Semiconductor Physics and Devices 3rd Ed.- Basic principles*, ch. 11, McGraw-Hill, 2003

[16] Warner, R.M. Jr. and Grung, B. L., *MOSFET - Theory and Design*, ch. 2-3, Oxford University Press, 1999

[17] Liew, S-C, ***PhD Thesis***, Nottingham Trent University, UK 2004

[18] Koutsogeorgis, D. K., ***PhD Thesis***, Nottingham Trent University, UK, 2004

[19] Cullity, B.D. *Elements of X-ray diffraction, 2nd Ed.* Addison-Wesley

[20] Hammond, C. *The basics of crystallography and diffraction 2nd ed.* Oxford University Press, 2001.

[21] Warren, B.E. *X-ray diffraction* Dover Publications, 1990.

[22] Cranton, W.M. et al., Growth and dielectric characterization of yttrium oxide thin films deposited on Si by r.f.-magnetron sputtering, Thin Solid Films, Vol. 226, pp.156-160, 1993

[23] Kalkur, T.S. et al., Yttrium oxide based Metal-Insulator-Semiconductor Structures on Silicon, Thin Solid Films, Vol. 170, pp. 185-189, 1989

[24] Manchanda, L. and Gurvitch, M. Yttrium oxide/Silicon Dioxide: A New Dielectric Structure for VLSI/ULSI Circuits, IEEE Electron Device Letters, Vol. 9 No. 4, 1988

[25] Araiza, J. J. et al., Structural, optical, and electrical characteristics of yttrium oxide films deposited by laser ablation, Journal of Vacuum Science and Technology, A16, No. 6, pp. 3305-3310, 1998

[26] Basak, D. and Sen, S.K. Electrical, dielectric, and optical properties of M/Y^2O^3/M devices, Thin Solid Films, Vol. 254, pp. 181-186, 1995

[27] Horng, R. H. et al., Effect of rapid thermal process on structural and electrical characteristics of Y2O3 thin films by r.f.-magnetron sputtering, Thin Solid Films, Vol. 289, pp. 234-237, 1996

[28] Hunter, M.E. Epitaxial Y_2O_3 films grown on Si(111) by pulsed-laser ablation, Applied Physics Letters, Vol. 76, No. 14, p.1935, 2000

[29] Sethu, Murugesan ***PhD Thesis*** - *Performance Studies of Thin Film Electroluminescent (TFEL) Devices*, Nottingham Trent University, UK 2002

[30] Rack, Philip D. and Holloway, Paul H. The structure, device physics, and material properties of thin film electroluminescent displays, Materials Science and Engineering, Vol. R21, p. 171, 1998

[31] Ono, A. Electroluminescent Displays, World Scientific Publishing Co., Singapore, 1995

[32] Krasnov, Alex N. Selection of dielectrics for alternating-current thin film electroluminescent device, Thin Solid Films, Vol.347, pp. 1-13, 1999

[33] Lee, Y-H. et al., Roughness of ZnS : Pr,Ce/Ta O Interface and Its Effects on Electrical Performance of Alternating Current Thin-Film Electroluminescent Devices, IEEE Electron Devices, Vol. 46 No. 5, 1999

[34] Sze, S. M. *Physics of Semiconductor Devices, 2nd Ed.*, pp. 402-405, John Wiley, 1981

[35] Barbottin, G. and Vapaille (Eds.), A. *Instabilities in Silicon Devices: Silicon Passivation and Related Instabilites*, Chater 5 (The Nature of Electronic Conduction in thin Insulating Layers by Hesto, P), Elsevier Science, 1986

Chapter 5

Properties of Barium Strontium Titanate Thin Films and MIS Capacitors

Overview

This chapter deals with dielectric properties of the perovskite-type BST thin films as a function of thickness, growth, and other processing parameters. As a building block for analysing and understanding the properties of BST thin film, a typical metal-oxide-semiconductor (MOS) capacitor structure is fabricated and then capacitance and leakage current measurements are conducted as a function of voltage. From *Capacitance-* and *Current-Voltage(C(I)-V)* experiments, various important parameters to evaluate insulating thin film will be discussed in detail in this chapter. At the same time, a comparative study was carried out to evaluate how this perovskite material contributed to the characteristics of the inorganic EL devices in comparison to Y_2O_3-based EL devices. In Section 5.1, a background to barium strontium titanate is discussed and the structural properties of the BST thin films are covered in Section 5.2. The *capacitance-voltage* characteristics of MIS capacitors are considered in Section 5.3 (see Section 4.2 of Chapter 4 and Appendixes A and B for the fundamentals of MIS capacitor devices). In Section 5.4, flatband and threshold voltage, and instabilities at the interface will be discussed. Frequency effect, dielectric hysteresis and leakage current density are pointed out in Section 5.5. Finally, the summary of this chapter is mentioned in Section 5.6.

5.1 Review of Barium Strontium Titanate

Barium Strontium Titanate ($Ba_xSr_{1-x}TiO_3$, BST, or BSTO) thin films are becoming more important as perovskite-type ferroelectric solid solution materials of barium titanate ($BaTiO_3$, BT) and strontium titanate ($SrTiO_3$, ST) with high-κ properties. Stoichiometric $(Ba_xSr_{1-x})TiO_3$ ((Ba+Sr)/Ti = 1) thin films possess superior dielectric properties to those of pure $SrTiO_3$ thin films[1,2]. In particular, barium titanate ($BaTiO_3$) is the one of the most well-known perovskite type materials and has been studied widely. The crystal structure of the unit cell of barium titanate ($BaTiO_3$) can change from a rhombodedral(< -90 °C) to an orthorhombic(< 5 °C), a tetragonal(< 120 °C), and cubic(>120 °C) according to the temperature. While strontium titanate shows a paraelectric phase at room temperature and its *Curie* temperature was known

as 40 K by an extrapolation estimation, but, around -164 °C is the actual *Curie* temperature[3,4]. Thus, $SrTiO_3$ is known for having better stability in structure and temperature-dependent feature because it has no distortion by pyroelectric phenomenon and a relatively lower *Curie temperature*, respectively. In general, barium titanate (BT) has the maximum dielectric constant at the *Curie temperature*, T_c = 120~130 °C. The *Curie temperature*, T_c as a function of concentration (mole %) of $SrTiO_3$ in BST is illustrated in Figure 5-1. The equation of the *Curie temperature* for the bulk was reported as T_c (°C) = 131.5 - 295.4x (x = ratio of Sr in BST, or $SrTiO_3$ mole %)[5], but a modified *Curie temperature* equation, T_c (°C) = 118.95 - 298.9x[41]., was obtained for the thin films. Hence, $Ba_{0.5}Sr_{0.5}TiO_3$ has a Curie temperature of about -30 °C.

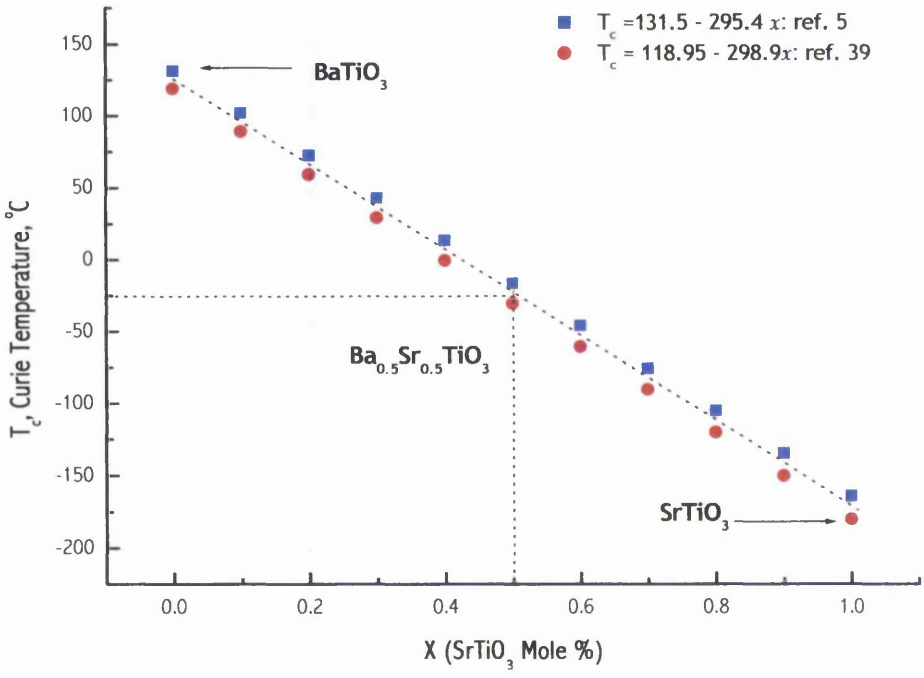


Figure 5-1 Curie temperature relationship of the bulk and thin film of a BST solid solution as a function of $SrTiO_3$ concentration ratio.

In order to utilise these merits from both materials - $BaTiO_3$ and $SrTiO_3$, the solid solution - $(Ba_xSr_{1-x})TiO_3$ - has been investigated with great interest. In particular, the ABO_3-family ferroelectric materials have been applied widely in dynamic random access memory

(DRAM)[6,7,8], wireless communication applications[9,10], bypass or multilayer ceramic capacitors(MLCCs)[9,11,12], optical applications[13] and many other electronic devices[14,15,16,17]. In addition, as investigated here, these high-κ dielectric or ferroelectric materials can used for the cladding layers in inorganic TFEL devices to take advantage of reducing a driving voltage of the devices. In order to make use of such a high dielectric constant feature of ferroelectric materials in EL applications, the perovskite-type thin films, such as $BaTiO_3$(BT) and $SrTiO_3$(ST), have been applied under various deposition/growth parameters[18,19,20,21,22].

Although BST thin films have great potential as an insulating layer of inorganic EL devices, the study of BST thin film as a solid solution in EL display devices has been limited except for a few reports or journals[1,23,24,25,26,27]. Thus, there is a need for more detailed studies to be carried out to improve and analyse various properties and effects of the perovskite-type oxide thin films, barium strontium titanate (BST).

5.2 Experimental Results and Discussion

5.2.1 $Ba_xSr_{1-x}TiO_3$ Thin Film Growth Parameters

In this study, BST thin films are grown using the systems and deposition methods described in Chapter 3. Growth parameters mentioned in Chapter 3 are re-summarised here briefly. The substrate temperature, sputtering time (i.e., thickness), sputtering gas mixture, post-annealing temperature and duration can affect the growth of thin film generally.

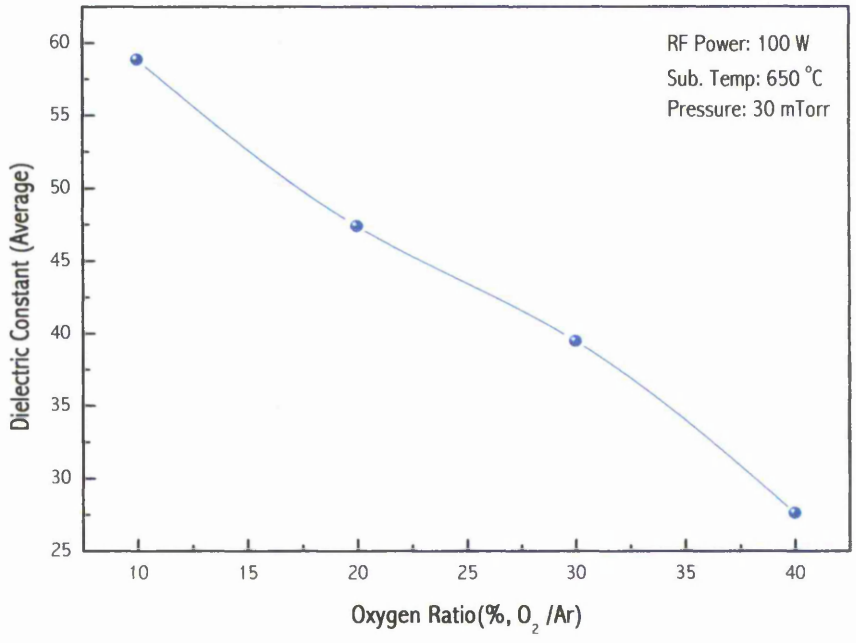
There are two different BST targets that were utilised with the same composition (x = 50%, $Ba_xSr_{1-x}TiO_3$). One was provided from South Bank University (SBU) and the other one is a commercial BST target from Testborne, Ltd. (UK). Initial deposition after loading the SBU target took more than 2 hours for one monitored interferometric cycle of deposition, but after a stabilisation period, the deposition time at 200 W dramatically reduced to around 60 minutes for one complete cycle, which was equivalent to 150 (± 10 nm) which was measured by various techniques described in Chapter 3. This will be discussed in the following Section 5.2.2 in detail. After this stabilisation stage of the targets, the two targets exhibited almost the same deposition rate.

Table 5-1 Deposition conditions for BST thin film

Deposition parameters	Deposition conditions
Base pressure	2.0×10^{-7} Torr
Sputtering pressure	10 ~ 60 mTorr
O_2 ratio (in Ar)	7 ~ 40%
Power Density	0.987 ~ 3.70 W/cm^2
Deposition rate	13.3 ~ 27.5 Å/min
Thickness	70 ~ 320 (+ 10) nm
Substrate temp	300 ~ 700 °C (10 ~ 50%)

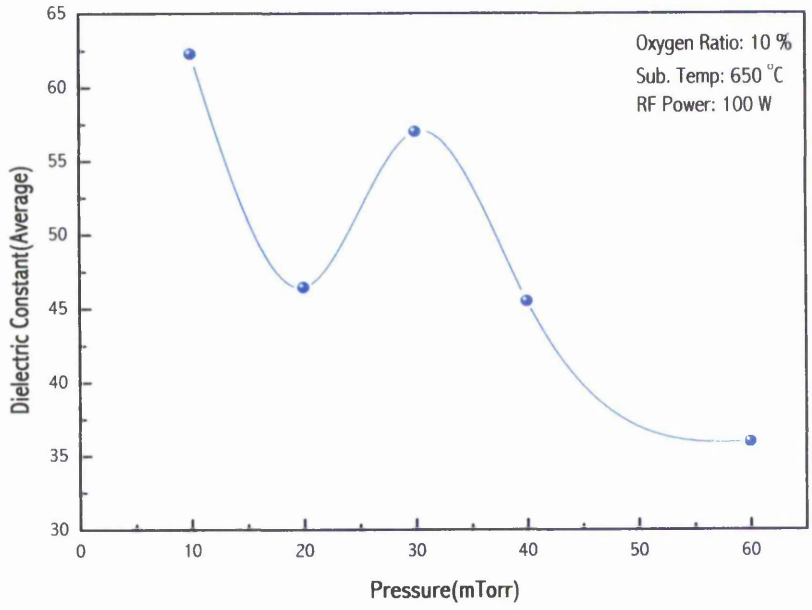
The growth conditions for BST thin films are summarised in Table 5-1. The deposited BST thin films clearly show higher dielectric constant at lower substrate temperature (300 (± 50) °C), sputtering pressure (10 mTorr), oxygen ratio(10%) and RF powder (100 W). The dependences of these growth parameters are plotted in Figure 5-2, respectively. In particular, the substrate

temperature at 10% (rate on a controller display of a heater, approximately 300(± 50) °C equivalent) showed the highest dielectric constant of 85 compared to other samples. Another important factor for evaluating dielectric materials is the dielectric loss (i.e., tanδ) or dissipation factor(D). It shows a similar trend in value regardless of the growth parameters and target used, but the dielectric loss is larger in the thin films(~ 1.5) of SBU target than the commercial one (< 0.2). Oxygen ratio has a significant effect on growth rate compared to the other three parameters. When the oxygen ratio increased from 10% to 40%, the growth rate per a cycle (time/cycle) dramatically dropped to more than 50%: (27.5Å/min at 10%, and 13.3 Å/min at 40%). Thus, from these deposition parameters, optimum BST thin film growth conditions are established for this study: the substrate temperature of 10(± 1)% (= 300 - 350 °C), the sputtering pressure of 10 mTorr, oxygen content of 10% and the RF power of 100 W are obtained as the optimised growth parameters for the BST thin film deposition by rf-magnetron sputtering. Therefore, hereafter all BST thin films are deposited at the suggested optimum conditions above if there is not any other note on thin film growth conditions.

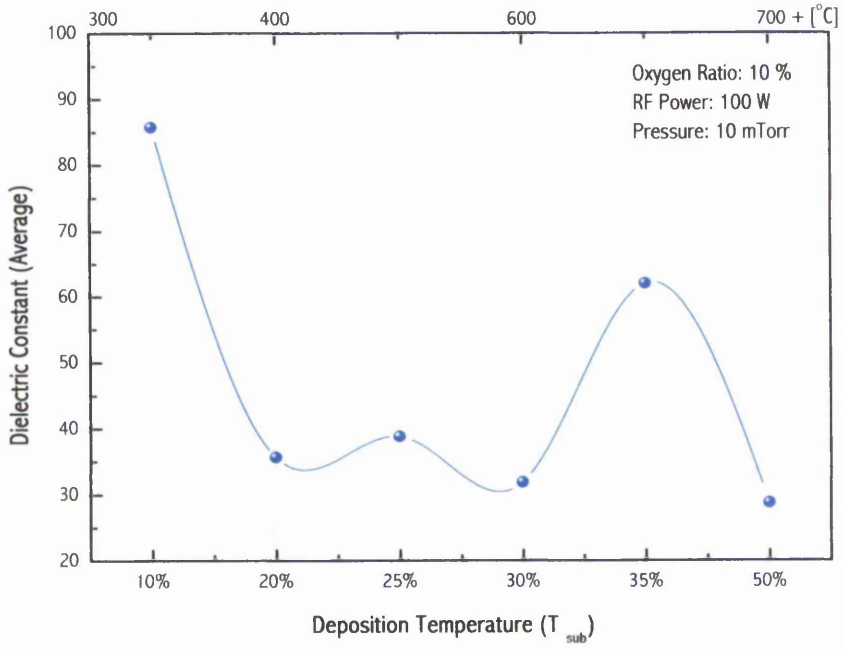


(a) Oxygen ratio of sputtering gas(O_2 to Ar)

Figure 5-2 The growth parameter dependence of the dielectric constant of BST thin film with 150 (± 10) nm-thick: (a) oxygen contents, (b) pressure, (c) substrate temperature, and (d) rf-power

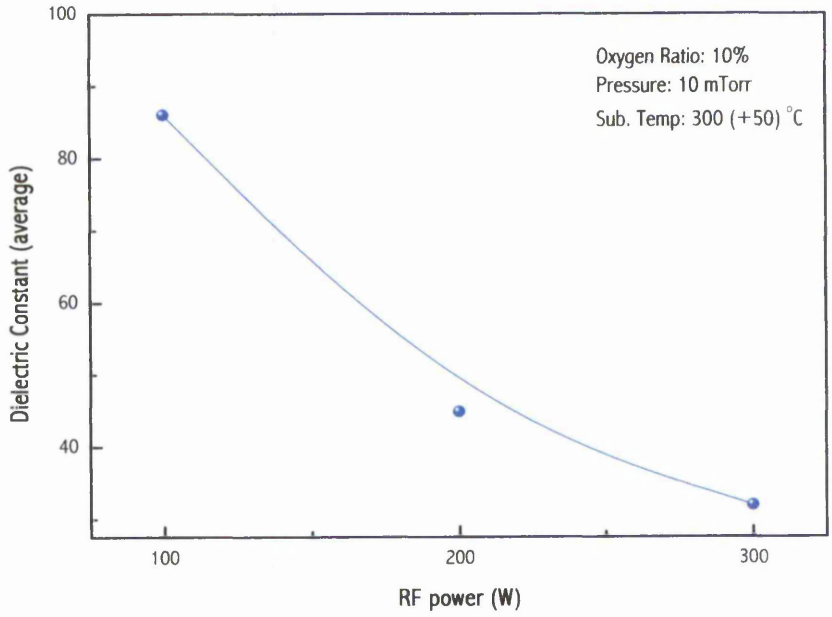


(b) Sputtering Pressure Dependence



(c) Deposition Temperature

Figure 5-2 (Continued) The growth parameter dependence of the dielectric constant of BST thin film with 150 (+10)nm-thick: (a) oxygen contents, (b) pressure, (c) substrate temperature, and (d) rf-power



(d) RF Power Dependence of dielectric constant of BST thin films

Figure 5-2 Continued.

5.2.2 Optical properties: Refractive index and Thickness

In addition to use in gate dielectric materials for DRAM application, there is also great interest in the study of optical properties of BST thin films because of their high electro-optical coefficient[13]. These films are expected to be excellent in realizing various optical applications because of their wide energy bandgap ($E_{g(BST)}$ = 3.2 eV), large static dielectric constant, high refractive index and low absorption coefficient[28]. Solid solutions allow for the possibility of changing many properties of the thin films, including refractive index, microstructure and surface roughness. BST films can display a paraelectric phase by controlling the Ba/Sr ratio and have a high transparency; hence they can be used as an insulating layer of electroluminescent devices [28]. The optical properties of BST can attract more interest because of the feasibility in flat panel display application and integrated optics [28].

The deposited BST thin film's thickness was estimated by the interferometric method and then it was confirmed optically and physically by using a spectral interference system - F20 FILMETRCS™ and a stylus-type Dektek system - 6M(Veeco, USA), respectively. Using the Equations 3-4 and 3-5, a complete cycle of thin film deposition exhibited average 150(±10) nm-thick of BST thin films and the refractive index, n, has the wide range of 2.09 ~ 2.39, but the measured refractive index by the spectral interferometric system (F20) has the lower range of 2.04 ~ 2.10 (average) at 632.8 nm wavelength as a function of thickness (i.e., the number of cycles). These calculated or measured refractive indexes are in the range of the values were reported in the literature[29,30,31,32,33,34]. For comparison, the refractive indexes of the single crystals, $BaTiO_3$ and $SrTiO_3$, are 2.37 and 2.41[35,36,37] at the wavelength of 589.3 nm, respectively and for thin films, they were 1.99 ~ 2.51 and 2.02 ~ 2.47 as a function of temperature, respectively[38]. Based on thickness measured by the thickness measurement system, 6M, the average refractive index of the BST thin films was set on 2.23 for the calculation and this study. The refractive index of the BST thin film increased with the substrate temperature from 2.08(@ 350 °C) to 2.31(@ 500 °C). It is believed that densification of the thin film between 350 °C and 500 °C takes place [39]. Refractive index as a function of substrate temperature is shown in Figure 5-3 including other reference data. Even though Wang et al.,[40], had different Ba/Sr ratio(x = 0.7) and a little higher value in the entire range of temperature, but it exhibited the similar trend in refractive index clearly regardless of film composition. As the substrate temperature increases, the refractive index increases

correspondingly due to increasing of a packing density and improved crystallinity of the thin film[28,40]. According to the result by Wang et al., the refractive index was increased significantly around 450 °C for the entire range of wavelength (400 ~ 900 nm), which may be another evidence of densification of the thin film around that temperature. In fact, approximately 400-450 °C has been accepted widely as a phase-transition temperature to the polycrystalline phase. These values are in good agreement with the range of the results reported in other references [41,42]. In addition, the refractive index is also increased by rapid thermal annealing (RTA) process, but the value was lower [43].

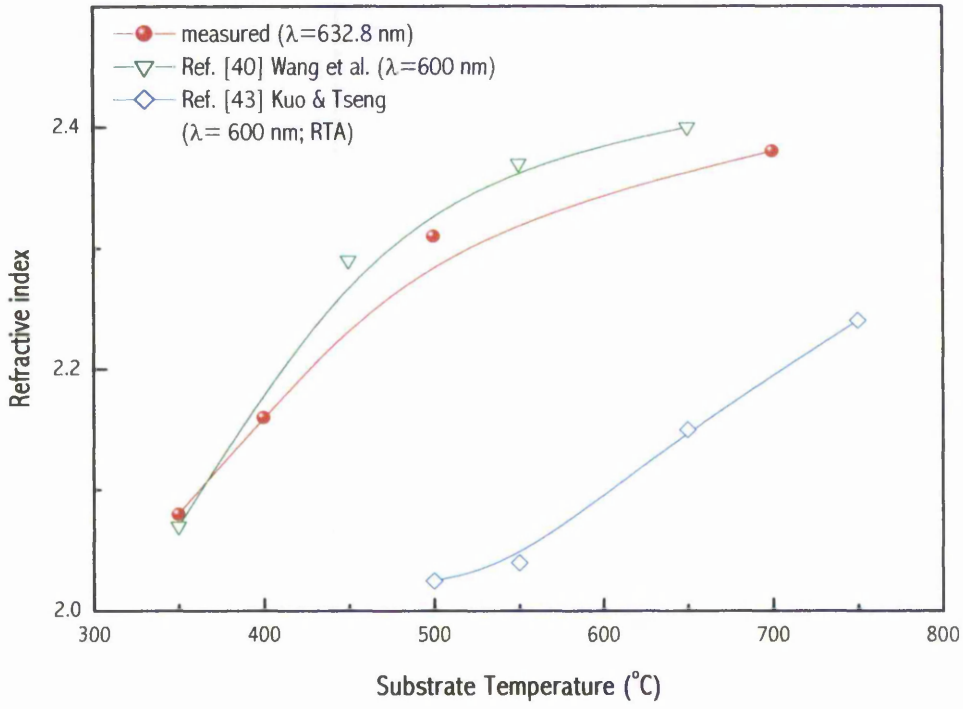


Figure 5-3 Refractive indexes of $Ba_xSr_{1-x}TiO_3$ thin films as a function of substrate temperature

Refractive index was affected by a post-annealing process as shown in Figure 5-3. As additional process, a pulsed laser annealing treatment was applied to the thin film and then refractive index was investigated with the cases of thermal- and non-annealed thin films. Laser annealed thin films reached at the highest refractive index (= 2.42) at certain thickness

(160 nm, only) and then decreased as the thickness of the films increased. However, the refractive indexes of laser annealed and non-annealed thin films were not much different. Overall, BST thin films displayed higher value in refractive index than thermal- or non-annealed thin films. Thus, in order to obtain higher refractive index, a proper laser-annealing process can be effective. More interestingly, unlike thermal-annealing, laser-annealed thin films demonstrated a decrease in thickness physically. Probably, this was the result of an ablation effect in interaction between highly coherent light and materials even though maximum 10 pulses (λ = 248 nm, KrF Laser) were irradiated. On average, the thickness difference was approximately ~ 40 nm.

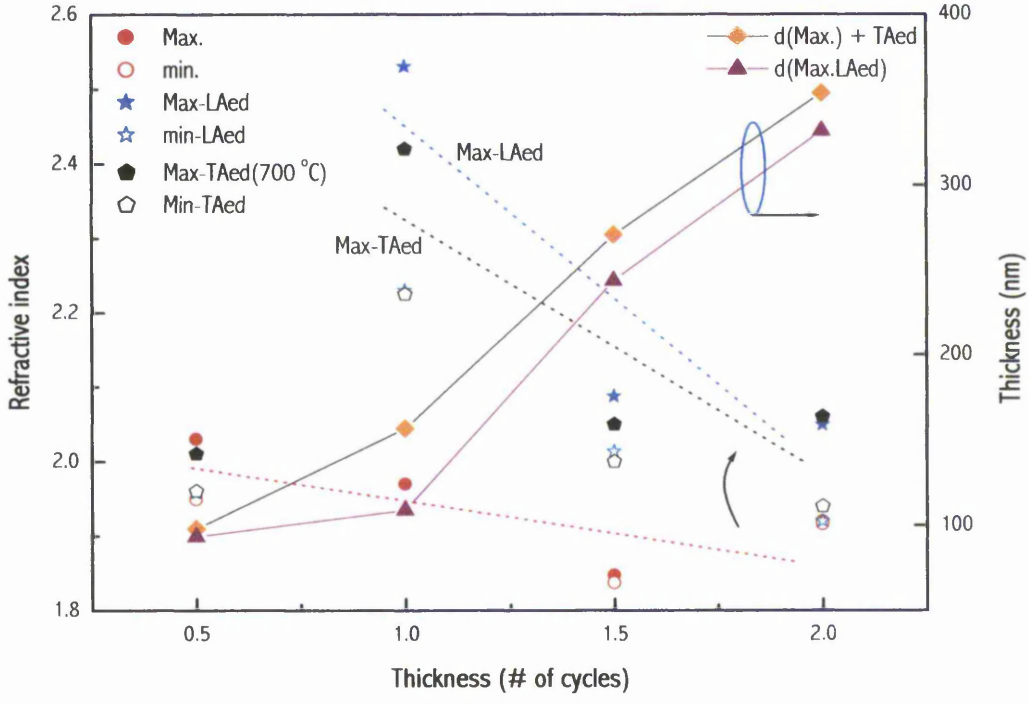


Figure 5-4 Post-annealing process effects in refractive index and film thickness of $Ba_{0.5}Sr_{0.5}TiO_3$ thin films as a function of post-annealing methods (laser- and thermal-annealing).

In terms of thickness of BST thin films, initially the colour of the film can be related to its thickness using an appropriate colour chart of Si_3N_4, Y_2O_3, and SiO_2 on silicon substrate[44,45]. Therefore, it is useful to use visible colour as an estimate of the thickness and uniformity of thin films. The corrected colour chart for BST thin film deposited in experiments is given in

Table 5-2 (with Si_3N_4 and Y_2O_3 thin film equivalents). During the deposition, *in-situ* film thickness monitoring by an optical interferometric technique is utilised to inspect growth of thin film as a real-time monitoring process. This interferometric technique was discussed in detail in Chapter 3.

Table 5-2 A colour chart of BST thin films based on their thickness

Cycle(s)	Thickness(Å)	**BST**	Y_2O_3[44]	Si_3N_4[45]
½	700 ~ 800	**Light blue**	Deep blue	Dark - red violet
1	1400 ~ 1700	**Light yellow**	Yellow	Light-gold and yellow
1 ½	2100 ~ 2500	**Greenish blue**	Blue green	Blue- blue green
2	2800 ~ 3300	**(Reddish) purple**	Red	Green yellow - violet red

5.2.3 Structure of r.f.-magnetron sputtered $(Ba_xSr_{1-x})TiO_3$ thin films

5.2.3.1 X-ray Diffraction Patterns of $(Ba_xSr_{1-x})TiO_3$ thin films

In order to understand BST structural properties, X-ray diffraction (XRD) experiments are performed and their patterns are investigated. Regarding X-ray diffraction patterns of the sputtered grown BST thin film, it is very useful to take a look at the X-ray diffraction patterns of other ABO_3-family materials - $SrTiO_3$ and $BaTiO_3$, respectively. According to International Centre for Diffraction Data (ICDD) powder diffraction file (PDF) data, the most significant five peaks of the diffraction data are summarised in Table 5-3. In this table, the angle(2θ) is calibrated correctly with X-ray source material, Cr (λ = 2.2897 Å), which was used in XRD analytical experiments for this study. For BST, the corresponding peak angels of the Cu source are included in parenthesis in the column of BST. While the BST's lattice constant is 3.947 Å, ST and BT have the lattice constant of 3.905 and 4.01 Å (for cubic), respectively[35,39].

BST thin films were deposited under the deposition conditions of the substrate temperature of 350 °C (10%), RF power of 100 W and sputtering pressure of 10 mTorr, respectively. The thickness of the thin film was approximately 300 (± 10) nm. After post-annealing BST thin films at 500, and 600 °C, respectively, some peaks are observed at approximately 48.0°, 60.0°, and 90.84° and their corresponding planes can be matched with (110), (111), and (211) planes according to the powder diffraction file(PDF) reference data in Table 5-3. The XRD patterns of the sputtered BST thin film are shown in Figure 5-5 including the XRD pattern of the non-annealed BST thin film for comparison.

Table 5-3 Interplanar spacing, intensity, orientation, and angles of ST, BT and BST XRD reference data [46]

$SrTiO_3$				$BaTiO_3$				BST			
d Å	Int.	*(hkl)*	2θ	*d*Å	Int.	*(hkl)*	2θ	*d* Å	Int.	*(hkl)*	2θ(for Cu)*
2.759	100	110	49.04	2.850	100	110	47.37	2.792	100	110	48.42(32.03)
2.253	30	111	61.07	2.328	30	111	58.91	2.280	64	111	60.28(39.50)
1.952	50	200	71.82	2.016	35	200	69.21	1.9737	74	200	70.91(45.95)
1.594	40	211	91.81	1.425	25	211	88.24	1.6114	78	211	90.55(57.11)
1.381	25	220	111.99	1.344	15	220	106.91	1.3954	64	220	110.26(67.01)

* In BST column, the detection angles of X-ray source(Cu) are in parenthesis for a reference.

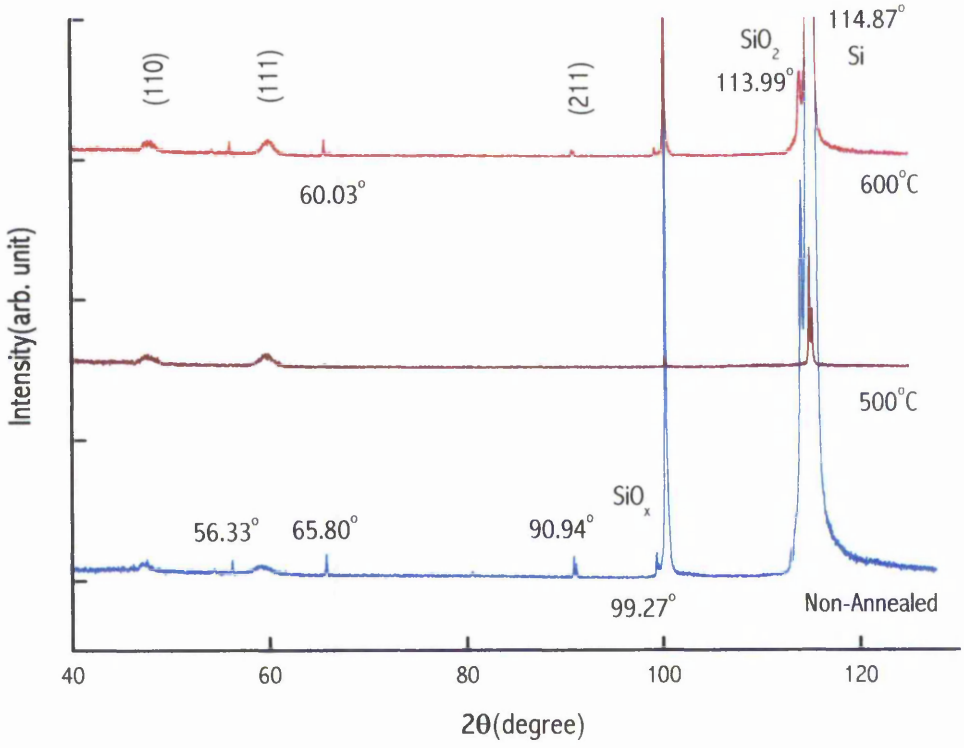


Figure 5-5 X-ray diffraction patterns as a function of post-annealing temperature: non-anneal (NA), 500 and 600 °C

The X-ray patterns reveal that the deposited thin films have a cubic structure and they show background interference from the substrate and a low dielectric constant interface layer with a pseudo-BST-SiO_x system which is often called a "dead layer". The SiO_x interface layer between BST and the substrate is created regardless of the thermal annealing temperature. Possible existence of SiO_2 interlayer can be confirmed by typical peaks at the angles of 47.46(47.53)‡, 54.38(54.82), 65.80(65.44), 90.94(90.49), 99.27(99.94) and 113.99(113.93) - the angles in parentheses are the reference data of SiO_2 XRD peaks. In general, the fact that SiO_2 or a metal silicide interface layer between high-κ perovskite material and Si substrate is formed easily during the deposition has been well known[47]. This undesirable new layer in between can lead to degradation of the perovskite-base devices due to lowering the total capacitance and increasing leakage current. In particular, a higher substrate temperature can accelerate the creation of the SiO_x-based interfacial layer. In the previous section 5.2.1, the reduced dielectric

constant of the BST thin film grown at high substrate temperature could be a possible evidence of this effect.

Figure 5-6 displays the reduced scale of the X-ray diffraction patterns from Figure 5-5. In addition, the XRD pattern of the BST thin film annealed at 700 °C is added. Figure 5-6 demonstrates a shifting effect of the diffraction peaks clearly as the annealing temperature increases. In particular, (110) and (111) planes are shifted to the right side with increase of annealing temperature. In this experiment, the sputtered BST thin film had stronger intensity in (111) orientation preference and additional post-annealing treatment improved the crystallinity of the BST thin film.

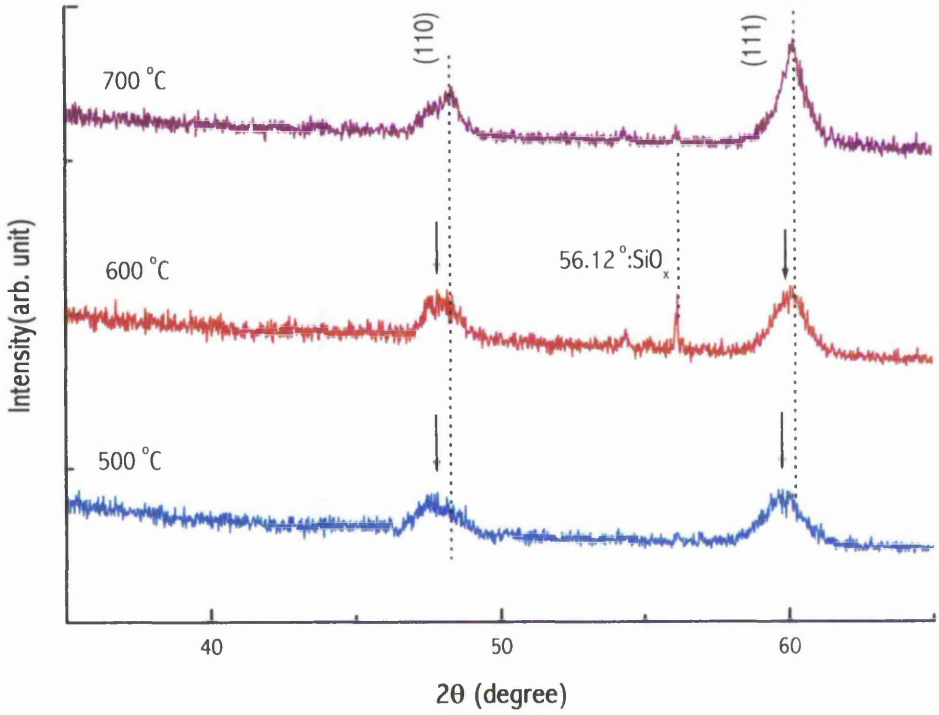


Figure 5-6 X-ray diffraction peak shifting of (110) and (111) planes according to annealing conditions. A possible SiO_2 peak is observed.

The orientation of the thin films was reported by Matsubara, S et al.[48] and Cook, L.P. et al.[49].

‡ The peaks at the angles might show splitting and/or mixed peaks from BST and SiO_2 layer.

The orientations of the perovskite-type materials resulted from tensile stresses and a compressive stress, respectively. The tensile stress is affected by a lattice mismatch and a thermal expansion coefficient difference and the compressive stress depends on a self-bias effect [48]. Regarding the tensile stress, $Ba_{0.5}Sr_{0.5}TiO_3$ can have the strongest tensile stress effect. As a result, the thin films may have (110) preference peak while the pure $BaTiO_3$ and $SrTiO_3$ thin films shows the trend of (100) preference[24], respectively. However, the results show somewhat differences in their preference orientation. The orientation preference differences among three major peaks - (100), (110), and (111) seems to result from the substrate material, film composition (e.g., Ba/Sr ratio > 1), lattice mismatch and interface layer(BST-SiO_x) created between BST thin film and the substrate.

When BST thin films are deposited on Si substrate, we need to consider lattice constants of BST and Si, respectively. As mentioned above, BST with cubic structure is 3.947 Å while silicon has 5.431 Å. While a SiO_2 interface thin layer is usually an amorphous state under the common semiconductor device processing and thermodynamically unstable below 1710 °C[50], it does exhibit a tetragonal structure in a short range structure or in higher temperature and its lattice constants are a = 4.9732 and c = 6.9236 Å, respectively [50]. Due to large lattice constant difference between BST and Si substrate, BST thin film on Si substrate is rotated around by 45° to minimise their internal distortion (i.e., strain) and the lattice mismatch difference. The lattice mismatch difference possibly could be reduced dramatically if the lattice mismatch can be larger than 38% without 45° rotation; i.e., $\frac{(a_{Si}/\sqrt{2} - a_{BST})}{a_{BST}} = -2.7\%$ [51,52] Another lattice mismatch difference between BST and SiO_2 interlayer is equal to approximately 10% in terms of BST thin film and SiO_2 a-axe lattice constant. This rotation of BST thin film on Si substrate is very likely to take place. In fact, this similar effect was reported when $SrTiO_3$ thin film is grown on Si substrate directly [51,52]. Thus, this rotation may lead the BST thin film to have (111) orientation preference on a BST-(SiO_x)-Si system.

The non-annealed BST thin films have the same plane peaks, but those peak intensities are relatively weak and broad compared to other annealed samples. In particular, the (111) peak at the angle of 60.35° is clearly shifted on the annealed sample. However, the detected peak at 90.94° is relatively weaker after annealing the samples. The reason for this trend is not clear because the peak can be attributed to BST(90.55°) and at the same time relation of SiO_2(90.49°)

peak is possible. The most significant peak of SiO_2 at the angle of 99.94 ° is reduced in its intensity after annealing treatment. From this evidence, after annealing the sample, the corresponding peaks of BST are more enhanced in their intensity. In spite of that, SiO_2 (302) plan peak is still much stronger than any other BST peaks.

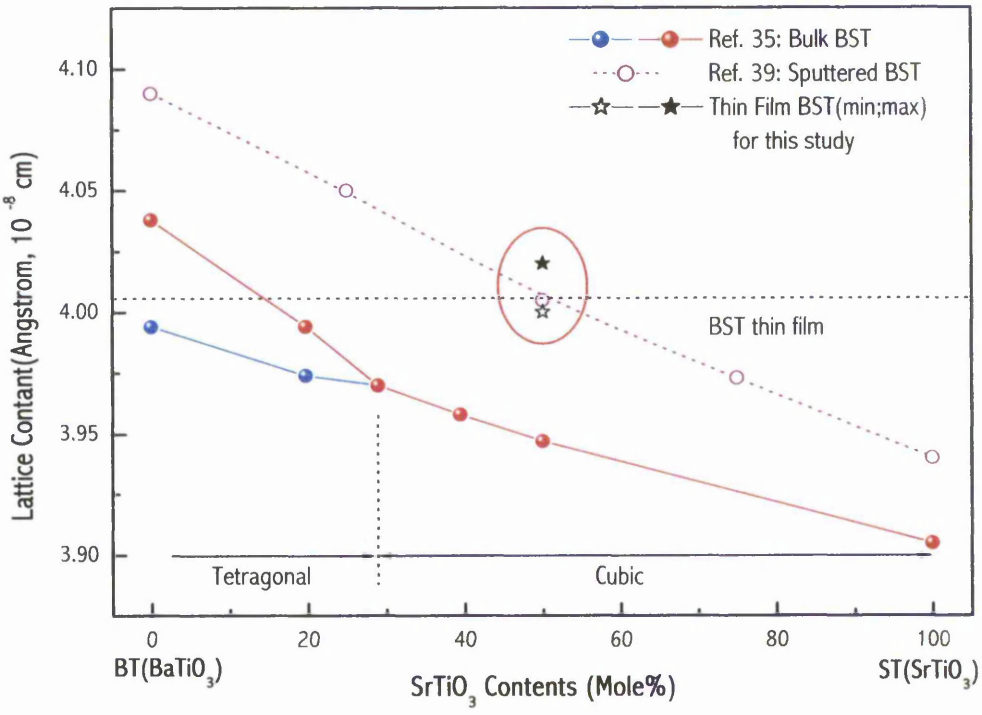


Figure 5-7 Lattice constant variation of the sputtered thin films and the bulk $(Ba_xSr_{1-x})TiO_3$ as a function of $SrTiO_3$ contents[35,39,41].

The interplanar spacing (often, so-called d spacing) can be calculated according to the equations, $d_{hkl} = \frac{a}{\sqrt{(h^2 + k^2 + l^2)}}$ for a cubic structure and $d_{hkl} = \frac{n\lambda}{2\sin\theta_{hkl}}$ (n is an integer).

Thus, according to the equation for the cubic structure, d_{110}, d_{111}, and d_{211} are 2.825, 2.288, and 1.607 Å, respectively. These calculated d spacing values are in good agreement with the reference data which are given in the Table 5-3. Therefore, the lattice constant of the sputtered BST thin film is larger than that of the BST bulk due to non-equibrilium states caused by having strain in thin films during the growth by sputtering[35,39]: a_{tf} = 3.995~ 4.02 and a_{bulk} =

3.95. For the bulk of the BST, the lattice constant decreases with the content of $SrTiO_3$ which is shown in Figure 5-7[35]. The measured lattice constant of the sputtered BST thin film are also shown in Figure 5-7. This trend that the lattice constant of thin film is larger than that of the bulk in perovskite-structure $BaTiO_3$ and $SrTiO_3$ is supported by other research teams[39,41].

By using the Scherrer formula (See Equation 4-21), the crystal size of BST thin films is approximately 14.1 (700 °C), 10.2(600 °C) and 8.3 nm (500 °C), respectively. In addition, laser annealed BST thin film (See Figure 5-8) has around 41.4 nm of crystal size. Laser annealing process shows feasibility to improve crystallinity of BST thin films by re-growing and re-crystallization compared to the crystal size of thermal annealed thin films. However, the peak angles (47 ° and 60.2°) are different, thus an absolute comparison is not suitable at this moment.

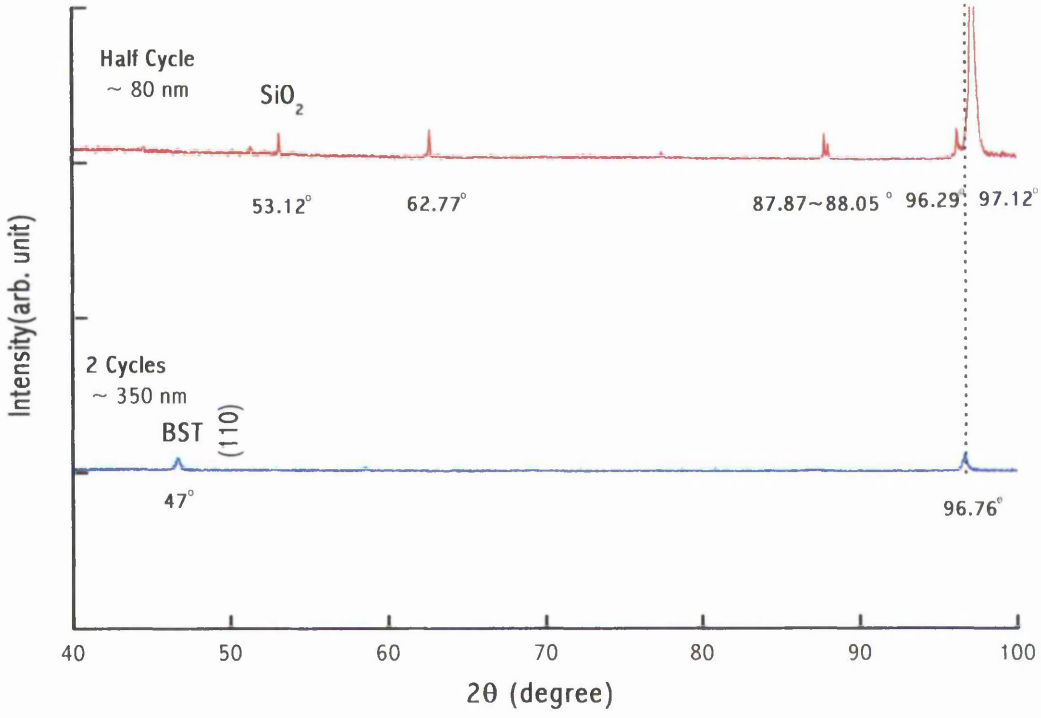


Figure 5-8 XRD patterns of pulsed laser annealed BST thin films with different thickness, 80 nm (half cycle) and 320(± 30) nm (2 cycles), respectively. 70 laser radiation pulses with approx. 300 mJ/cm² (KrF λ = 248 nm) are applied.

As a further investigation of the effect of annealing, pulsed laser annealing was applied to BST thin films as a function of thickness. The X-ray diffraction patterns of pulsed laser annealed BST thin films are shown in Figure 5-8. An 80 nm thick BST thin film has interestingly SiO_2-related peaks only while the other 320 nm-thick BST sample shows only the (110) plane. There are only two noticeable peaks at 47° and 96.76°, respectively, and they are relatively weak in intensity as well. The peak at the angle of 47° can be attributed to the BST plane with (110) orientation. These peaks are probably shifted to the left. The peak shifting effect can be identified on the 80 nm-thick samples as well. At least approximately 2~3 degrees are shifted to the left. In other words, the refraction angles are reduced slightly as a result of laser annealing. The left shifting of peaks means the increase of the crystal size and lattice constant. By the laser annealing process the surface of the thin film (~ 20 nm deep) seems to recrystallize and re-grow, thus, the grain size becomes larger[53] and after regrowing and recrystallzing, phase transition can take place. In addition, it is necessary to bear in mind that experimental error from lack of reproducibility in sample preparation can cause the peak shifting to left.

The existence of SiO_x interfacial layer between BST thin film and Si substrate can cause an oxygen deficiency within BST thin films. The oxygen deficiency in BST thin film is well known from many other reports [53,54]. Oxygen deficiency could accelerate the phase transition from a cubic to a tetragonal structure. Unfortunately, peak splitting due to the phase transition is not confirmed. Due to the lack of number of the peaks, manual or auto-indexing of the detected peaks is practically is not possible.

There is an important result regarding laser annealing and the film thickness. After the laser annealing, the SiO_2-related peaks seems to be removed effectively on the 320-nm thick BST sample. It is assumed that the undesirable SiO_2 interfacial layer can be reduced after laser annealing. This result supports the thickness-dependence of the deposited BST sample. According to Baldus, O. *et al.*[55], the optimum thickness of laser annealed BST thin films for reducing the interface or a dead layer was suggested as approximately 95 nm. However, the important differences between these cases are the device structures and the ratio of Ba/Sr; one is deposited directly on Si substrate, the other one is deposited on a multilayer structure with $Pt/Ti/TiO_2/SiO_2/Si$ in order to avoid interfacial layer creation between bottom electrode(Pt) and BST gate oxide for DRAM applications. In addition, the ratio of Ba/Sr is 1and 2.33,

respectively.

In summary, the films investigated here, when the laser annealing is applied to BST/Si, 300 nm-thick BST sample is better than a thinner film in terms of crystalline quality as indicated by X-ray diffraction patterns. It can be understood there may be some possibility of reducing or removing the interfacial or dead layer of the pseudo-BST-SiO_2 system (i.e., $Ba_xSr_{1-x}TiO_y$-SiO_z, for instance) effectively by the laser annealing. However, in order to fully understand the laser annealing effects mentioned above on the BST film, additional further study is needed.

5.2.3.2 Scanning Electron Microscopy of $(Ba_xSr_{1-x})TiO_3$ thin films

The cross-sectional view of the BST thin films by scanning electron microscopy (SEM) analysis is given in Figure 5-9. The main purpose of SEM analysis is to investigate the thickness of the BST thin film and existence of SiO_2 interface layer. Regardless of post-annealing treatment, it was difficult to identify the interfacial layer between BST thin film and Si substrate. Thus, the SiO_x interface layer thickness was not determined due to the resolution of the Scanning Electron Microscopy (SEM) system. However, the thickness of deposited BST thin film can be confirmed and they show good agreement with other thickness measurement results mentioned previously.

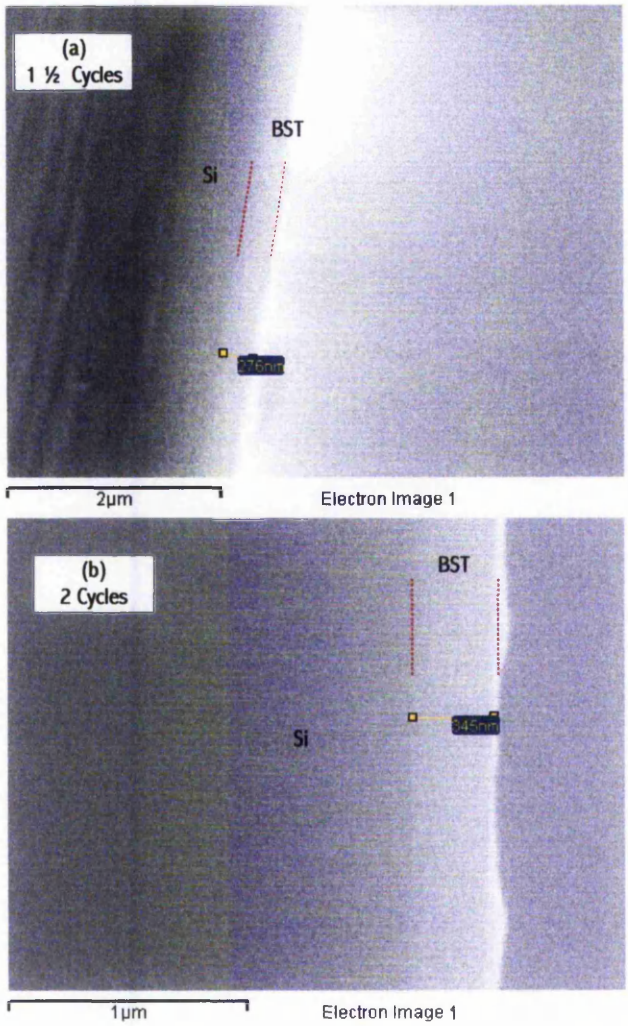


Figure 5-9 The cross-section and thickness of BST thin films by SEM analysis: (a) 1½, (b) 2 cycles

5.2.4 Instabilities in Capacitance-Voltage

From the *C-V* analysis, the BST MIS capacitors show two different types of *C-V* curves which are shown in Figures 5-10 and 5-11. Figure 5-10 shows the capacitance in accumulation region of the BST MIS devices remains constant regardless of the applied gate voltage and the diameter (i.e., area) of the top Al electrode, respectively. However, Figure 5-11 displays capacitance decreases under the accumulation condition after reaching the maximum capacitance as the gate voltage increases. It is believed that this capacitance change might come from BST thin film's tunable properties which have been studied widely in BST thin film's for microwave applications. Tunability of ferroelectric materials is defined as $[\varepsilon_{max}(v_o)-\varepsilon_{min}(v)]/\varepsilon_{max}(v_o)$, where v_o is zero applied bias and v is the corresponding applied voltage at minimum dielectric constant [56]. In order to make use of BST thin films as the dielectric layer in TFEL devices, the capacitance change can lead to a reduced dielectric constant of the thin films so that it is not desirable in practice. However, the capacitance change as a function of the gate voltage is not so significant. Thus, the measured maximum capacitance is applied as a saturated capacitance in accumulation region for this study.

The calculated dielectric constants of the 160nm and 100nm-thick BST thin films at 1 MHz under the accumulation condition are 62.3 and 32.4, respectively. When the thickness of BST thin film increase from 1/2 to 2 cycles , the corresponding dielectric constants show some deviation from the linear relationship($\varepsilon_r \propto d$, if the capacitance were not changed) between dielectric constant and thickness. For the area of the electrode, it shows lower dielectric constant than estimated figures. On average, the observed dielectric constants are a multiple of 1.43 and 1.26 in thickness (# of cycles, increasing) and electrode diameter (mm, decreasing), respectively. This relationship is shown in Figure 5-12.

Under the inversion region, the minimum capacitance (C_{min}) represents the total capacitance of the MIS capacitor system which is a series combination of the oxide capacitance (C_{BST}) and the semiconductor depletion-layer capacitance(C_{SD}). Thus, the semiconductor depletion-layer capacitance (C_{SD}) is calculated by Equation A-2 in Appendix A.

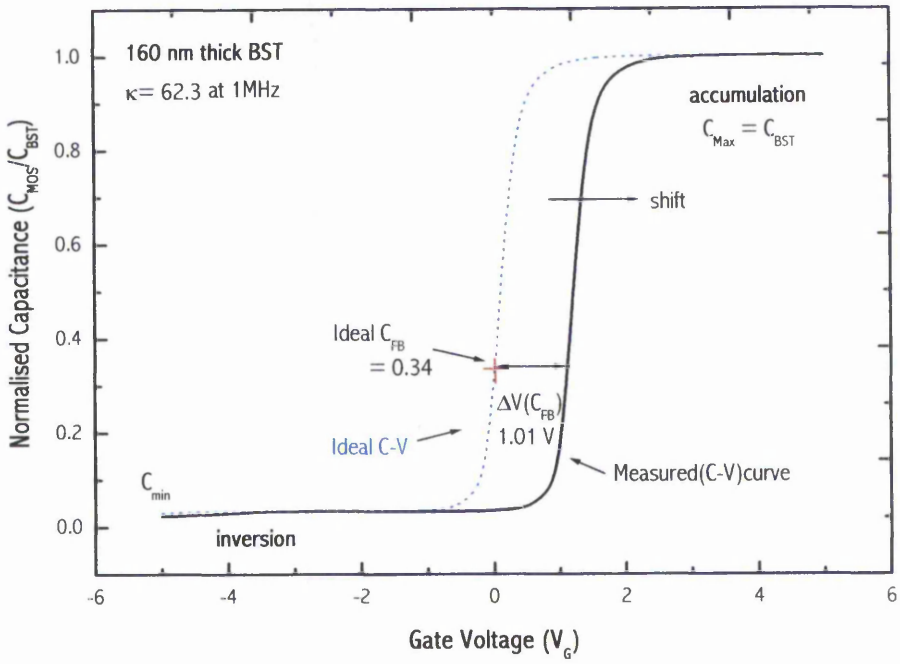


Figure 5-10 Normalised *C-V* curve of the 160 nm-thick BST MIS capacitors which is based on Figure 5-8.

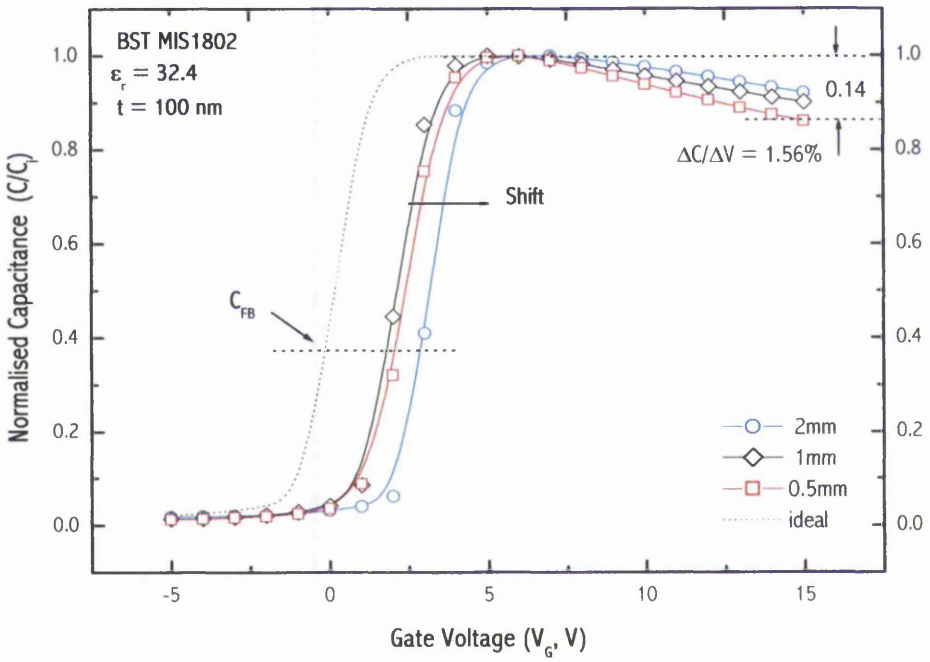


Figure 5-11 Normalised *C-V* curve as functions of gate voltage and a top electrode diameter of the 100 nm-thick BST MIS capacitors.

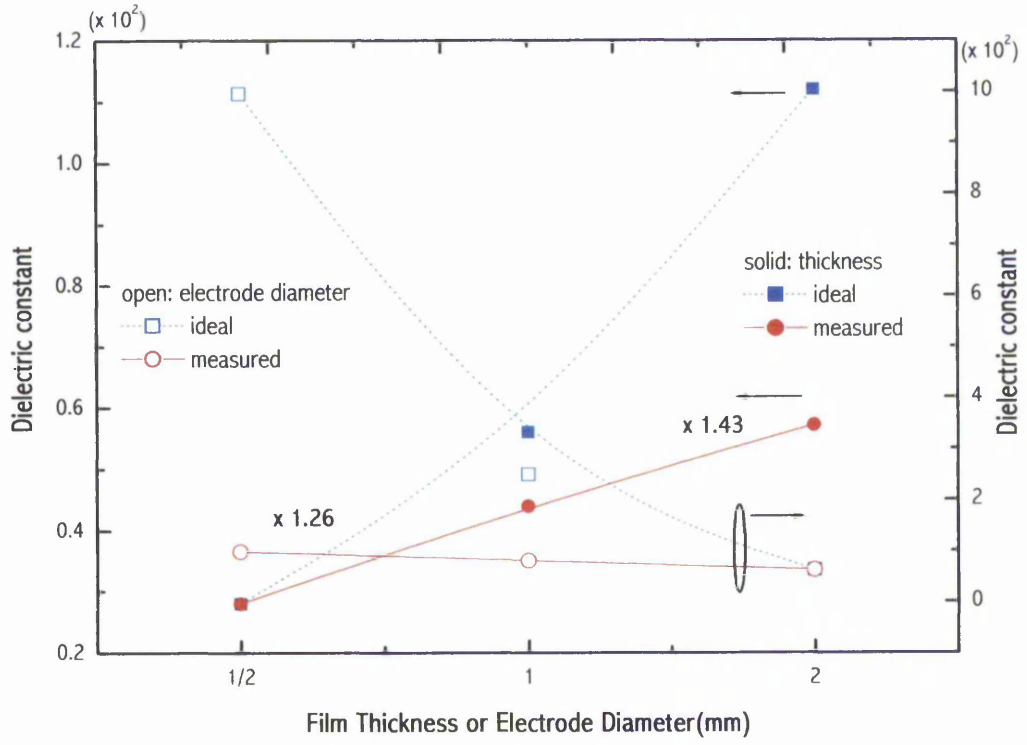


Figure 5-12 Dielectric constant of BST thin film as functions of film thickness and electrode area

The capacitance of the MIS capacitors in accumulation condition, C_{BST} is 3.45 × 10^{-7} F/cm² (Figure 5-10) and 2.87 × 10^{-7} F/cm² (Figure 5-11), respectively. The total capacitances (e.g., minimum capacitance) of MIS capacitor in inversion condition, C_{min}, are 2.34 x10^{-8} F/cm² and 2.31 x 10^{-8} F/cm², respectively. Hence, each normalized flatband capacitance (C_{FB}/C_{BST}) of an ideal MIS capacitor is 0.343 and 0.386, respectively and they are indicated in Figures 5-10 and 5-11. However, real devices have various charges in the oxide, at the interfaces, and at the surface of the substrate. These various charges and *C-V* curve basics are discussed in Appendix B in detail. In addition, the work function difference (ϕ_{ms}) between a metal electrode and the substrate should be considered. Thus, an ideal *C-V* curve commonly shows shifting phenomenon and the shifting direction depends on the polarity of the charges in the MIS system.

From Figures 5-10 and 5-11, the shifting effect is easily identified from the ideal *C-V* curves. In order to investigate various charges, the shape of the *C-V* curve can be important because the shape of *C-V* curve implies a major type of charges involved at high frequency measurement conditions. Figure 5-10 exhibits a rigid parallel shift which means the shift of the *C-V* curve is a result of fixed oxide charges[57]. In addition, the rigid parallel shift can imply mobile charge and interface traps are small enough so that they can be neglected[57]. The fixed oxide charges (Q_f) had the following features that they are fixed at the Si-oxide(BST, here) interface; they can not charged or discharged over a variation of a surface potential; they come from dangling bonds[58] at the surface of Si substrate; they are generally considered as positive charges. However, the direction of the shift in Figures 5-10 and 5-11 is more positive value of gate bias, which means unlike a general fixed oxide charge feature mentioned above, the fixed oxide charge is not positive, but negative[59,60]. The positive Q_f charge causes the decrease of capacitance at a fixed gate voltage from the ideal case. Charge neutrality requires every positive charge on the gate to be compensated by an equal and opposite charge in the BST layer and the Si substrate[59]. A depletion width (W_m) of a fixed-oxide-charge-free ideal case (Q_f = 0) is going to increase to maintain the charge neutrality condition because of the existence of additional negative fixed oxide charge. Thus, the decrease of capacitance of the *C-V* curve happens and the result is a shift of the *C-V* curve toward more positive gate bias for negative fixed oxide charge.

The fixed oxide charge can be obtained by the following equations,

$$Q_f = (\phi_{ms} - V_{FB})C_{BST} \qquad \textbf{Equation 5-1}\ [61]$$

or

$$\Delta V_f = \frac{Q_f}{C_{BST}} \qquad \textbf{Equation 5-2}\ [59]$$

where, ϕ_{ms} is work function difference between Al top electrode and the Si substrate, V_{FB} is a flatband voltage(= 1.11 *V*, Figure 5-10), and ΔV_f is voltage difference between a measured value and an ideal value at the flatband capacitance (C_{FB}). In a rigid parallel shift, the fixed oxide charge can be just total oxide charge ($Q_f = Q_{oxide}$).

The estimated fixed oxide charge concentration per unit area ($N_f = Q_f/qA$) are 3.49×10^{-12}, or 3.28×10^{-12} Cm^{-2}, respectively. Two obtained values are almost the same due to a very small work function difference (~ 0.04). Here, it should be mentioned that the electron affinity of BST material is different from literature to literature (χ_{BST} = 1.7 ~ 4.1 eV)[15,62,63,64] so that there is unavoidable uncertainty.

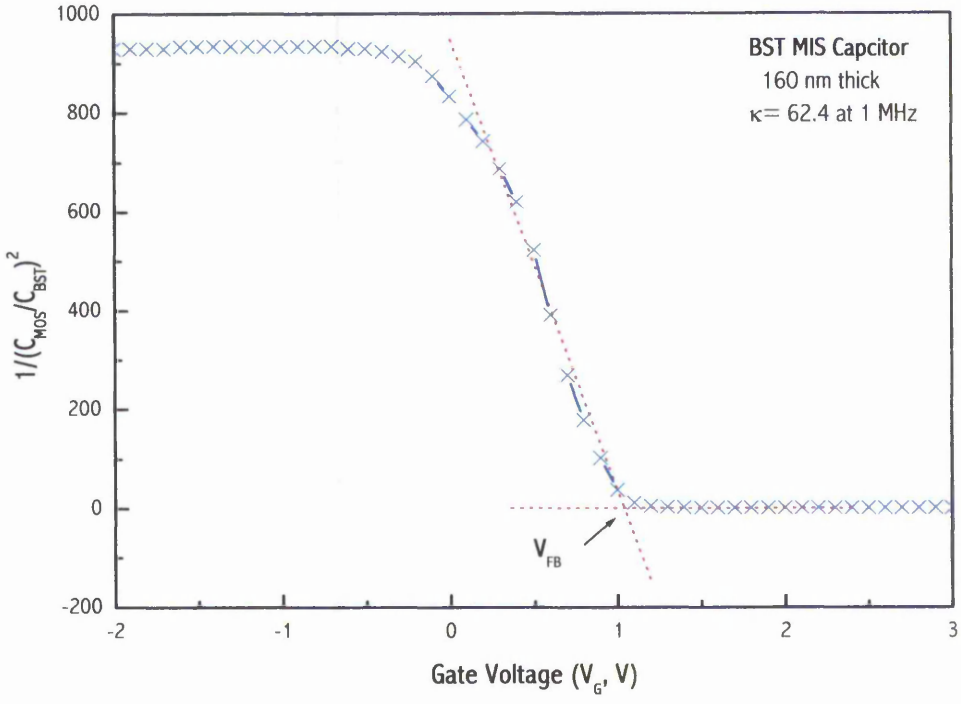


Figure 5-13 A new method for determining the flat band voltage from the plot of $1/C^2$ vs V_G. The flat band voltage is the lower knee point of the intersection of two dotted tangent lines.

The flat band voltage (V_{FB}) is one of the important parameters in investigating MIS devices. As mentioned above, a real device has deviation from the ideal device conditions because, basically, of the work function difference and various charges exist in the device. The introduction of charges and work function difference in the system causes image charges and a band bending of Fermi energy level (E_i) on the Si substrate surface. Thus, a gate bias should be applied for compensating the image charges and work function difference. To obtain more correct and reliable flat band voltage (V_{FB}) is critical in MIS devices. In the previous paragraph,

the flat band voltage is obtained from its capacitance (C_{FB}) simply. Another direct-and-rapid method (Hillard method) [65] for determining the flat band voltage will be examined in this section to verify the previous result.

The method is based on the sharp transition that occurs in the $1/C^2$ vs V_G. The capacitance can be normalized. Figure 5-13 shows a new normalised *C-V* curve from $1/(C_{MOS}/C_{BST})^2$ vs V_G. In the figure, the *x* component of lower intersection point of two dotted tangent lines is the flat band voltage ($V_G = V_{FB}$). From this method, the obtained flat band voltage is approximately 1.05 V. This value is slightly lower than the flat band voltage previously by around 5% difference, but the method is easy to use and a quite reliable for determining the flat band voltage. This Hillard method was applied to other devices with 100 nm thick BST layer (e.g., Figure 5-11). The flat band voltage obtained was approximately 0.97 ~ 1.01 V, which is shown in Figure 5-14.

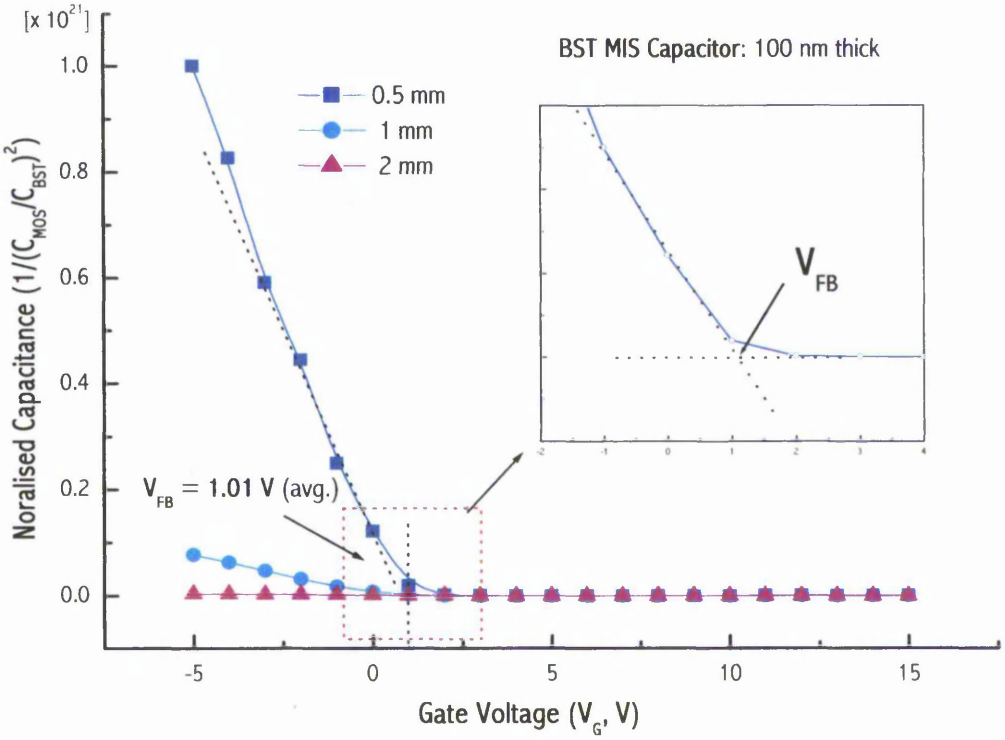


Figure 5-14 A graphical method (Hillard method) for determining the flat band voltage of MIS capacitors with 100 nm thick BST layer from Figure 5-11.

5.2.5 Frequency Effect and Instabilities at the Interface

In order to investigate the frequency dependence of MIS, or MFIS devices, various frequencies are applied to the device under test (DUT) during *C-V* characterisation. In general, in inversion condition, high frequency (HF) and low frequency (LF) *C-V* characteristics are different because charged carriers (e.g., mobile charges, ions, and etc.) in space charge regions of the devices cannot follow immediately to the response of applied high frequency so that in high frequency range (≥ 0.1 ~ 1 MHz), they cannot contribute to capacitance in inversion region. In low frequency, however, these carriers can move to the response of the frequency. Therefore, the *C-V* curve has frequency-dependent characteristics.

The *C-V* characteristic curves of BST MIS capacitors as a function of frequency is shown in Figure 5-15. In the observed capacitance response, there was no difference in inversion the range from 1 kHz to 1 MHz. In other words, the observed *C-V* characteristic curve did not exhibit a typical LF response at 1 kHz probe signal frequency.

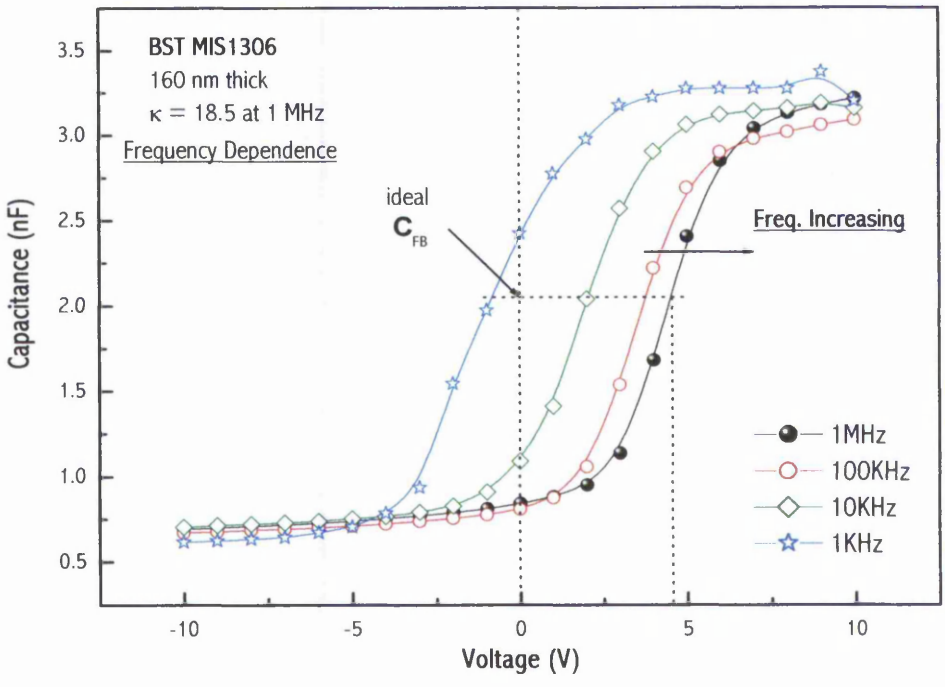


Figure 5-15 The frequency effect and voltage shift in *C-V* measurements

With increasing the frequency, the *C-V* curve patterns tend to shift to the right (i.e., positive bias). As discussed in the previous section, this shifting effect with high frequency can be explained by negative oxide charge at the interface between BST layer and the n-type Si substrate. Although the *C-V* characteristic curves did not show an LF feature in applied range of frequency, the flat band voltage showed a characteristic frequency dependence. Thus, the flat band voltage of *C-V* curve at 1 kHz was negative. Therefore, $\Delta V_{FB} (= V_{FB} - V_{FB(ideal)}) < 0$, which means a charge trapping in the film can be opposite from higher frequencies (10 kHz ~ 1 MHz)[61,66]. This frequency dependence is not understand clearly at this moment, so that it needs further study for analysing this effect.

The normalised ideal flat band capacitance (C_{FB}/C_{BST} at 1 MHz) of *C-V* curve in Figure 5-14 is 0.64, which is equivalent with capacitance of 2.05 nF (See Figure 5-14). From the Equations 5-1 and 5-2, the fixed oxide charge concentration per unit area (N_f) of this device is approximately 2.9×10^{12} Cm^{-2}, which has the same order with other devices mentioned in previous section.

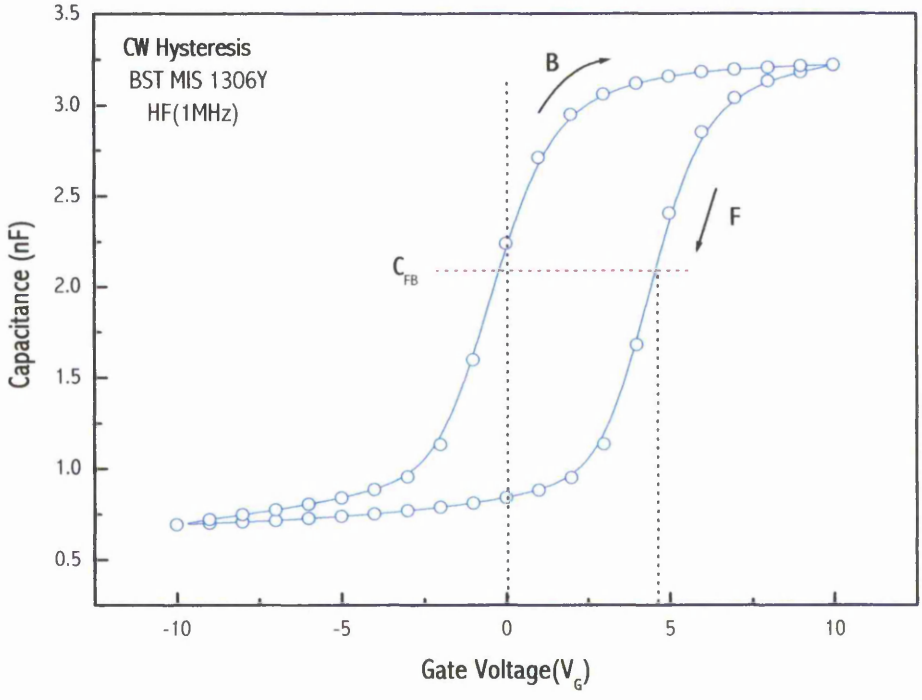


Figure 5-16 Dielectric hysteresis of MIS Capacitor with BST thin film under the high frequency of 1MHz: Clockwise(CW) Hysteresis.

The typical dielectric hysteresis of MIS devices is given in Figure 5-16. Regardless of high or low frequency, the hysteresis patterns with a clockwise direction are observed. As mentioned above, from the direction of the voltage shift of the *C-V* pattern, the polarity of the oxide charge can be determined. If reverse mode are considered as the ideal *C-V* curve (no oxide charge), the right shift of the *C-V* curve is caused by negative oxide charge. Due to the negative oxide charge, the *C-V* curve is shifted to more positive region. Drift of the oxide charges can be associated with tunnelling mechanism from the semiconductor to insulator states near the interface between the oxide layer and semiconductor.

5.2.6 Leakage current - Voltage Characteristics

Leakage current is one of the most important properties in BST thin films. Of course, leakage current or leakage current density is an important parameter to any dielectric material in microelectronic devices for evaluating the material. Various leakage current-density (J, A/cm^2) characteristic curves of BST thin films are observed and they are plotted in Figure 5-17. From current-voltage measurements, MIS capacitors with BST thin film layer showed low leakage current levels up to 80 V. The device can maintain low leakage current under maximum electric field conditions: < 1.58μA/cm^2. According to the criteria of selecting suitable dielectric material for TFEL devices, the observed value is satisfied with the conditions. In addition, the dielectric constant of BST layer with Si/BST/Al structure showed around 32.4 for 100 nm-thick BST thin films. Therefore, a figure of merit (FOM), or charge storage capacity (CSC) can be obtained as large as 22.95 μC/cm^2, which can be about eight times larger than the minimum requirement (3 μC/cm^2) of charge storage capacity for dielectric material in TFEL applications.

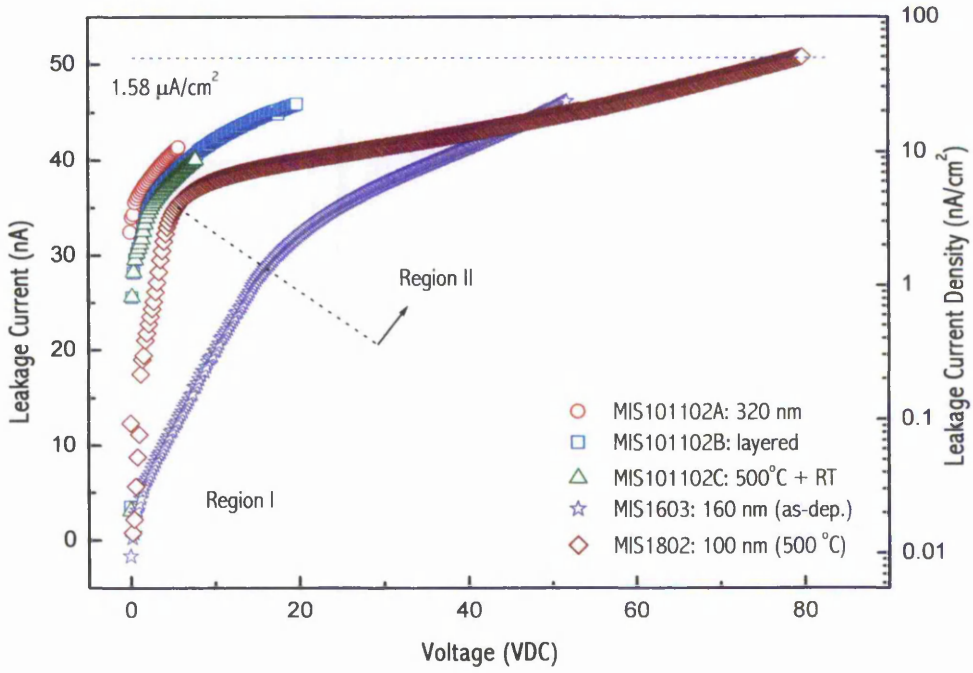


Figure 5-17 Average *I(J)-V* Characteristics of MIS capacitors with BST thin films. It shows relatively low leakage current density of lower than 1.58 μA/cm^2 until 80 V.

These *I-V* curves of Figure 5-17 exhibited non-linear characteristics, which can be explained generally by an electrode-limited current conduction and a bulk-limited current conduction mechanism, respectively [67,68]. At the initial stage (region I, low electric field), an abrupt increase of current density is attributed to the electrode-limited current conduction (tunneling, or Schottky effect) and then the bulk-limited current (Poole-Frenkel, Space charge limited or hopping conduction) is a dominant mechanism in a saturated (or quasi-saturated) regime (region II).

The conduction mechanism of BST thin films is still a controversial issue. Basically, the electron affinity (1.7 ~ 4.1 eV) of BST material is not determined correctly as mentioned earlier. Thus, it is difficult to develop the energy band diagram of Al electrode-BST- Si device. Thus, the energy band depends on work function of Al electrode (4.1 ~ 4.28 eV) and the electron affinity of BST material. In order to utilize BST thin film and understand it more clearly, it is necessary to establish the important parameters first. For a reference, an energy band diagram is illustrated in Figure 5-18.

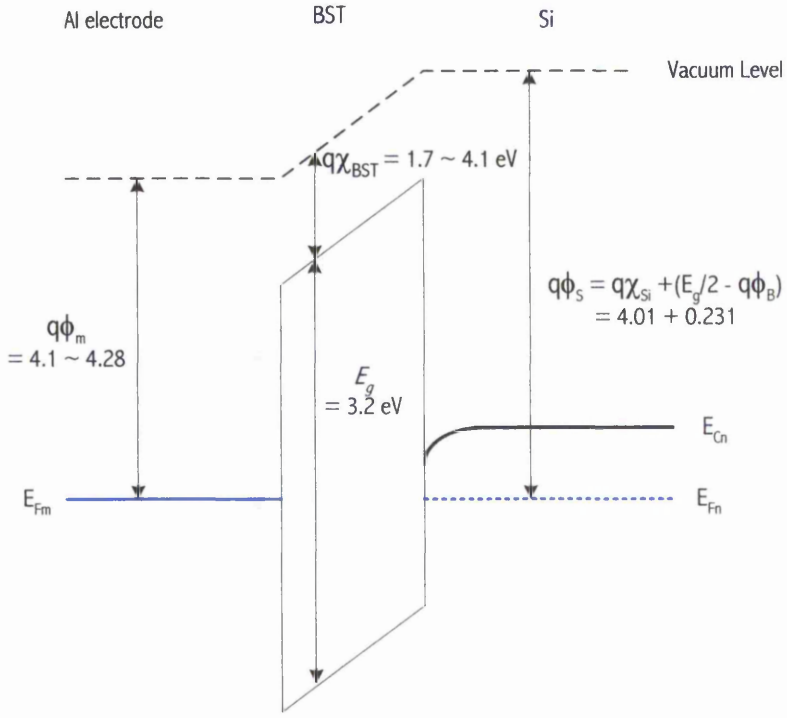


Figure 5-18 An estimated energy band diagram of Al-BST-Si(n-type) MIS devices

5.3 Summary and Conclusions

In order to utilize optical and dielectric properties of barium strontium titanate (BST) for TFEL devices, BST thin film was investigated by various experimental methods such as growth parameters, X-ray diffraction, Scanning Electron Microscopy(SEM), refractive index and capacitance (and current)-voltage characterization.

Optimum growth conditions for BST thin film were established for obtaining high quality thin films. The substrate temperature, sputtering pressure, oxygen content ratio, and rf power are 300-350 °C, 10 mTorr, 10% O_2, and 100 W, respectively (See Figure 5-2). In addition, a post-thermal annealing temperature of 500 ~ 700 °C is inevitable to improve crystallinity and optical properties of BST thin film. Improved crystallinity of BST thin film as a function of the annealing temperature was confirmed by X-ray diffraction patterns analysis. Grown BST thin film on Si substrate had a (110) and (111) preference, which mean a cubic structure. Generally, deposited BST thin films for this study showed (111) orientation preference, which can be explained by BST thin films rotating by 45 degree to minimize internal distortion from a lattice mismatch between BST film and Si substrate.

Barium strontium titanate thin films showed a wide range of refractive index from 2.09 ~ 2.47 by various growth conditions. In particular, the refractive index of BST thin film heavily depended on the substrate temperature. In addition to that, a colour chart of BST thin films as a function of thickness (approximately, 80 ~ 320 nm) was established from this research. BST film thickness estimated by using *in situ* interferometric and refractive index was confirmed physically by scanning electron microscopy (SEM) and a stylus profiler.

Laser annealed BST thin film exhibited the highest refractive index (~ 2.42) at a certain thickness only. This value is comparable to the substrate temperature of 700 °C while laser annealing processes can affect BST film thickness. BST thin film thickness showed a decrease approximately up to 40 nm by a spectral interference technique after laser annealing treatment with laser fluence of 300 mJ/cm^2 and 10 pulse irradiation (max.).

A relationship between dielectric constant of BST thin films and their film thickness (or electrode diameter) was developed. Observed dielectric constant increased by a multiple of 1.43 in thickness and decreases by a ratio of 1.26 in electrode area.

By capacitance-voltage characterization, a rigid parallel shift to the positive voltage was observed. This rigid parallel shift from the ideal *C-V* curve is attributed to fixed oxide charges at the interface vicinity between BST thin film and the Si substrate. In general, these fixed oxide charges are positive, but the oxide charge was negative from the shifting direction of *C-V* curve at high frequency (1 MHz). Estimated fixed oxide charge concentration per unit is 2.9 ~ 3.49 × 10^{12} cm^{-2}. A quick and simple method (Hillard method[65]) was applied for determining a flat band voltage (V_{FB}) of MIS devices. The obtained flatband voltage showed approximately 5% difference from a calculated flat band voltage by an ideal capacitance ($C_{FB(ideal)}$).

C-V characteristic curves as function of frequency were investigated. Observed *C-V* curves showed typical *C-V* characteristics – accumulation, depletion and inversion regions from positive to negative bias. Characteristic *C-V* curves shifted to the positive bias region from the flatband capacitance of ideal *C-V* curve. On the contrary, at lower frequency (1k ~ 10k Hz) the *C-V* curves were tending to move to an opposite direction. As a result, the *C-V* curve at 1 kHz moved to the negative region. Thus, the flatband voltage of the MIS device can change from positive to negative.

Leakage currents of BST thin films were as low as 1.58μA/cm^2 at 80 V. Thus, the breakdown strength field (E_{BD}) of rf sputtered BST thin film (100 nm thick) was of 8 MV/cm (max). A conduction mechanism of MIS device with BST thin films can be separated by an initial low and a high electric field. Thus, a rapid increase in leakage current under low electric field is governed by electrode-limited current conduction mechanism. At the higher electric field region, the current density tends to be saturated, which implies a bulk-limited current conduction mechanism can be dominant in that regime.

A charge storage capacity (CSC) for evaluating dielectric material was obtained. In general, a minimum requirement of the charge storage capacity for selecting the dielectric of TFEL devices was known as 3 μC/cm^2. A 100 nm-thick BST thin film (κ = 32.4) showed 8 times (=

22.95 μC/cm²) higher than the requirement, which means BST thin films have good feasibility as a cladding material for TFEL devices.

Capacitance – Voltage (*C-V*) characterisation of laser annealing BST thin film was performed for investigating laser annealing effects on MIS devices as a function of film thickness. X-ray diffraction patterns (70 pulses irradiated with 300 mJ/cm²) implied improved BST thin films, but unlike expectation, *C-V* characterisation of laser annealing BST thin films was not successful. Interestingly, observed *C-V* curves did not show a typical *C-V* characteristic curve. Therefore, it was not possible to undertake the experiments. Regarding laser annealing on BST thin film, it is necessary to have additional consideration in identifying important factor for utilising BST thin film. Actual laser fluence of 300 mJ/cm² (KrF λ = 248 nm) and maximum 10 pulse irradiation was applied to the samples for *C-V* characterisation.

REFERENCES

[1] Kim, T. S., et al, Electrical properties of radio frequency magnetron-sputtered (Ba, Sr)TiO_3 thin films on indium tin oxide-coated glass substrate, Journal of Vacuum Science and Technology, A 12(2), 1994

[2] Kimura, Hidekazu, XAFS studies on (Ba, Sr)TiO_3 Thin Films, Fundamental Research Lab., NEC Corporation, Japan

[3] Lines, M. E. and Glass, A.M, *Principles and Applications of Ferroelectrics and Related Materials*, Clarendon, Oxford University Press, 1977

[4] Lee, J. Y. and Lai, B. C., The electrical properties of high-dielectric-constant and ferroelectric thin films for very large scale integration circuits (from *Handbook of Thin Film Materials* by Nalwa, H.S (ed.)), pp. 1-98, Academic Press, 2002

[5] Wechsler, B.A. and Kirby, K.W., Phase Equilibria in the System Barium Titanate-Strontium Titanate, Journal of American Ceramic Society, Vol. 75, No. 4, pp. 981-984, 1992

[6] Kotecki, D. E. et al., (Ba, Sr)TiO_3 dielectric for future stacked-capacitor DRAM, p. 367, 43(3), IBM J. Res. Develop, 1999

[7] Ramesh, R. *Thin Film Ferroelectric Materials and Devices*, Kluwer, 1997

[8] Kingon, A.I. et al., High-Permittivity Perovskite Thin Films for Dynamic Random-Access Memories, MRS Bulletin, Vol. 21, No. 7, pp.46-52, July 1996

[9] Dey, S. K. and Alluri, P.V., PE-MOCVD of Dielectric Thin Films: Challenges and Opportunities, MRS Bulletin, Vol. 21, No. 6, pp. 44-48, June 1996

[10] Cole, M. W. et al., Structure-property relationships in pure and acceptor-doped $Ba_{1-x}Sr_xTiO_3$ thin films for tunable microwave device applications, Journal of Applied Physics, Vol. 92, No. 1, p. 475, 2002

[11] Scott, J.F. et al., Structure and Device Characteristics of $SrBi_2Ta_2O_9$-Based Nonvolatile Random-Access Memories, MRS Bulletin, Vol. 21, No. 7 pp.33-39, 1996

[12] Bernacki, Thomas A. et al., Barium Strontium Titanate Thin-Film Multi-Layer Capacitors, Passive Component Industry, p. 11, 2004

[13] Biharaj, B. et al., Journal of Applied Physics, Vol. 76, No. , p. 1169, 1994

[14] Polla, D. L. and Francis, L.F., Ferroelectric Thin Films in Microelectromechanical Systems Applications, MRS Bulletin, Vol. 21, No. 7, pp. 59-65, 1996

[15] Nalwa, Hari Singh, *Ferroelectric and Dielectric Thin Films (Handbook of Thin Film Materials, Vol. 3)*, Academic Press, 2002

[16] Nalwa, Hari Singh *Handbook of Low and High Dielectric Constant Materials and Their Applications, Vol. 1-2*, Academic Press, 1999

[17] Paz de Araujo, C. A. et al., *Ferroelectric Thin Films: Synthesis and Basic Properties*, Gordon and Breach, 1996

[18] Lee, Y-H. et al., Comprehensive Understandings on the High Dielectric Constant Insulating Layers for Alternating-Current Thin Film Electroluminescent Devices, , IEEE Trans. Electron Devices, vol. 48(4), p.653,2001

[19] Song, M. H. et al., Effects of a new stacking method on characteristics of multilayered $BaTiO_3$ thin film, Journal of Applied Physics, 79(7), p. 3744, 1996

[20] Konofaos, N. et al., Properties of Al-$SrTiO_3$-ITO Capacitors for Microelectronic Device Applications, IEEE Trans. Electron Devices, Vol. 51 (7), p. 1202, 2004

[21] Evangelou, E.K. et al., Characterisation of the $BaTiO_3$/p-Si interface and applications, Applied Surface Science, Vol. 166, p. 504, 2000

[22] Evangelou, E.K. et al., Characterisation of $BaTiO_3$ thin films on p-Si, Materials Science and Semiconductor Process, Vol. 4, p. 305, 2001

[23] Kim, T. S. et al, The effect of buffer layer on the structural and electrical properties of (BaSr)TiO_3 thin films deposited on indium tin oxide-coated glass substrate by using a rf magnetron sputtering method, Journal of Applied Physics, Vol. 76, No. 7, 1994

[24] Kim, T. S. et al, Structural and electrical properties of rf magnetron-sputtered $Ba_{1-x}Sr_xTiO_3$ thin films on indium-tin-oxide-coated glass substrate, Journal of Applied Physics, Vol. 75. No. 12, 1994

[25] Kim, T. S. et al., Influences of Indium Tin Oxide Layer on the Properties of RF Magnetron-Sputtered (BaSr)TiO_3 Thin Films on Indium Tin Oxide-Coated Glass Substrate, Japanese Journal of Applied Physics, Vo. 32, Part 1 No. 6A. pp. 2837-2841, 1993

[26] Kim, T.S. et al., The thickness dependence of $(Ba_{0.5}Sr_{0.5})TiO_3$ thin films deposited on indium tin oxide-coated glass substrate using r.f. magnetron sputtering, Thin Solid Films, Vol. 254, pp. 273-277, 1995

[27] Alt, P.M, Proceeding of Society for Information Display (SID), Vol. 25, p. 123, 1984

[28] Nayak, N. et al., High-Permittivity (Ba,Sr)TiO_3 Thin Films (from *Handbook of Thin Film Materials*, p. 99, edited by Nalwa, H.S.), Academic Press, 2002

[29] Tcheliebou, F. et al., On the microstructure and optical properties of $Ba_{0.5}Sr_{0.5}TiO_3$ films, Thin Solid Films, Vol. 299, pp. 14-17, 1997

[30] Samantaray, C. B. et al, Effect of post0deposition annealing on microstructural and optical properties of barium strontium titanate thin films deposited by r.f. magnetron sputtering, Journal of Materials Science: Materials in Electronics, Vol. 12, pp. 365-370, 2001

[31] Thielsch, R. et al., Structure-related optical properties of laser-deposited $Ba_xSr_{1-x}TiO_3$ thin films grown on MgO(001) substrates, Thin Solid Films, Vol. 301, pp. 203-210, 1997

[32] Panda, B. et al., Optical properties of RF sputtered strontium substituted barium titanate thin films, Thin Solid Films, Vol. 332, pp. 46-49, 1998

[33] Pasierb, P. et al., Structural and optical properties of $Sr_{1-x}Ba_xTiO_3$ thin films prepared by rf sputtering, Thin Solid Films, Vol. 324, pp. 134-140, 1998

[34] Chen, W.K. et al., Study of linear and nonlinear optical properties of distorted Ti-O_6 perovskite structure in $Ba_xSr_{1-x}TiO_3$, Journal of Physics and Chemistry of Solids, Vol. 61, pp. 969-977, 2000

[35] Hellwege, K. H and Hellwege, A.M., Ferroelectrics and Related Substances: Oxides, 2nd Ed. p. 540, Springer, 1981

[36] Lawless, W.N. and Devies, R.C., Accurate Determination of the Ordinary-ray Refractive index in BaTiO3, Journal of Applied Physics, Vol. 35, No. 9, pp. 2623, 1964

[37] Bond, W. L. Measurement of the Refractive indices of Several Crystals, Journal of Applied Physics, Vol. 36, No. 5, pp. 1674, 1965

[38] Wöhlecke, M. et al., Refractive index of $BaTiO_3$ and $SrTiO_3$ films, Journal of Applied Physics, Vol. 48, No. 4, p. 1748, 1977

[39] Kim, T.S. *PhD Thesis* (in Korean), Korea Advanced Institute of Science and Technology(KAIST), South Korea, 1993

[40] Wang, Y.P. and Tseng, T. Y., Journal of Materials Science, Vol. 34, p. 3575, 1999

[41] Baumet, B.A. et al., Characterization of sputtered barium strontium titanate and strontium titanate-thin films, Journal of Applied Physics, Vol. 82, No. 5, p.2558, 1997

[42] Tanase, Tomokazu, et al., Dielectric properties of lead zirconate titanate thin films seeded with barium strontium titanate nanoparticles, Thin Solid Films, Vol. 471, pp. 71-75, 2005

[43] Kuo, Y. F. and Tseng, T. Y., Materials Chemistry and Physics, Vol. 61, p. 244, 1999

[44] Cranton, W. M. et al, Growth and dielectric characterization of yttrium oxide thin films deposited on Si by r.f.-magnetron sputtering, Thin Solid Films, Vol. 226, pp. 156-160, 1993

[45] Sze, S. M *Physics of Semiconductor Devices, 2nd Ed.* p 393. John Wiley and Sons, 1981

[46] International Centre for Diffraction Data(ICDD) Powder Diffraction File Data CD-ROM (PDF-2)or book Set # 42

[47] Kim, Dongsoo, Future Direction for a Diffusion Barrier in Future High-Density Volatile and Nonvolatile Memory Device, Critical Reviews in Solid State and Materials Sciences, Vol. 27 No. 3-4, pp. 143-226, 2002

[48] Matsubara, S. et al, Preparation of epitaxial ABO_3 Perovskite-type Oxide Thin Films on a (100) MgAl2O4/Si Substrate, Journal of Applied Physics, Vol. 66, No. 12, pp. 5826-5832, 1989

[49] Cook, L. P. et al., Microstructural Changes during Processing of Laser Deposited $BaTiO_3$ and PZT Thin Films, Proceeding MRS Symposium, Vol. 202, p. 241, 1991

[50] Campbell, S. A. *The Science and Engineering of Microelectronic Fabrication*, ch. 4, Oxford University Press, 1996

[51] Aguirre-Tostado, F.S. et al., Displasive phase transition in $SrTiO_3$ thin films grown on Si(001 Journal of Vacuum Science and Technology, A22(4), 1356 (2004)

[52] Yu, Z., et al, Epitaxial perovskite thin films grown on silicon by molecular beam expitaxy, Journal of Vacuum Science and Technology, B18, 1653 (2000)

[53] Shye, Der-Chi, et al., The Effects of Post Excimer Laser Annealing on $(Ba,Sr)TiO_3$ Thin Films at Low Substrate Temperature, Japanese Journal of Applied Physics, Vol. 42, Pt. 1, No. 4A, pp. 1680-1685, 2003

[54] Becker, Robert Jürgen, ***PhD Thesis***: Oxygen Vacancies in Barium Strontium Titanate Thin Films, Stanford University, 2002

[55] Baldus, O. and Waser, R., Laser crystallization studies of barium strontium titanate thin films, Journal of the European Ceramic Society, 24, pp. 3013-3020, 2004

[56] Xia, Y. et al, Enhanced tuning properties of (Ba,Sr)TiO_3 bilayer thin films formed by rf magnetron sputtering, Journal of Physics D: Applied Physics, 37, 2256 (2004); Ichinose, N. et al, Preparation and Rapid Thermal Annealing Effect of (Ba,Sr)TiO_3 Thin Films, Japanese Journal of Applied Physics, Vol. 34, Part 1, 9B, 5198 (1995)

[57] Greve, David W., *Field Effect Devices and Applications – Devices for Portable, Low-Power, and Imaging Systems*, Chapter 3, Prentice-Hall, 1998

[58] Neamen, Donald A. *Semiconductor Physics and Devices: Basic Principles*, Chapter 12, Irwin, 1992

[59] Sze, S. M., *Physics of Semiconductor Devices, 2nd Ed.* pp 390-391, John Wiley, 1981

[60] Nicollian, E. H. and Brews, J.R., *MOS (Metal Oxide Semiconductor) Physics and Technology*, John Wiley, 1982

[61] Schroder, Dieter K., *Semiconductor Material and Device Characterization*, Chapter 6, John Wiley, 1990

[62] Scott, J.F., *Ferroelectric Memories*, Springer-Verlag, 2000

[63] Dietz, G.W. et al., Journal of Applied Physics, Vol. 82, p. 2359, 1997

[64] Hwang, C.S. et al., Applied Physics Letters, Vol. 71, p. 371, 1997

[65] Hillard, R. J. et al, Direct and Rapid Method for Determining Flatband Voltage from Non-equilibrium Capacitance Voltage Data, (from Proceedings of the symposium on *Diagnostic Techniques for Semiconductor Materials and Devices* by Benton J. L et al. (Eds.)), Vol. 92-2, p. 261, The Electrochemical Society, Inc., 1992

[66] Kundu, T. et al., Electrical Techniques for the Characterization of Dielectric Films, Interface, p. 17, The Electrochemistry Society, Fall, 2005

[67] Screenivas, K. et al., Structural and Electrical Properties of rf-Sputtered Amorphous Barium Titanate Thin Films, Journal of Applied Physics, Vol. 62, No. 11, pp. 4475-4481, 1987

[68] Salama, C.A.T. and Siciunas, E., Characteristics of rf-Sputtered Barium Titanate Films on Silicon, Journal of Vacuum Science and Technology, Vol. 9, No. 1, pp. 91-96, 1972

CHAPTER 6
Electro-Optical Characterisation and Analysis of TFEL Devices

Overview

In this chapter, the electro-optical characterisation of fabricated TFEL devices will be discussed in detail for evaluating inorganic full EL devices. In addition, the electro-optical properties of EL device's lateral (or, edge) emission are included. According to phosphor materials, there are two main types of fabricated TFEL devices to be discussed here. In the first part of this chapter, the experimental results and analysis of ZnS-based (ZnS:Mn, yellowish orange emitting phosphor) TFELs with barium strontium titanate and other insulating layers will be the main topic. In the second part, the electroluminescence(EL) and photoluminescence(PL) properties of blue-emitting SrS-based(SrS:Cu,Ag) TFEL devices with yttrium oxide insulating layers are discussed. In addition, laser annealing effects on performance of full TFEL devices is presented – a ZnS-based EL(BST layer was laser-annealed) and a SrS-based EL (phosphor layer was laser-annealed). The electro-optical characterisations include luminance (*B-V* or *L-V*) (for BST), luminescence – electroluminescence (EL) and photoluminescence (PL), external charge-voltage (Q_{ext}-V), dynamic capacitance-voltage (*C-V*), internal charge-phosphor field (Q_{int}-F_p) and luminous efficiency-voltage (η-V).

6.1 Introduction

For inorganic (AC)TFEL devices, there are two critical issues to be mentioned. ① The lack of an efficient blue phosphor material has been a critical drawback to the realisation of full-colour inorganic TFEL display devices for many years. ② The layers need to be optimised with a high dielectric constant and good breakdown properties to improve the EL device' operational stability and to reduce the device threshold voltage to generate light emission more efficiently. Ultimately, the goal of reducing the device threshold voltage to operate the TFEL device leads to overall reduced power consumption and helps to realise cost-

effective displays devices. Therefore, study of high dielectric constant material and blue-phosphor material for inorganic TFEL devices are of high significance for full-colour commercial-purpose displays. To address this, alkaline-earth sulphide(AES) phosphor material with copper and silver co-doped - SrS:Cu,Ag and perovskite-structure (Ba,Sr)TiO_3 with complete solid solution properties have been studied for improving efficiency of blue-emitting active layer material and reducing driving voltage of the devices, respectively.

Once full ACTFEL devices are fabricated, electro-optical characterisation is the fundamental technical method for evaluating the devices. The electro-optical properties of EL device's lateral(or, edge) emission are also included. In fact, luminance loss within the devices is quite large when only a surface emission is used in applications, which is well known[1,2]. In other words, lateral emission can be brighter than the surface emission. Thus, the importance of edge emission is to take advantage of approximately 90% of total emission from the device due to the ACTFEL's intrinsic waveguide structure. However, the surface-emission property is preferable over edge emission in general-purpose display devices such as FEDs, PDPs and LCDs due to ease of fabrication.

Generally, the important parameters for engineering the characteristics of the ACTFEL devices can be summarised as follows[3]:

① dielectric coupling of the phosphor and insulator layers
② charge states of the insulator/phosphor interface as source of electrons
③ crystalline quality of the phosphor layer which determine the carrier transport
④ efficiency of the luminescent centres and charge transfer in multiple activators
⑤ stability of the individual layers and the device in operation

Based on the important parameters suggested above, the electro-optical properties of full TFEL devices with BST or yttrium oxide layers will be discussed.

6.2. Electro-Optical Characterisation of ZnS:Mn TFEL Devices

6.2.1 External Charge-Voltage(Q_{ext}-V)

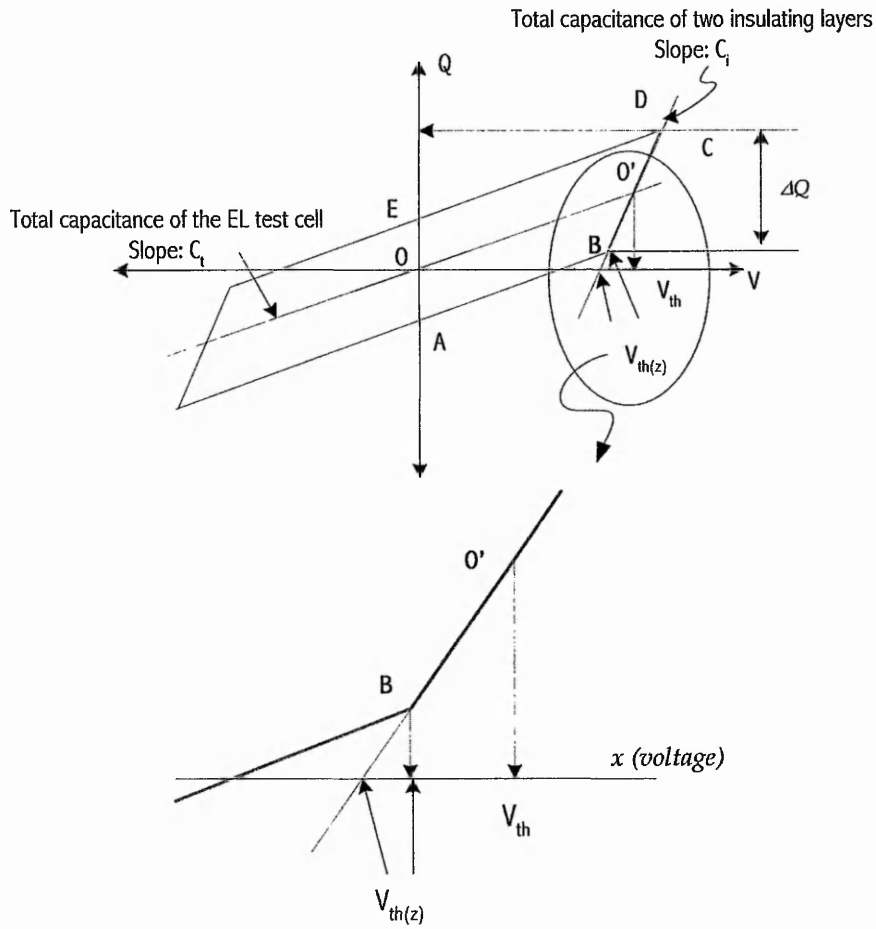
The relationship of transferred charge and applied voltage(***Q-V***) is one of the important characterisations in TFEL devices, where the transferred charge refers to the external total charges delivered to the test EL device. This Q-V measurement has been a commonly performed as a basic characterisation technique[4,5,6,7] to understand the electrical characterisation of the EL devices when the devices were in operation. With the same EL measurement setup - Sawyer Tower Circuit[8,9,10] - which is described in Figure 3-17(also see Figure 6.3), the Q-V curve is a measure of transferred charge to the test EL cell/device using a sense(or reference) capacitor, which is connected to the EL device in series. Therefore, the external charge across the EL device is calculated from the following relation: $Q_{ext}(=Q_{external})=C_{sense}v_s(t)$. The Q-V curve shows the external charge as a function of the applied voltage for the EL test device.

The Q-V loop has a counter-clockwise direction with respect to time so that it starts from the point **A** at zero bias in Figure 6-1. The section **A-B** of the Q-V loop exhibits a status of the test EL device when the applied voltage is lower than the threshold voltage of the device. The slope of the section (**A-B**) represents the total capacitance of the device, which means the equivalent capacitance of two insulating layers (capacitors) and phosphor layer in series connection. When the applied bias becomes greater than the threshold voltage ($V_{th(z)}$), the Q-V loop represents another line with a different slope. This is for the segment **BO'CD** and the slope of this section means total capacitance of two insulating layers only. At this point, the phosphor layer is virtually a short circuit in the optical point of view due to light emission.

More precisely, if the applied voltage is lower than the threshold or turn-on voltage, the real waveform on the oscilloscope is a straight line passing through the origin of the coordinate and then the line is expanding up and downside simultaneously to make a closed loop like a parallelogram shape as the applied voltage increases and finally is greater than the threshold voltage. The short line on the section **O-O'** in Figure 6-1 and 6-2

shows the status that the applied voltage is lower than the threshold voltage. The slope of the section(O-O') is the same of the slope of the section **A-B** or **D-E**.

When two straight lines meet each other, the x component of the line joining point (point **B**) will be the threshold voltage of phosphor layer[6,11,12], while the intercept point of imaginary extension of the line **BO'CD** on the x axis (voltage) can be the turn-on (threshold) voltage as well[6]. Actually, two threshold voltages may be a little different in magnitude, but it is not significant. Of course, these two voltages can be the same in given conditions. Therefore, in the chapter, the two threshold voltage will be treated as one.



The Q-V waveform has a counterclockwise direction from A and then back to A for an entire loop

Figure 6-1 An ideal Charge-Voltage (Q-V) characteristic parallelogram when $V_a > V_{th}$ and the graphical definitions of the threshold voltages, V_{th}, and $V_{th(z)}$, respectively.

Practically, the measured Q-V loop has some distortion in the section C-D, which corresponds to the relaxation charge when the applied voltage is steady state, but the external charge increases up to the maximum (point D). As the applied voltage decreases, the external charge reduces accordingly. The slope of this region (D-E) is expected to be the same of the first one, the section **A-B**. Because the applied bias is less than the threshold voltage, the phosphor layer can act a normal capacitor again. This is for the positive half cycle. When the polarity of the applied voltage changes, the rest half of the loop goes with the same way.

The difference in charge between point **B** and point **D** is defined for the conduction charge, $Q^{+}_{conduction}$, which is the amount of transferred charge (ΔQ) for the positive half cycle. At zero bias (point E), there may be a difference in magnitude of charge between positive and negative applied voltage. The charge difference is known as the leakage charge, $Q^{+}_{leakage}$. The leakage charge is due to the field created from the previous applied voltage and the existence of interface charge at the boundary between the phosphor and insulator layers[13]. The leakage charge is not shown in Figure 6-1. A typical Q-V loop is given in Figure 6-2.

Additionally, there is another threshold voltage for the EL device. When the section **O-O'**(dotted line), which is the same slope of the section **A-B**(the total capacitance of the test EL device) intersects with the straight line of the section **B-D**, the x component(i.e., voltage) of the point(O') is known for the threshold voltage of the device[6,11,12]. Thus, the phosphor threshold voltage ($V_{th(z)}$) can have the following equation by a voltage divider rule in capacitor circuit,

$$V_{th(z)} = \frac{C_{insulators}}{C_{insulators} + C_{phosphor}} V_{th} \qquad \textbf{Equation 6-1}$$

The Equation 6-1 means V_{th} is the applied voltage to the entire EL device and $V_{th(z)}$ is the partial voltage of the phosphor layer by the voltage divide principle. The capacitance of the phosphor layer, C_p, is obtained by a simple relation of the series connection of capacitors. The capacitance can be expressed as

$$\frac{1}{C_p} = \frac{1}{C_{total}} - \frac{1}{C_{insulators}} \qquad \text{Equation 6-2}$$

or,

$$C_p = C_{ZnS:Mn} = \frac{C_t \times C_i}{C_i - C_t}, \qquad \text{Equation 6-3}$$
$$(C_i \equiv C_{insulators}, C_t \equiv C_{total})$$

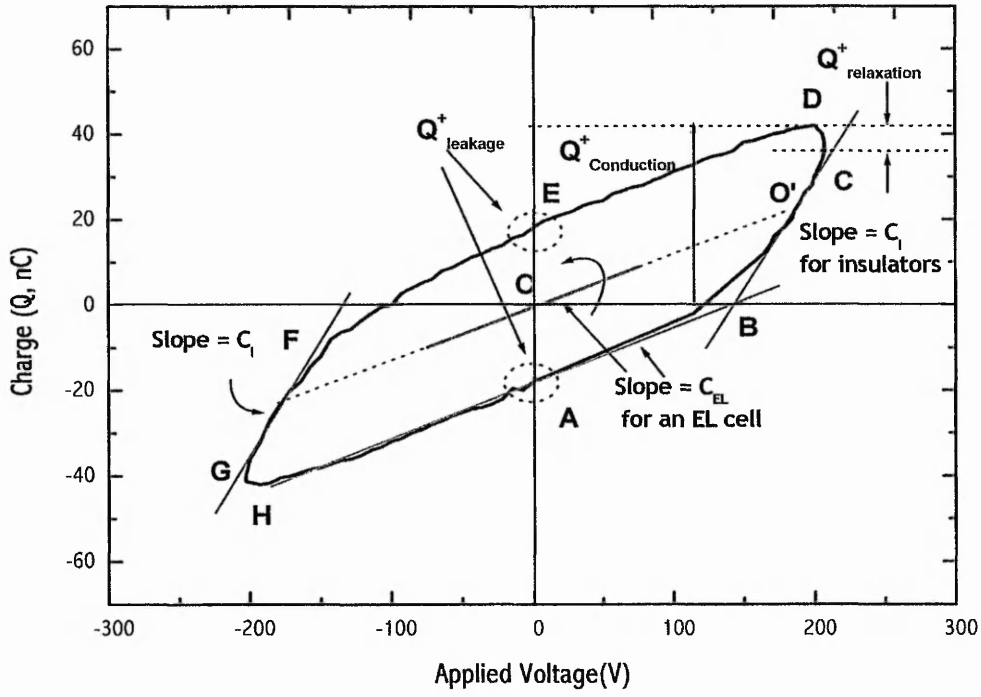


Figure 6-2 Transferred external charge($Q_{external}$-V) waveform of a ZnS:Mn TFEL with BST layer when a sine wave is applied. The waveform generally traces out a counterclockwise direction from point A and finally come back to the point A for the entire loop.

6.2.2 Dynamic Capacitance - Voltage(*C-V*) Characterisation

A dynamic capacitance-voltage(*C-V*, or C_D-*V*) is based on the equation of $Q_{ext} = C_{EL} v_{EL}(t)$ from $Q_{ext} = C_{sense} v_s(t)$ in *Q-V* characteristics. Therefore, its capacitance can be rewritten as:

$$C_D \cong \frac{\Delta Q_{external}}{\Delta v_{EL}} = \frac{dQ_{ext}}{dv_{EL}} = \frac{dQ_{ext}/dt}{dv_{EL}/dt} = \frac{i(t)}{\frac{dv_{EL}}{dt}} = \frac{i(t)}{d(v_a - v_s)/dt} \qquad \textbf{Equation 6-4}$$

$$(Q_{external} \equiv Q_{ext};\ v_{EL} = v_a - v_s)$$

where, $i(t) = v_s / R_s$ and $v_{EL}(= v_a - v_s)$ means the actual applied voltage to the test EL device after the voltage drop due to the EL test cell in Figure 6-3, which is a simplified Sawyer-Tower circuit[5,7,8,10] from Figure 3-17, Chapter 3.

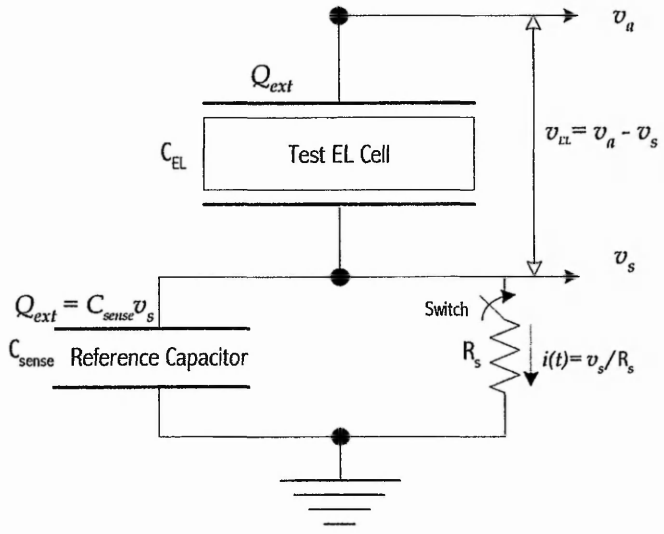


Figure 6-3 A simplified Sawyer-Tower Circuit from Figure 3-17 for a dynamic *C-V* curve and the definitions of voltages at terminals; v_a, v_s, and v_{EL}.

The *C-V* characterisation can provide further information on capacitance components of the test EL devices. In addition, the *C-V* curve has different meaning from the general

relation of the parallel plate capacitor, $C = \frac{\varepsilon_0 \varepsilon_r A}{d}$, where ε_0 is permittivity of vacuum, ε_r relative permittivity of dielectric material, A the area of the capacitor, and d the thickness of the dielectrics, respectively. Without knowing the physical parameters of the materials, the *C-V* curve can be obtained from differentiating the *Q-V* curve simply. In other words, C_{EL} is not fixed, but depends on the applied voltage. According to the magnitude of the applied voltage, the capacitance of the phosphor layer is changing accordingly. That is why it is called a dynamic capacitance.

A typical *C-V* curve has two plateaus for a double insulator standard structure EL device. The lower(minimum) plateau represents the total capacitance of the EL cell and the upper(maximum) one shows the total capacitance of two insulators only. If the EL device has double phosphor layers structure such as ZnS:Mn/SrS:Ce for full colour devices, the three plateaus are displayed according to the capacitance of the each layer within the devices[4,13,14]. The dynamic capacitance of ZnS:Mn TFEL with BST and Y_2O_3 layer as a function of applied voltage is shown in Figure 6-4.

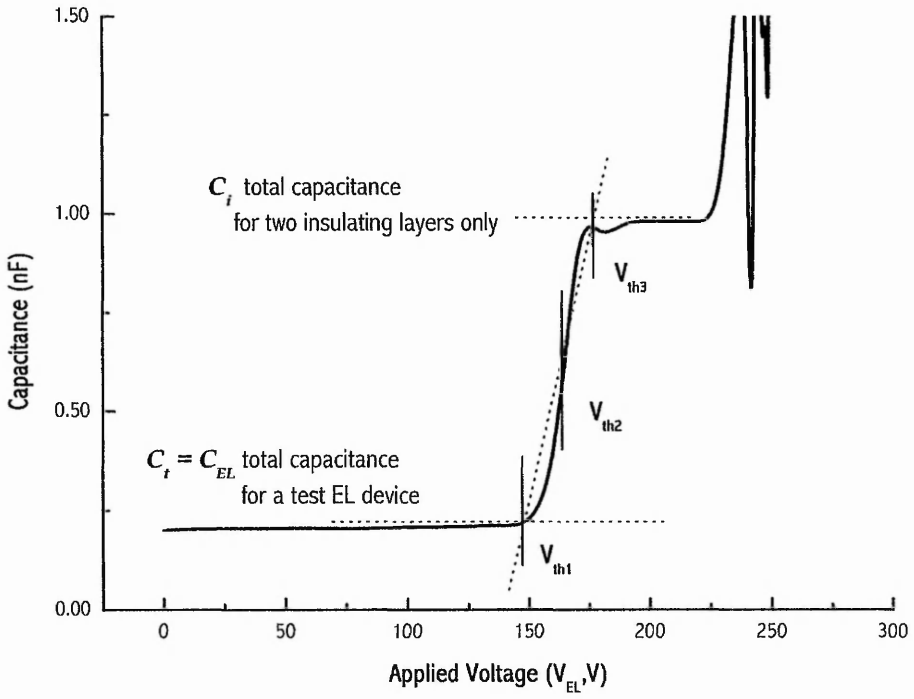


Figure 6-4 A real dynamic capacitance vs voltage (*C-V*) curve of ZnS:Mn TFEL device. For more details, refer to Figure 6-12 in Section 6.3

There are three different definitions of the threshold voltages in C-V curve in Figure 6-4. These are possible corresponding to the onset of the transition, the midpoint of the transition, and the saturation of the transition in which the capacitance is exclusively that of the insulator capacitance, where V_{th1}, V_{th2}, and V_{th3} are denoted, respectively[3,4,13,14]. V_{th1} might be attributed to the onset of light emission of electrons from shallow interface traps. For V_{th3}, it can be correspond to the initiation of field clamping state. Therefore, V_{th2} is most likely to be the actual threshold voltage for the device and the value is close to the threshold voltage defined from Q-V loop. Also, this is similar to the situation like the definitions of V_{th} and $V_{th(z)}$ mentioned in previous section which has some ambiguity according to researchers.

6.2.3 Internal Charge-Phosphor Field (Q_{int}-F_p) Characterisation

Two important electrical characterisation techniques - Q-V and C-V - mentioned above focus on the external charge for the entire EL devices. In order to understand internal information of the EL cell better, we need additional characterisation techniques to investigate it. Generally, this is called Q-F_p characterisation, which is the internal charge of the test device and this internal charge is expressed as a function of the phosphor field. The physical meaning of Q-F_p is based on the following two equations, Equation 6-5 and Equation 6-6[4,7,13]:

$$q_{int}(t) = \frac{C_i + C_p}{C_i} Q(t)_{external} - C_p v(t)_{EL} \qquad \textbf{Equation 6-5}$$

and

$$F_p(t) = \frac{1}{t_p}\left(\frac{C_{sence} v_s(t)}{C_i} - v(t)_{EL}\right) = \frac{1}{t_p}\left(\frac{Q(t)_{external}}{C_i} - v(t)_{EL}\right) \qquad \textbf{Equation 6-6}$$

where, C_i and C_p are total capacitance of two insulator layers and the phosphor layer, respectively and t_p the thickness of the phosphor layer.

Equation 6-5 means the internal charge within the phosphor layer. In the absence of space charge in the phosphor layer, Equation 6-6 is the instantaneous electric field in the phosphor layer and the first term within the parenthesis one the right side, $\frac{C_{sence} v_s(t)}{C_i}$, is just the voltage applied to the insulator, $v(t)_{insulator}$. Thus, a Q-F_p curve is obtained by plotting $q(t)$ vs $F_p(t)$. A general Q-F_p curve loop is shown in Figure 6-5 for a sample. The phosphor field(F_p) can have a simple form by the voltage divider principle capacitively in series capacitor connection as in Equation 6-7 below,

$$F_p(t) = \left(\frac{C_i}{C_i + C_p} \right) \frac{v(t)_{EL}}{t_p} \qquad \textbf{Equation 6- 7}$$

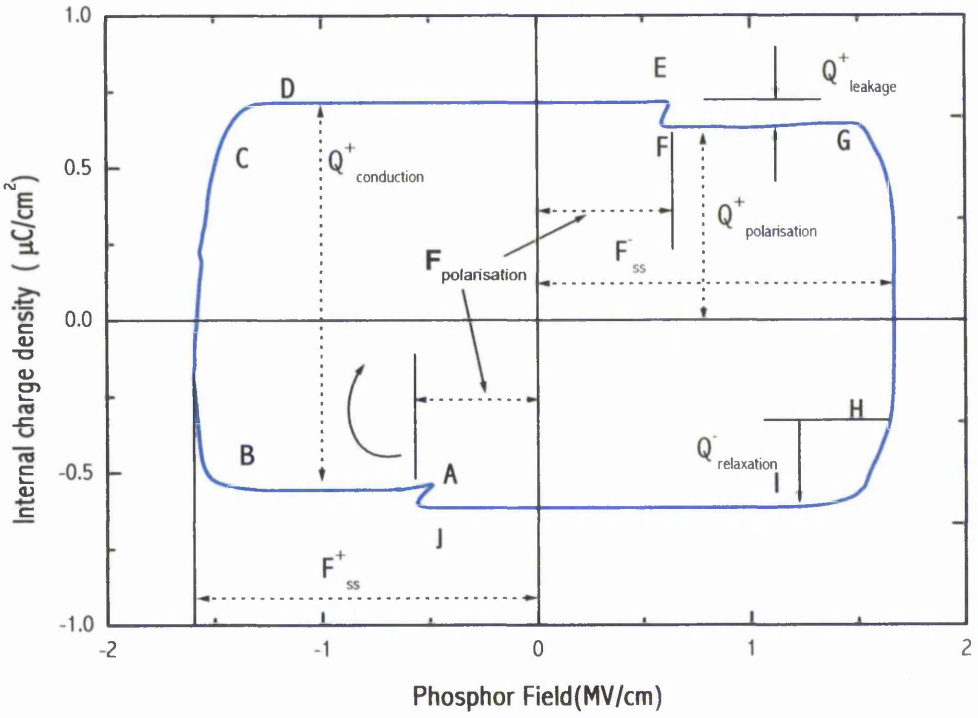


Figure 6-5 An internal charge density versus phosphor field intensity(Q_{int}-F_p) curve loop of a BZY TFEL device

Unlike the *Q-V* loop, The *Q-F*$_p$ curve has a clockwise direction and generally it starts at point **A**. The segment from point **A** to point **B** is the state when the applied voltage is lower than the threshold voltage. At point **B**, the device has the initiation of the internal conduction. From point **B** to **C**, the region is the steady state phosphor field ($\mathbf{F^{+}_{ss}}$) which is constant. Even though the applied voltage increases, the internal phosphor field is not affected. The applied voltage is the maximum from point **C** to **D**. The internal field decreasing during the region **C-D** results from the charge transfer and finally the phosphor field is relaxed. This is known as relaxation charge ($\mathbf{Q^{+}_{relaxation}}$). When the polarity changes, a counterpart relaxation charge (from point **H** to **I**) is shown in Figure 6-5 instead. As the applied voltage decreases (region **D-E**), the internal phosphor field goes to zero and changes its polarity. The phosphor field intensity (point **E** and point **J**) on both side from zero shows the polarization field ($\mathbf{F_{polarisation}}$). At zero bias, the charge difference between point **E** and **F** is known as the leakage charge. Therefore, several important internal parameters can be obtained from *Q-F*$_p$ characterization.

6.3. Results and Discussion

6.3.1 Lateral Emission Characteristics of ZnS:Mn TFEL Devices

As one of electro-optical characterisation of TFEL devices, brightness-voltage (*B-V*, or luminance-voltage(*L-V*)) measurements are performed as described in Chapter 2. The main focus of this measurement is to investigate the intensity of lateral emission and the threshold voltage of the devices as a function of applied voltage. In fact, the luminance-voltage (*L-V*) characterisation is a general measurement which is performed by measuring the output of light emission from the test EL cell. In this experiments, there are three different devices with different insulating layers on silicon substrates for comparison: BST/ZnS:Mn/BST(BZB), BST/ZnS:Mn/Y_2O_3(BZY), and Y_2O_3/ZnS:Mn/Y_2O_3(YZY).

The lateral emission characteristics of the BZY samples are shown in Figure 6-6. In Figure 6-6, the BZY and BZB devices did not show any substantial difference in the threshold voltage characteristics between these devices. However, in luminous intensity, the BZY device showed better than the BZB devices. In fact, the BZB devices are not fully saturated and decreased with the applied voltage. The BZB devices reach breakdown condition without showing full intensity. It can be estimated that the operational instability of the BZB devices might result from the intrinsic properties of perovskite-structure dielectric materials. Unlike other insulating materials, many perovskite structure insulating materials are well known for their breakdown mechanism as a propagating type[12]. This propagating mode in breakdown properties is that once dielectric breakdown begins locally, it tends to spread out catastrophically so that it affects the whole material or device. However, a self-healing mode is somewhat opposite concept from the propagating mode. Therefore, a device with the self-healing type dielectric material can have better operational stability under high electric field condition, particularly, in TFEL device applications. In fact, high dielectric constant dielectric materials exhibit normally relatively low breakdown strength. It is easily verified to investigate the basic relationship of dielectric constant and breakdown strength in Table 2-7, Chapter 2. At this point, BZY devices exhibited better brightness and stability than that of BZB devices. It seemed to correlate to not only dielectric material, but also device structures, electrodes and their

interface conditions. Therefore, it is necessary to carry on further study on this matter to analyse.

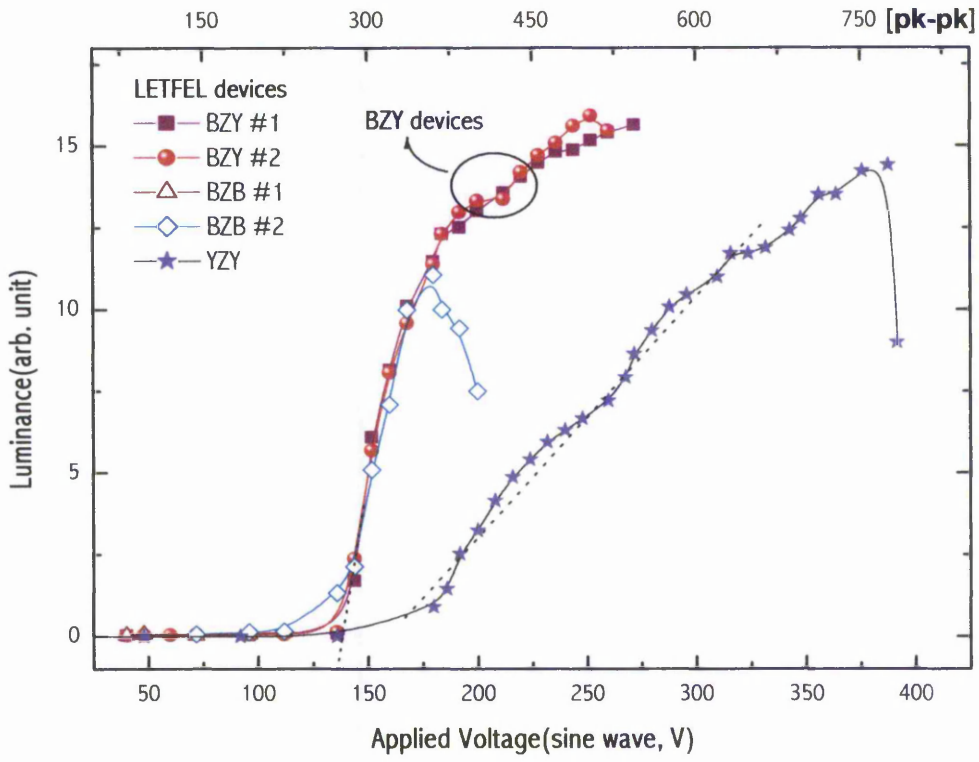


Figure 6-6 Luminance - Voltage(*L-V*) characteristics of the Lateral(edge) Emission TFEL devices(LETFELDs) with three different devices: BST-ZnS:Mn-Y_2O_3(BZY), BST-ZnS:Mn-BST(BZB), and Y_2O_3-ZnS:Mn-Y_2O_3(YZY). For BZY and BZB devices, the luminance is an arithmetic average value from 10 devices at 5 kHz, respectively. (Dotted lines are given for the slope, $\Delta L/\Delta V$)

For comparison purpose, the lateral emission characteristics of the YZY devices are investigated. The YZY devices have a monotonous increase trend in their luminous intensity and they can operate under the range of high driving voltage more than 700 peak-to-peak voltage (See Figure 6-6). This seems to be an example of the self-healing mode characteristics of yttrium oxide insulating material. As expected, the YZY devices have somewhat higher threshold voltage compared to the BZX(X= B or Y) devices by approximately 50 V. However, there is no significant difference between BZX and YZY

devices in their maximum luminous intensity. More important, when a fixed applied voltage, the BZY devices showed approximately up to four times the brightness of the YZY device at 200 V in *L-V* characteristic curve. In addition to that, the device turn-on characteristics are far better in BZX devices. The steepness of the slopes ($\Delta L/\Delta V$) of *L-V* curves in luminous intensity curves can be compared straightforwardly: BZX devices are steeper than that of the YZY device in its slope.

As mentioned before, high dielectric constant materials can reduce the device turn-on voltage and then to help to reach at the saturated luminance of the device at lower operating voltage. Compared to YZY devices, high-permittivity BST thin film in EL devices showed more effective in its turn-on and saturated luminance characteristics: lower turn-on voltage and the same level of luminance were achieved at lower driving voltage, which are the main purpose of using BST thin film in EL device application. Unlike barium titanate ($BaTiO_3$, BT), BST materials were known for stability in their structure and thermal conditions with high dielectric constant properties due to the effect of adding strontium titanate ($SrTiO_3$, ST) (see Figure 5-1) and a complete solid solution feature.

An additional monotonous increase in luminous intensity of the YZY devices is shown in Figure 6-7. Although annealing treatment was performed at high temperature (>= 5 ~ 700°C), the fabricated YZY devices did not exhibit ideal turn-on *L-V* characteristics. For the YZY devices, the turn-on voltage of the YZY devices is affected by the post-annealing treatment so that the voltage can be reduced largely according to annealing temperature. However, if the post-annealing temperature is above 500 °C, the *L-V* curve is not changed significantly. It is possible to understand that the device turn-on characteristics may not be changed much by a simple post-annealing treatment and heavily depends on materials and the interface state to contribute to emission. It is well known that the interface states between the insulator and phosphor layer have great effect on the turn-on characteristics of the devices[15]. This turn-on characteristics of the YZY devices show a similar trend to other results reported by one of the research members in our research group[3].

Electroluminescence (EL) spectrum and luminous intensity of individual devices were measured by using Ocean Optics S2000 Spectrometer and Minolta LS-110 described in

detail in Chapter 3 (See Figure 3-17). One thing should be mentioned for this EL spectrum and luminance measurement is that these results are for different devices than those reported in the previous section. The experiments of measuring lateral EL spectrum and luminance were not performed simultaneously due to difficulty in measurements.

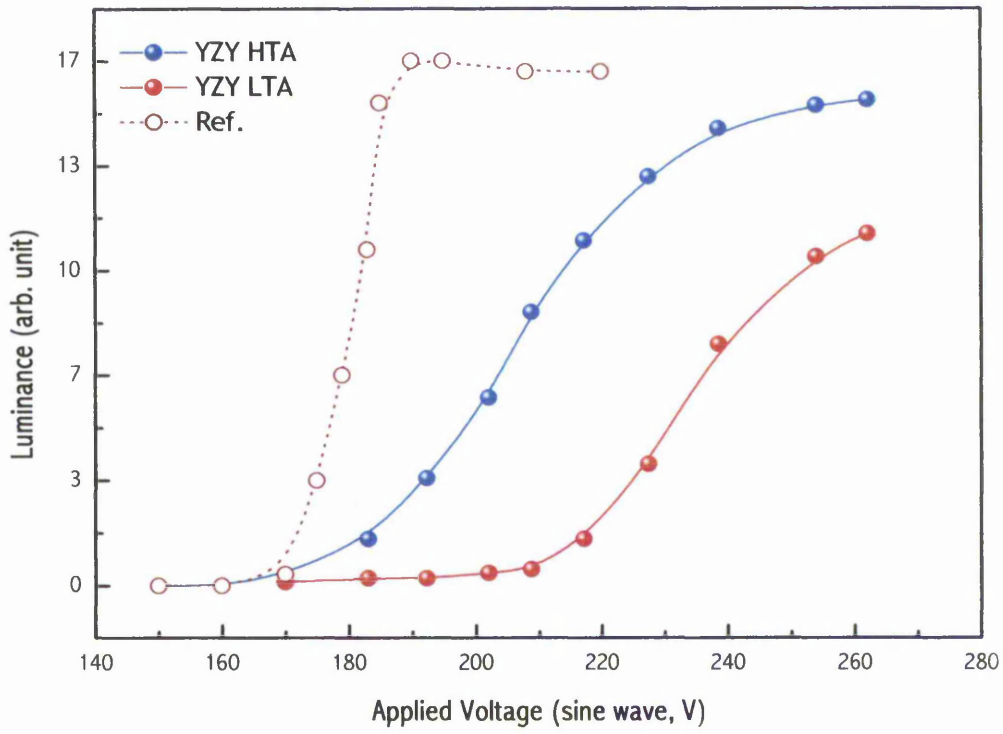


Figure 6-7 Luminance vs Voltage (*L-V*) curves of the YZY devices as a function of annealing temperature. High temperature annealing(HTA >= 500°C) and Low temperature annealing(LTA = 400°C) (Ref. curve is a typical *L-V* curve for comparison purpose)

The EL emission spectrum shows a typical emission characteristic of ZnS:Mn phosphor with around 580 nm peak in wavelength. There is no observed difference in the major peak wavelength among the devices. The EL emission spectrum is given in Figure 6-8. Due to the divalent transition-metal ion, Mn^{2+}, generally it has yellowish-orange peak around 580 nm in the ZnS host material. According to the CIE (Commission Internationale de l'Eclairage) chromaticity diagram, 580 nm yellowish orange emission has the coordinate of $x = 0.519$ and $y = 0.498$.

From this lateral emission, the BZY devices showed feasibility to improve the device turn-on characteristics and reduce its driving voltage by introducing perovskite solid solution BST thin films with high dielectric constant. The maximum normalised brightness (luminous intensity) of BZX devices had more than 40 cd/m² and particularly, BZY devices had brightness of around 64 cd/m² in lateral emission. For actual lateral luminance, conversion factor (ratio) of emitting area to the measurement area (0.0095 cm² for 1.1 mm diameter; 8 μcm² for emitting area)[22] should be considered. It is approximately 1188 for this device. Therefore, actual brightness of BZY devices is of 76,000 cd/m².

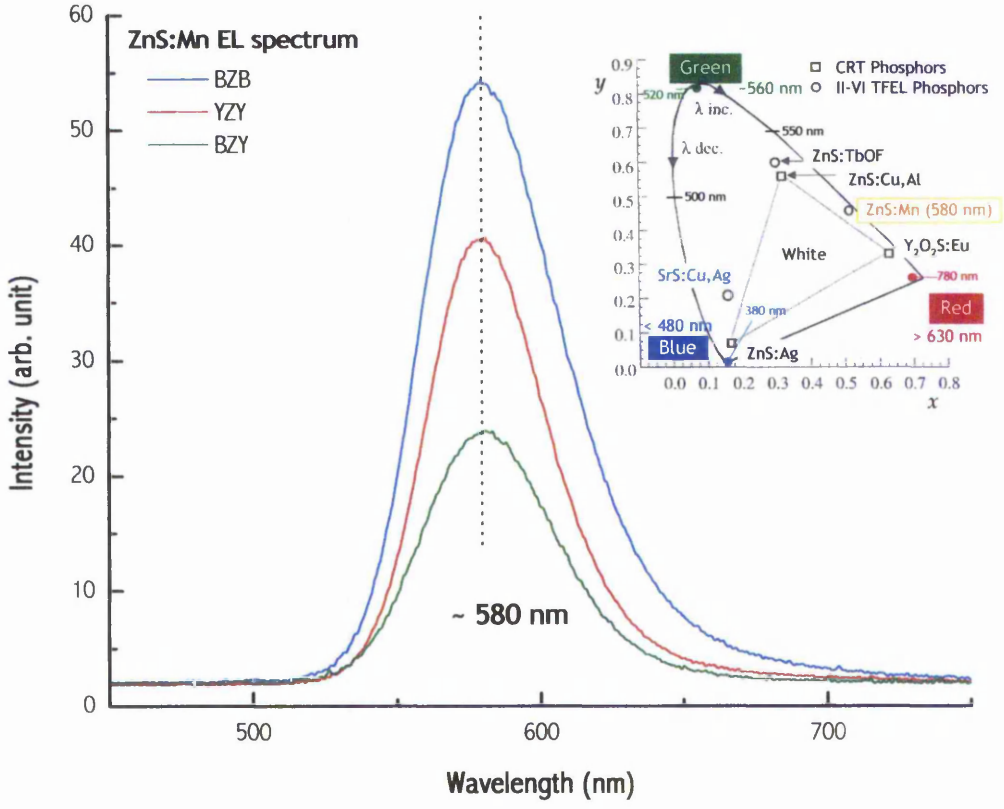


Figure 6-8 EL emission spectrum of ZnS:Mn lateral emission(LE) TFEL devices for EL emission optical properties. The applied voltage was not fixed because the maximum luminous intensity is achieved at different applied voltage and device-dependent. The peak wavelength is ~ 580 nm (yellow-orange region). x = 0.519, y = 0.498 of CIE coordinate[16] of the yellow emission is on insert.

6.3.2 Transferred Charge-Voltage (*Q-V*) Characterisation and Analysis

The relationship of transferred charge and applied voltage(*Q-V*) is one of the important characterisations in TFEL devices, where the transferred charge means the external total charges delivered to the test EL device. This measurement was commonly performed to understand the electrical characterisation of the EL devices when the devices were in operation.

An ideal parallelogram waveform and a real waveform of the transferred charge-voltage (*Q-V*) characterisation are shown in Figure 6-1 and 6-2, respectively. From the *Q-V* waveforms of EL devices, the individual capacitance of the components of the test EL device can be derived from the following basic equation:

$$C = \frac{dQ}{dV} \cong \frac{\Delta Q}{\Delta V} \qquad \textbf{Equation 6-8}$$

As explained in section 6.2.1, the two slopes of the parallelogram *Q-V* waveform are representing the total capacitance of the test EL device and the equivalent capacitance of two insulators, respectively. Therefore, two capacitances are easily obtained from the *Q-V* curve. Of course, the capacitances depend on the magnitude of the applied voltage.

From Figure 6-2, the total capacitance of the test EL device is measured as 0.22 nF and 0.98 nF is for the equivalent total capacitance of two insulating layers. And finally, the phosphor layer capacitance can be calculated by the equations 6-2 and 6-3 and the calculated capacitance of the ZnS:Mn phosphor layer is approximately 0.29 nF.

By studying the *Q-V* waveform, various information are obtained such as threshold voltages, conduction charges, relaxation charges and leakage charges according to the polarity of the applied voltage. In Figure 6-2 due to the symmetry property of the parallelogram waveform, it shows only some charges ($Q^{+}_{conduction}$, $Q^{+}_{relaxation}$, $Q^{+}_{polarisation}$ and $Q^{+}_{leakage}$) when the positive waveform of applied voltage is applied to the device. The transferred charge ($\Delta Q^{+}_{conduction}$), the relaxation charge ($Q^{+}_{relaxation}$), and the polarisation charge ($Q^{+}_{polarisation}$) are approximately 1.27 μC/cm², 0.16 μC/cm², and 0.64 μC/cm², respectively during the positive cycle of the applied voltage, while it is difficult to

determine the leakage charge (or leakage charge density) correctly from the Q-V loop of Figure 6-2. This conduction charge means the transferred charge for the entire EL device under the positive applied voltage. This unclear leakage charge seemed to be dependent on the waveform type and the magnitude of the applied voltage. In order to investigate the leakage charge and other interesting phenomena in more detail, superimposed Q-V loops are shown in Figure 6-9 as a function of the applied voltage at 200, and 250 V, respectively. The leakage charge density at the BST/ZnS:Mn interface was 0.26 μC/cm² at 250 V while at 200 V, it was 0.11 μC/cm². At reverse polarity of the applied voltage, these leakage charges were not different largely, respectively at Y_2O_3/ZnS:Mn interface.

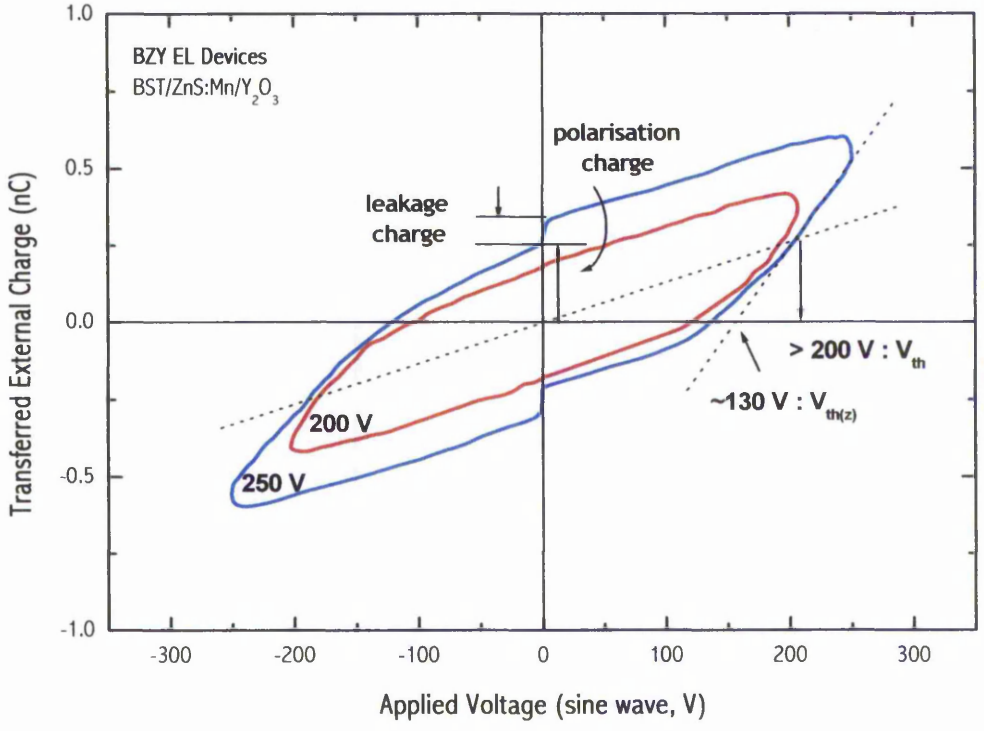


Figure 6-9 Superimposed double Q-V loops of BST/ZnS:Mn/Y_2O_3 (BZY) EL device as a function of the applied voltage at 200 and 250 V, respectively.

The threshold of the active layer, ZnS:Mn phosphor, means the actual minimum turn-on voltage for initiation of luminescence. The threshold voltage ($V_{th(z)}$) of ZnS:Mn active layer is approximately 150 V (approx. 130 ~ 171 V) on average and the threshold voltage(V_{th}) of the test EL device is approximately 200 V. Using Equation 6-1, the turn-on voltage of the

ZnS:Mn phosphor layer is about 153.8 V (or the threshold voltage of the test EL device will be approximately 195.1 V) in calculation. The difference between the threshold voltages is due to error of total capacitances in the experiments. However, calculation or measurement error can be accepted within that range of approximately 2.53% (from 150 versus 153.8 V for $V_{th(z)}$ and 200 versus 195.1 V for V_{th}). In fact, the phosphor layer's turn-on voltage ($V_{th(z)}$) is in good agreement in calculation. In addition, the threshold voltage is similar to the threshold voltage of the lateral emission TFEL device on Si in previous section in this chapter.

6.3.3 Dynamic Capacitance-Voltage(C_D-V) Analysis

As the two different slopes from the Q-V loop, a C-V graph of the EL device is shown in Figure 6-4 and 6-10. There are two plateaus which represent the total capacitance(C_t, or C_{EL}) of the test EL device and the total capacitance(C_i or $C_{insulators}$) of two insulator layers, respectively.

In Figure 6-10, V_{th1} is around 150 V at which the phosphor layer is initiated to be in conduction state. V_{th2} is about 170 V and this midpoint has been know as the actual turn-on voltage of the phosphor layer[3,4,13]. Finally, V_{th3} as a steady-state applied voltage is measured at 180 V from the Figure 6-12. As the applied voltage increases from this value, the phosphor field is in the steady-state and a field clamping effect occurs. The field clamping effect is an important and interesting phenomenon that when the electrical field is applied to the phosphor layer. It is not increasing and sustains the steady-state as the applied voltage increases. The field clamping effect is also shown in the Figure 6-9 of the superimposed Q-V loops. In the Q-V loop, the shorter lines in the region (or section) of the total insulating capacitance (C_i) are overlapped as the effect of the field clamping. Regardless of increasing the applied voltage, the region (**BO'CD** in Figure 6-2) of the slope representing the total capacitance of two insulator layers is not longer expanding.

These capacitances are calculated by taking the thickness and relative dielectric constant of the phosphor and insulator layers. In the case of the ZnS:Mn TFEL device, the dielectric

constant of the phosphor, BST, and Y_2O_3 are 8.3, 34‡, and 13, respectively. The measured capacitance from the *C-V* curve and the numerical calculation of the capacitance from the relation, $C = \frac{\varepsilon_o \varepsilon_r A}{d}$, are given in Figure 6-9. The capacitances of the 300 nm-thick yttrium oxide layer and the 300nm-thick BST layer are 1.39 nF and 3.16 nF, respectively. Thus, the equivalent capacitance of the two insulator layers is 0.965 nF. The capacitance of the 800 nm-thick ZnS phosphor layer in theory is 0.289 nF. Therefore, the total capacitance of the test EL device will be 0.223 nF. These capacitances are in good agreement with measured capacitances from the Figure 6-10 and the *Q-V* loops in Figure 6-2 and 6-9.

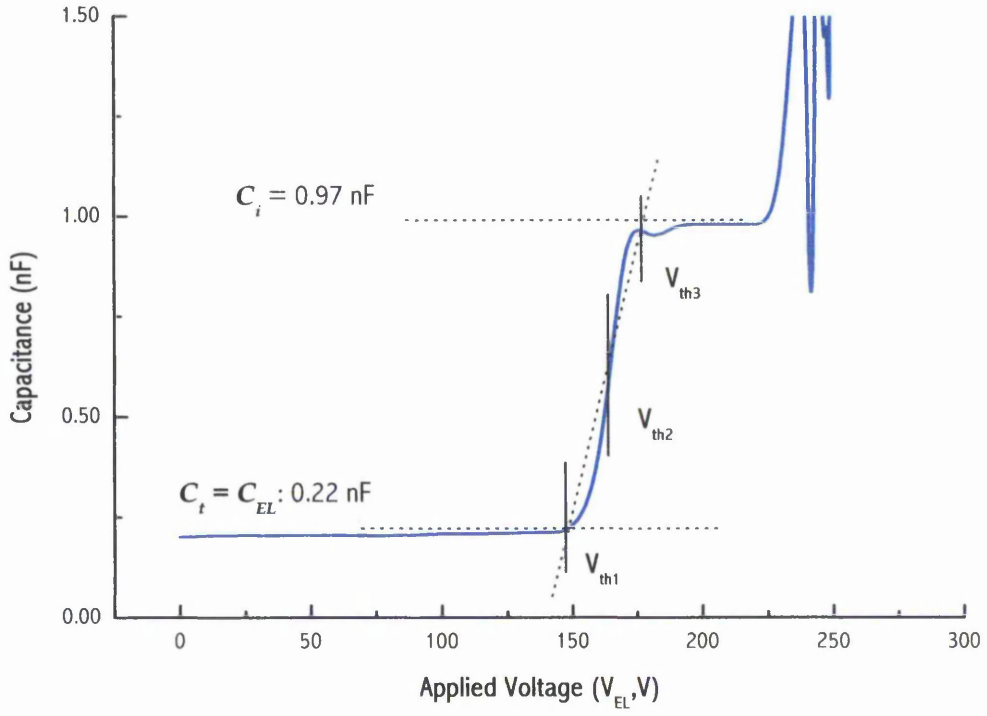


Figure 6-10 A dynamic *C-V* curve of a ZnS:Mn TFEL device with BST(300 nm thick) and Y_2O_3(300 nm thick) layers as bottom and top insulating layer, respectively. V_{th1}, V_{th2}, and V_{th3} show the different stages for the device turn-on voltage.

In addition, the interface state density (Q_{ss}) can be derived from the *C-V* curve. Particularly, the slope of the transition region of the *C-V* curve is related to the density of the interface

‡ The dielectric constant of BST thin film has various values. From the results of the previous chapter, BST, 34 is taken for calculating capacitance of BST layer as an average.

traps in the sub-field clamping regime. Assuming a linear transition from V_{th1} to V_{th3} in the *C-V* curve, the externally measured interface state charge state and the internal interface state charge in the pre-field clamping can be given by[13]

$$Q_{ss}^{ext} = \frac{1}{2}(\Delta C)^2\left[\frac{\Delta C}{\Delta V}\right]^{-1} \qquad \textbf{Equation 6-9}$$

and

$$Q_{ss}^{int} = \frac{C_i^2}{2}\frac{C_i}{C_p}\left[\frac{\Delta C}{\Delta V}\right]^{-1} \qquad \textbf{Equation 6-10}$$

where $\Delta C = C_{th3} - C_{th1}$ (C_{th} means the capacitance corresponding to the applied voltage, V_{th}), $\Delta V = V_{th3} - V_{th1}$.

Finally the interface state density Q_{ss}, can be expressed in units of number of states per square centimeter, which is defined by the following equation[13]

$$Q_{ss} = \frac{C_i^2}{2qA}\frac{C_t}{C_p}\left[\frac{\Delta C}{\Delta V}\right]^{-1} \qquad \textbf{Equation 6-11}$$

where q is the electron charge of 1.602×10^{-19} C, A is the pixel area of the device (= 0.031516 cm^{-2}). Equation 6-11 indicates the interface state density has inverse proportion to the slope of the *C-V* transition. This abrupt *C-V* transition represents a small density of interface states[13]. Using Equation 6-11 and taking the capacitances and corresponding voltages from Figure 6-10, the interface state density for ZnS:Mn/BST was $1.90\sim2.17 \times 10^{12}$ cm^{-2} and $1.6\sim1.87 \times 10^{12}$ cm^{-2} was the interface state density of ZnS:Mn/Y_2O_3 for the negative half cycle.

6.3.4 Internal charge($Q_{internal}$) - Phosphor field(F_p) Analysis

In section 6.3, the total transferred charge is investigated as a function of applied voltage. This is a basic method to characterise the electric properties of the TFEL devices in point of view of the entire device. Additional charge-phosphor(Q-F_p) field technique has been developed to investigate the internal behaviour information of the EL devices. A clockwise direction of the Q-F_p loop is opposite to the direction of the Q-V loop. Figure 6-5 indicates the internal charge-phosphor field(Q-F_p) loop of a ZnS:Mn TFEL device with a steady-state phosphor field.

Like the Q-V loop, the conduction charge density during the positive half cycle of the applied voltage (waveform) is approximately 1.3 μC/cm². A maximum phosphor field at steady state is about 1.61 MV/cm, which is indicating proof of the field clamping effect. At this moment, the actual electric field applied to the phosphor layer does not increase any more and remains constant even though the applied voltage increases. From the Q-F_p loop, the polarisation and relaxation charges have approximately 0.64 and 0.2 μC/cm², respectively. The phosphor field by polarisation is on the range of 0.6~ 0.65 MV/cm due to the polarity of the applied voltage. The relaxation charge means the phosphor field reduces due to charge transfer.

The phosphor field starts to reduce its intensity in advance after reaching the maximum phosphor field. When a trapezoidal waveform of the applied voltage is used, there is a short period (i.e., duty cycle) to remain at the maximum voltage before changing its polarity of the waveform. However, a sine waveform does not have that kind of minimum time difference and continuously decreases its intensity. As a result, the field intensity can correspond accordingly. Therefore, it is very difficult to measure the relaxation charge correctly. It seems to strongly depend on the type of the waveform of the applied voltage in Q-F_p loop. Thus, 0.2 μC/cm² is an estimated value for applying a sine wave.

As the applied voltage increases, the Q-F_p loop shows an increase of conduction, polarisation, relaxation, and leakage charge accordingly, but the phosphor field shows the steady-state and sustains the constant phosphor field of 1.6 MV/cm. Therefore, after the

turn-on voltage, the field clamping effect is in progress as the applied voltage increase. The superimposed Q-F_p loops as a function of the applied voltage is shown in Figure 6-11.

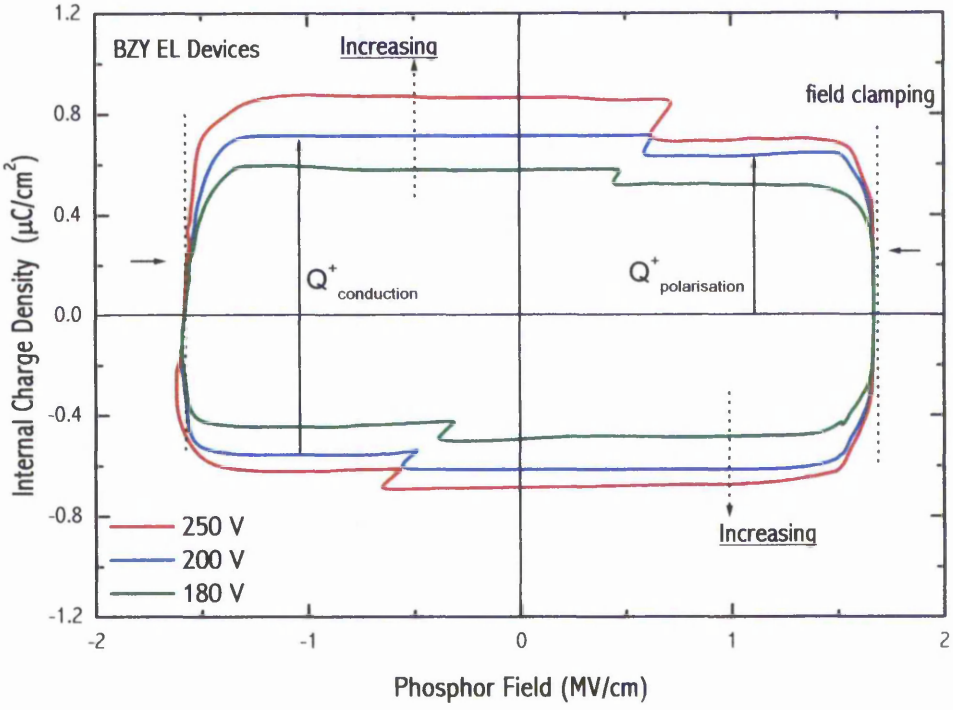


Figure 6-11 Superimposed internal charge-phosphor field(Q-F_p) loops of BZY EL devices as a function of the applied voltage.

6.3.5 Luminance(Brightness) and Luminous Efficiency

Luminous efficiency - Voltage(η-L), also known as Efficiency-Voltage, characterisation is an interesting experiment with luminance-voltage(L-V) measurement. Basically, the η-L measurement determines the luminous intensity of an EL device per unit power consumed, or luminous efficiency(η), which has the unit of lumens per watt (lm/W). The lumens, an SI unit of luminous flux, is defined as the luminous flux emitted by a uniform point source, of intensity one candela(cd), in a cone of solid angle one steradian. Thus $1\,\mathrm{lm} = \frac{1}{4\times\pi}\,\mathrm{cd}$ [17]. The luminous efficiency, η, can be expressed by

$$\eta = \frac{\pi \times L}{P_{in}} (\times 10^{-4}) \text{ [lm/W]} \qquad \textbf{Equation 6-12}^{[11]}$$

where L is the measured luminance with the unit of cd/cm^2, P_{in} is the applied input power density in W/cm^2. If there is difference between units, the factor, 10^{-4}, should be considered.

The input power density, P_{in}(W/cm^2), is known as the following relations[18],

$$P_{in} = 2 \times f[Hz] \times V_{th(z)} \times \Delta Q \ [\mu C/cm^2] \times 10^{-6} \qquad \textbf{Equation 6-13}$$

or

$$P_{in} = 2 \times f[Hz] \times V_{th} \times \Delta Q_{(z)} [\mu C/cm^2] \times 10^{-6} \qquad \textbf{Equation 6-14}$$

where f is the frequency(Hz) of the applied voltage, ΔQ is the transferred charge density and $\Delta Q = [(C_i + C_p)/C_i] \times \Delta Q_{(z)}$.

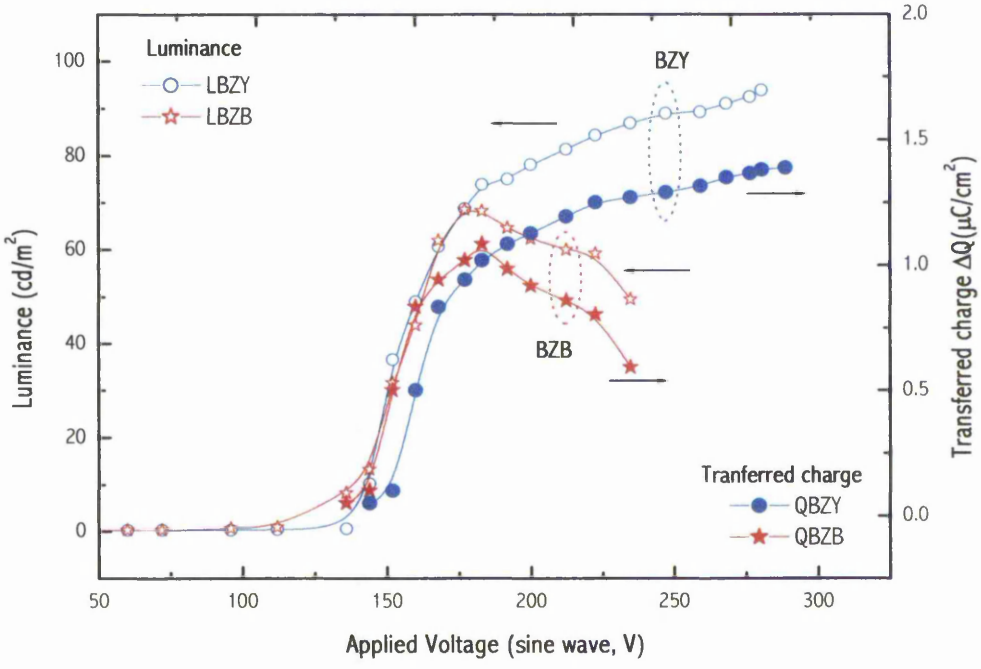


Figure 6-12 Luminance-Voltage(L-V) and transferred charge density-Voltage(ΔQ-V) characteristics of the ZnS:Mn TFEL devices.

Before investigating luminous efficiency of the EL device, the transferred charge density-voltage(ΔQ-V) relationship was studied. Luminance-Voltage(L-V) and transferred charge density(ΔQ-V) curves are shown in Figure 6-12. Transferred charge increases with the same trend of the luminance in both devices. As the applied voltage increases, the transferred charge is likely to be saturated at 1.4μC/cm² and 300 V for the BZY devices. The BZB device's instability in operation was observed again as the lateral emission case. A L_{40} (luminance at 40 V above the turn-on voltage) of the test ZnS:Mn EL device is 75 cd/m² and it shows the maximum luminance of approximately 90 cd/m², while the BZB device had the maximum luminance of 68 cd/m² at 180 V. These luminance are still lower than that (260 cd/m²) of YZY devices[3]. However, the BZY and BZB devices show good turn-on characteristics around its turn-on voltage of 150 V which is a significant drop in V_T.

Luminescence as surface emission and its luminous efficiency was investigated as a function of frequency. EL intensity of two devices, BZY and BZB, strongly showed dependence of the applied frequency. As the frequency increases, luminance tends to increase accordingly. It is believed that higher possibility of cross-sectional impact excitation in the ZnS host material rapidly increases due to high frequency. In addition, luminance also depends on the transferred charge density and the ZnS:Mn phosphor layer material properties[11]. Thus the luminance can be expressed by the following equation[11],

$$L[\mathrm{cd/m^2}] = k \times f[\mathrm{Hz}] \times \Delta Q[\mu \mathrm{C}/cm^2] \qquad \textbf{Equation 6-15}$$

where k is the coefficient which depends on the active layer properties.

In order to increase the luminance, it is necessary to improve the active layer properties and to increase the transferred charge density if the frequency is fixed (see Eq. 6-15). In fact, the transferred charge density heavily depends on the interface properties between the phosphor layer and the insulating layers. When the frequency is fixed at 5 kHz, the obtained coefficient k can have the range of 1.35~1.45. Thus, according to the frequency, the transferred charge density will be estimated for the fixed luminance.

Luminous efficiency, η, is supposed to be a constant with respect to the driving frequency and voltage because the luminance is proportional to the transferred charge density from the Equation 6-15 and the luminous efficiency, η, has the inversely proportional to the frequency and transferred charge density in Figure 6-9 and 6-10. Using the Equations 6-12~14, the estimated (calculated) luminous efficiency can be obtained. L-V and η-V characteristic curves are shown in Figure 6-15. Regardless of the driving frequency, the luminous efficiency, η, shows almost a constant range of 1.1 ~ 1.0 (lm/W) after turn-on voltage. This is in good agreement with other results of ZnS-based or ZnS:Mn TFEL devices[18]. However, ZnS:Mn-based TFEL devices were reported to have 5 (lm/W)[19], which is one of the most efficient devices in various TFEL devices including non-ZnS-based EL devices.

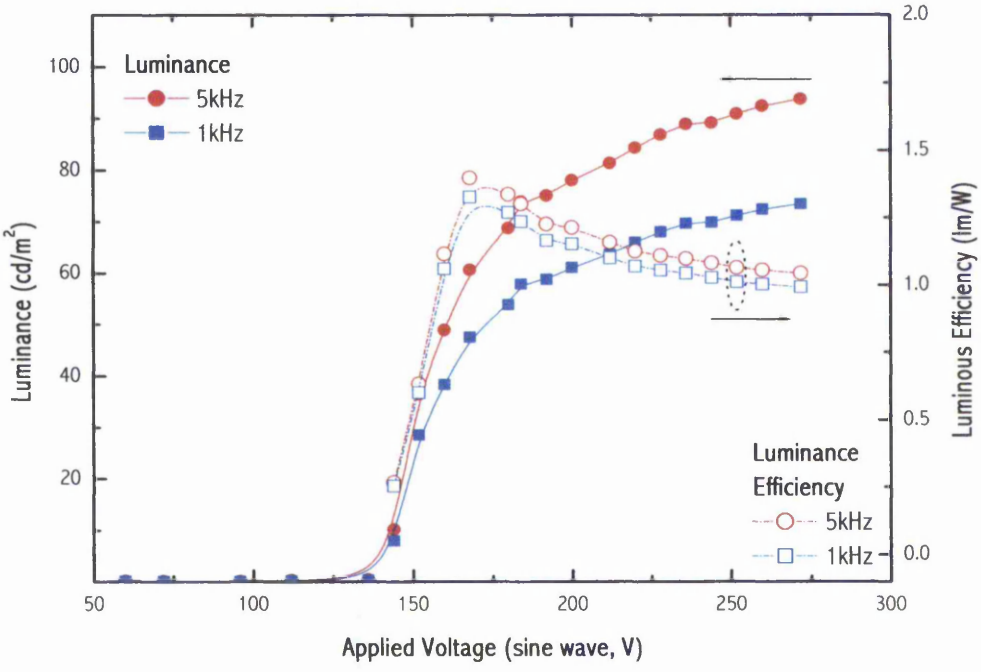


Figure 6-13 Luminance-Voltage(L-V) and Luminous efficiency-Voltage(η-V) characteristic curve of BZY EL devices as a function of the driving frequencies at 1 and 5 kHz, respectively.

6.4 Blue Emitting TFEL devices

Yellowish-orange emitting ZnS:Mn TFEL device's electro-optical properties have been discussed in previous sections. In this section, a blue emitting TFEL device will be dealt with. Blue emitting phosphors and EL devices are one of the most important subjects in inorganic TFEL devices with high-κ dielectric materials. In order to realise blue emitting EL devices, copper (Cu) and sliver (Ag) co-doped strontium sulphide(SrS:Cu,Ag) phosphor and yttrium oxide (Y_2O_3) dielectric material were used. In addition, a dielectric thin layer which is named "barrier layer" was inserted within SrS:Cu,Ag phosphor layer to improve total luminance of the devices. At the same time, instead of a thermal annealing process, pulsed laser annealing treatment was applied to the SrS:Cu,Ag phosphor layer as material engineering technique for structural and physical improvements. The reason for applying the laser annealing process to SrS:Cu,Ag phosphor was to get working devices. More specifically, thermal annealed SrS:Cu,Ag EL devices showed no proper EL emission and at the same time they had critical problem on device stable operation [20]. The effects of the structural modification (barrier layer structure) and laser annealing process applied to enhance the device total performance in luminance and turn-on voltage characteristics will be discussed here.

6.4.1 Non-Barrier Layer EL Devices

6.4.1.1 Pulsed Laser Annealing Effects

Before going on to investigate the barrier layer effects in EL devices, it is necessary to examine the EL emission spectra of non-barrier layer(NBL) devices under high laser fluence (average ~ 2.29 J/cm^2) and low laser fluence (average ~ 1.85 J/cm^2) with different number of laser pulses (2 ~ 5 pulses (2 ~ 5ps) for high fluence and 4 ~ 7 pulses (4~ 7ps) for low fluence), respectively. The number of laser pulse applied in this study was based on some previous experimental results at NTU[21]. The measured EL emission spectra of non-barrier layer devices are shown in Figures 6-14 and 6-15. There are three emission bands observed at 503.9 nm, 532.1 nm, and 556.4nm. Throughout this section, EL emission intensity was measured at its maximum peak so the corresponding applied voltage depended on the devices. In terms of emission intensity, the device of low laser fluence

was better than that of high laser fluence. From these figures, under the laser annealing treatment with the low laser fluence, the EL devices having a low number of pulses (4 pulses) showed the highest emission intensity. The intensity decreased as the number of pulses increased. There was minor irregularity in high fluence, but the similar trend of intensity could be identified on the devices with high laser fluence treatment.

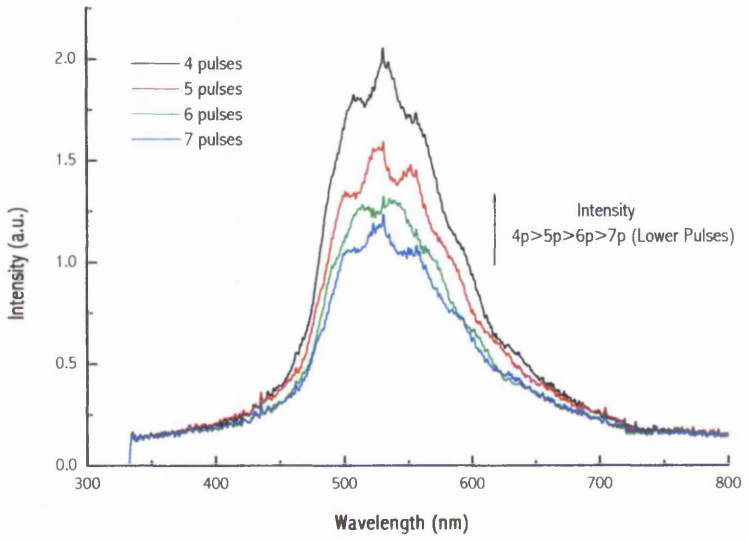


Figure 6-14 EL spectrum of non-barrier layer (NBL) EL device with laser annealing treatment in lower fluence (1.85 J/cm^2)

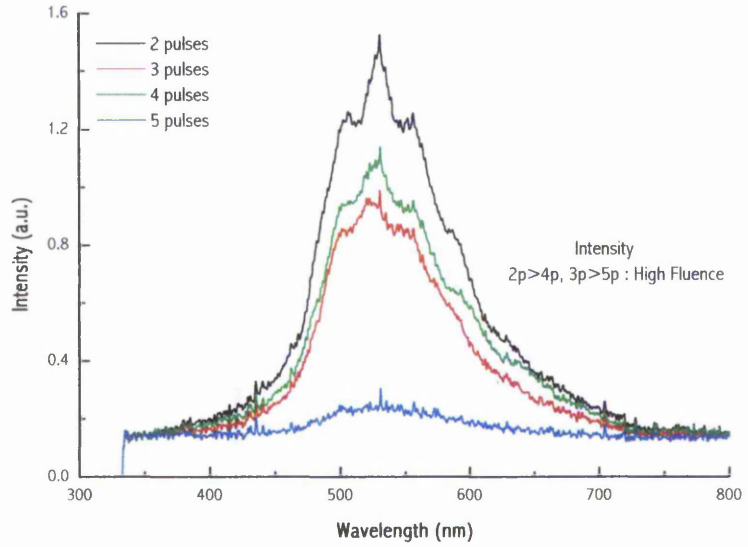


Figure 6-15 EL emission spectrum of NBL EL devices with laser annealing treatment in higher fluence (2.2 J/cm^2)

In order to find out more detailed characteristics of electroluminescence of non-barrier layer devices, EL emission properties of only 4- and 5-pulse laser annealed non barrier layer devices are presented in Figure 6-16. Now it is possible to observe some clear trend in pulsed laser annealing dependence in both of high and low fluences. In low fluence, the intensity of the non barrier layer device with 4-pulse laser annealing treatment was the peak and almost two times higher than the devices with the same number of laser pulses in high fluence. As a result, lower pulse laser treatment is clearly more effective. In addition, a lower number of pulses could be considered as one of the critical factors to improve EL emission properties. Probably it can be understood that the higher fluence caused some laser ablation of the films.

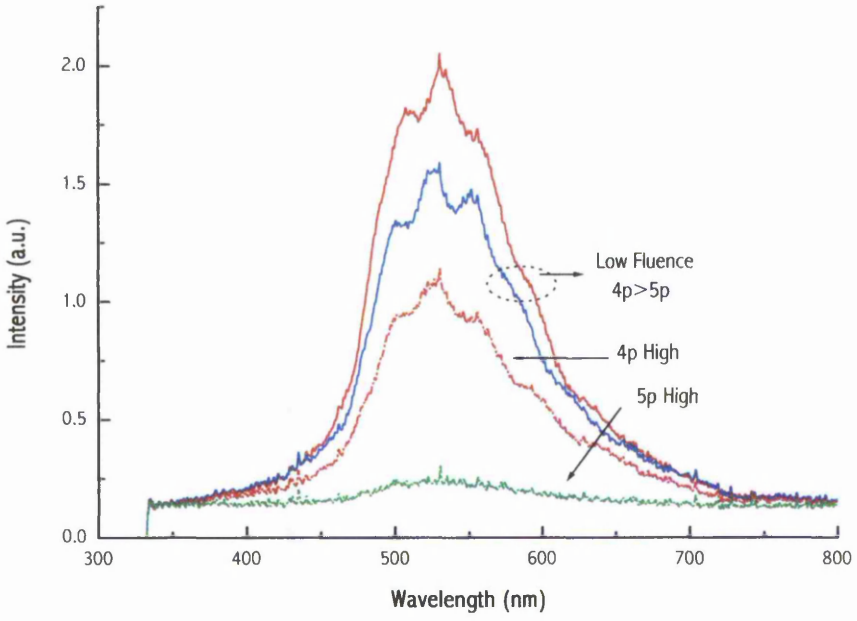


Figure 6-16 EL emission spectrums of NBL EL devices with 4 and 5-pulse laser annealing in low and high fluences

6.4.2 Barrier Layer EL Device

6.4.2.1 Barrier Layer Effects in Electroluminescence

For the barrier layer effects in EL, it is necessary to compare two devices under the same conditions. It is clearly very difficult to discuss what the main factors are in mixed conditions. That means because all devices had laser annealing treatment, it can be complex to identify pure barrier layer effects. However, before analysing the barrier effects, there is one thing to bear in mind from the previous section: the intensity of EL emission of the NBL devices was decreasing with the number of pulses in laser annealing.

At 2-pulse with high fluence, there were no significant effects associated with the addition of the barrier layer. In this case, the non barrier layer device showed better results. For other cases – 3-, 4- and 5-pulse, in high fluence, apparently seemed to have some positive effects from the barrier layers. All barrier layer devices demonstrated improvements in luminance compared to that of non barrier layer device in luminance. Individually, three devices except the 2-pulse device had some improvement from having the barrier layers. In particular, the 30 nm barrier layer device with 5 pulse laser annealing had outstanding improvement in luminance. As an interim (or tentative) analysis, they might not be improved, but the non barrier devices were degraded by a higher number of pulse with high fluence. Figure 6-17 shows EL emission characteristics of 2- and 5-pulse laser annealed devices with high fluence.

In lower fluence, only 5-pulse laser annealed device had positive effects. Similar to the higher fluence devices, individually the devices were improved in terms of brightness except 4-pulse laser annealed NBL device. The difference between the high and the low fluence is that after 5 pulses in low fluence, the EL emission intensity of the device remained at least at the similar level. The EL emission spectra of 4-pulse laser annealed NBL device and the 5 pulse laser annealed barrier layer device is given in Figure 6-18. Hence, considering the effect of two or more processing variables, it can be predicted that the laser annealing effect can be a much more dominating factor than the barrier layer in the overlapped conditions - the number of pulse, barrier layer thickness (including non

barrier layer) and laser fluence. EL emission properties of all devices are summarized in Table 6-1.

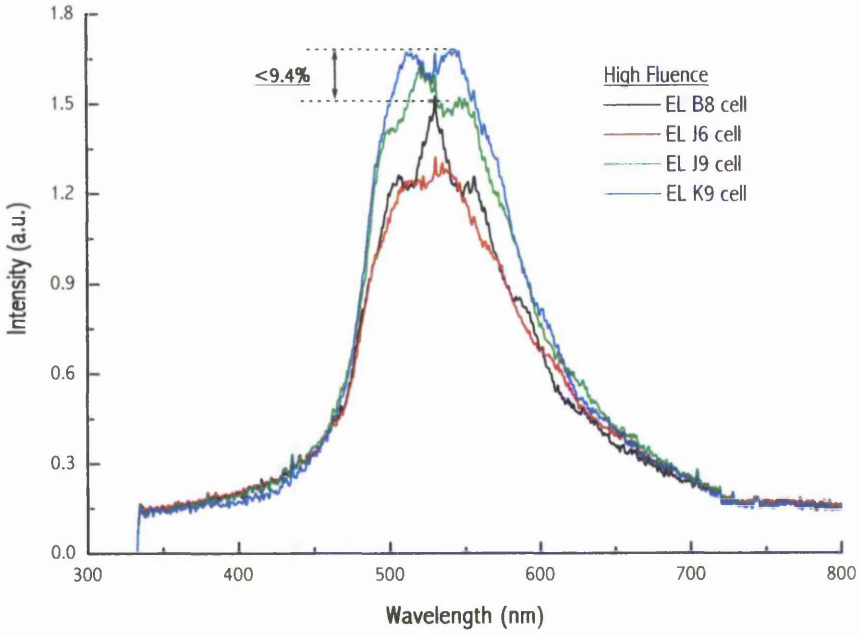


Figure 6-17 Emission intensity of 2-and 5-pulse laser annealed devices in high fluence

Thermal annealed single barrier layer devices was known to have significant improvement in luminance of ZnS-based EL device[22]. According to Cranton, W. M.[22], a 10 nm barrier thickness device was superior to the thicker barrier layers in EL emission properties. However, from the results of this study, only 5 pulse laser annealed devices with 10 nm barrier layer showed its improvement, but it is hard to say the improvement by the barrier layer or laser annealing, thus requiring more work to identify this point. Some noises in the EL and PL spectra from Figure 6-14 to 6-18 and Figure 6-19 are due to interference by the stacked thin film structure.[23]

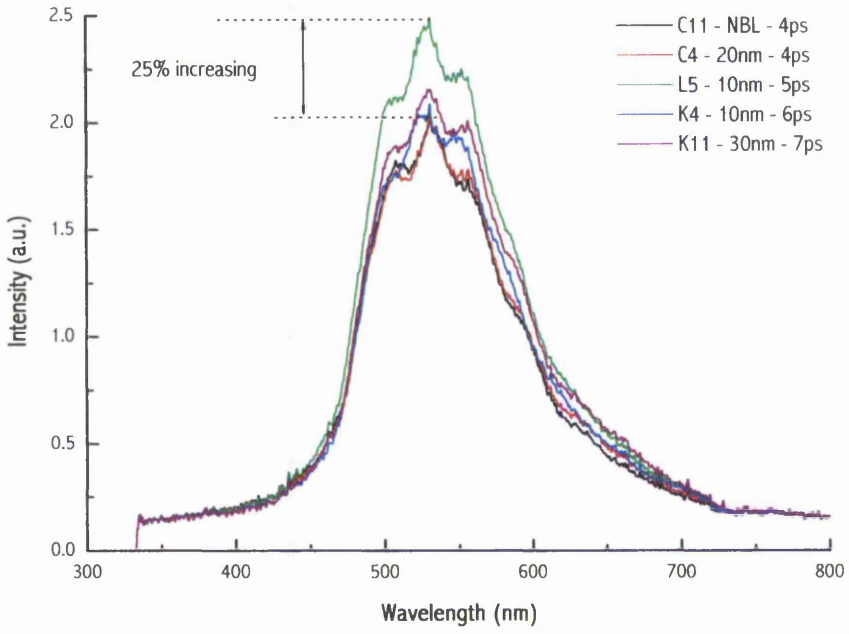


Figure 6-18 Emission luminance of 4(NBL) and 5(BL) pulse laser annealed devices in low fluence

Table 6-1 EL emission characteristics of the laser annealed devices with three variables; barrier layer thickness, the number of pulse, and laser fluence.

Laser Fluence	4 pulses	5 pulses	6 pulses	7 pulse	
Low (1.85 J/cm²)	NBL/20 nm	10 nm	10nm	30 nm	↑
		NBL/20nm	30nm	10 nm	
	30 nm		NBL	NBL/20 nm	
	10 nm	30 nm	20nm		
	2 pulses	**3 pulses**	**4 pulses**	**5 pulses**	
High (2.29 J/cm²)	NBL/20 nm	10 nm	30 nm	30 nm	
		20 nm	20 nm/NBL	10 nm	↑
	10 nm	NBL		20 nm	
	30 nm	30 nm	10 nm	NBL	

[The direction of arrows denoted increase in EL intensity.]

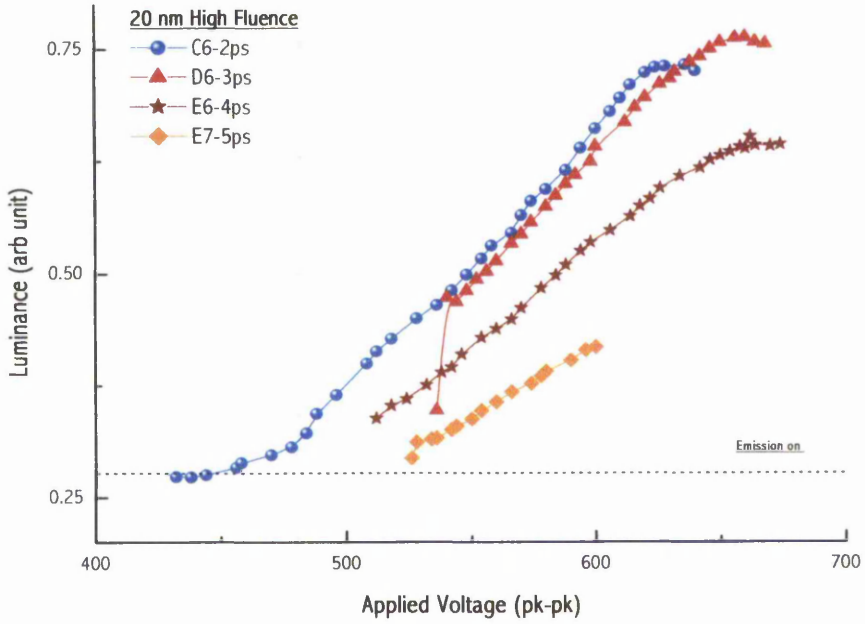


Figure 6-19 *L-V(or B-V)* curves of 20 nm barrier layer devices in high fluence

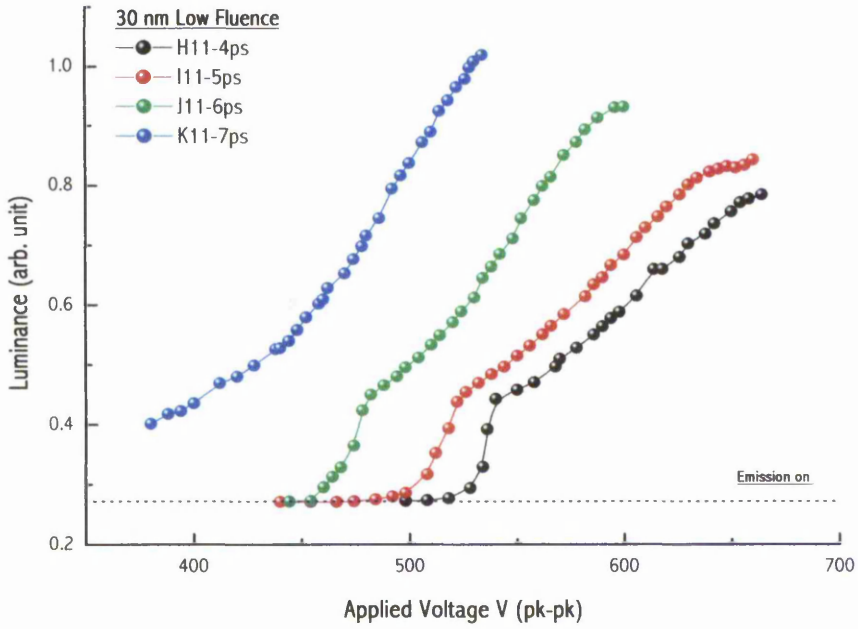


Figure 6-20 *L-V(B-V)* curves of 30 nm barrier layer device in low fluence

6.4.2.2 Laser Annealing Effects

In addition to spectral measurement, brightness-voltage (*B-V*) characteristics were studied to examine the effect of laser annealing in EL performance. The barrier layer device was discussed already in previous section. According to the *B-V* curves of barrier layer devices, the results can be divided into two subgroups: 10/20 nm barrier layers and 30 nm barrier layers. Figure 6-19 and 6-20 show 20 nm barrier layer device (high fluence) and 30 nm barrier layer device (low fluence).

Like the NBL devices, the brightness of 10 and 20 nm barrier layer devices decreases with the number of laser annealing pulses. Although there were some irregularities in 10 and 20 nm barrier layers, the highest brightness was on lower pulse laser annealed devices. The typical trend of brightness decreasing is shown in Figure 6-20. For 30 nm barrier layer devices, the *B-V* properties improved with the number of laser pulses in low and high fluence.

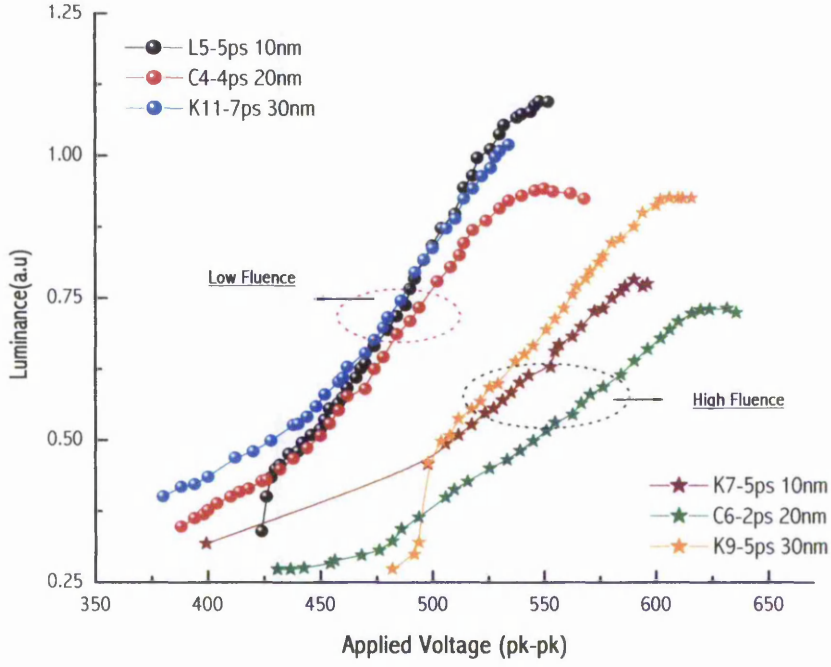


Figure 6-21 *B-V* properties of laser annealed devices with barrier layers

The barrier layer and laser annealing effects discussed above are incorporated in Figure 6-21. These devices showed good performance among all fabricated devices in EL emission properties. The devices were annealed by low fluence are better than ones in high fluence in brightness and in terms of driving voltage. From these results, it may be concluded that a 10 or 30 nm barrier layer thickness can have the feasibility of improving the device performance.

Specifically, in laser annealing a low fluence and low number of pulses was effective in improving device performance, whether the device has the barrier layers or not. For this, it is possible that the phosphor layer could be ablated by the laser energy and multiple irradiation, and then after irradiation, the phosphor layer could have two or more re-growing regimes[24]; in low fluence, phosphor layer can have fine grain structure. In medium or high fluence, large grain layer or columnar grains could be grown within the phosphor layer due to non-equibrilium condition, which means that the surface and interior of the phosphor layer could have two different phase states during the cooling. For having fine grain layer, crystallinity of the phosphor layer can be improved, but crystallinity of the phosphor layer, on the contrary, could be degraded severely in large or columnar grain structure. Additionally, through the laser irradiation, insulator-semiconductor interface states as a major carrier injection source could be favourable or detrimental[24].

6.4.2.3 Photoluminescence

A He-Cd laser system with 325 nm ($E_{excitation}$ = 3.81 eV) for PL measurement was used at room temperature in dark room condition. The PL characteristics in this experiment are explained in Chapter 3. One of the advantages by using the sub-bandgap ($E_{excitation} < E_{g[SrS]}$ = 4.3 eV) excitation is that reduced energy absorption of host material[25]. There are six PL emission bands and their emission peaks were observed at 407(3.05 eV), 413.7 (3.0 eV), 437(2.84 eV), 506(2.45 eV), 684(1.81 eV), 706(1.75 eV) and 730(1.70 eV) nm, respectively. Among these peaks, only the peaks within the range of 400 ~ 550 nm will be discussed. The PL emission spectra in Figure 6-22 show each one from the EL devices with different barrier layer thickness. In fact, other devices, regardless of their barrier layer thickness and

irradiated laser pulse, had almost the same peak properties except 20 nm barrier layer device (only low fluence), which may be an anomaly.

According to some reports[26,27,28,29,30], various emission bands have been reported. PL emission at 459(455), 490, 510(505), 528, and 530 nm were assigned to the Cu^+ emission bands, with emissions at 360 and 430 nm thought to be Ag^+ emission bands. Basically, due to temperature- and activator concentration-dependent properties of PL emission characteristics and its excitation energy, the measured PL emission bands were a little different: 407, 414, 437, and 506 nm. Hence, the emission band at 506 nm can be assigned to Cu^+ and the band at 437 nm can be assigned to Ag^+. Two emission bands at 407 and 414 nm are likely related to Ag^+ rather than Cu^+.

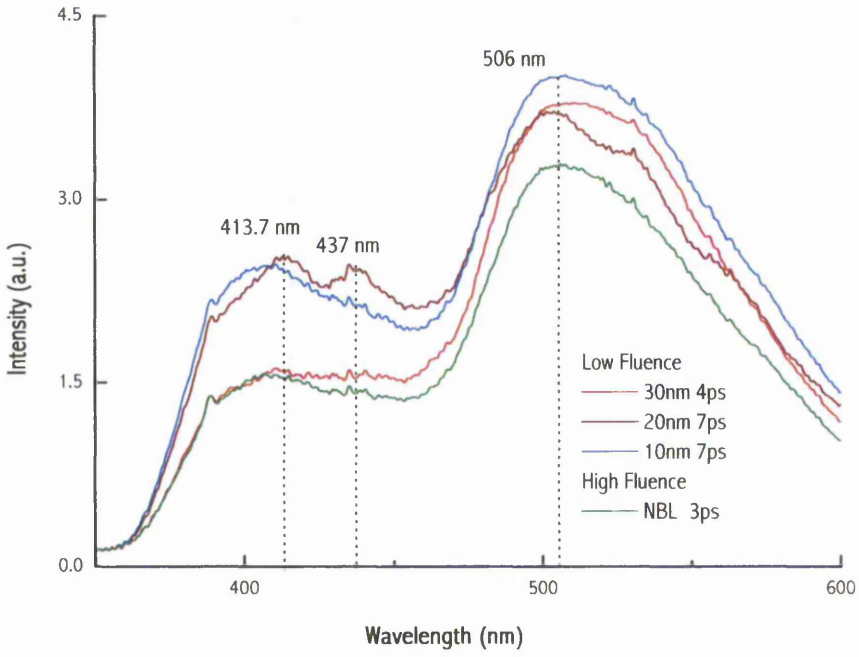


Figure 6-22 PL emission spectra of the SrS:Cu,Ag phosphor thin films

From the PL emission bands observed, the band at 437 nm was only detected in 20 nm barrier layer devices with low laser fluence. Except the 20 nm barrier layer devices, the band at 437 nm is too weak to notice. Interestingly, there were no emission bands at

around 530 nm from Cu^+ in this measurement. The PL emission can be more greenish-blue or bluish-green caused by these emission bands[28]. PL emission properties of activator Cu has been understood by the following process: by excitation, a Cu^+ ion can have $^1A_{1g} \rightarrow {}^1E_g$ or $^1T_{2g}$ of spin allowed transitions and then have an emission transition from the lowest excited state: $^3E_g \rightarrow {}^1A_{1g}$ in the crystal field with octahedral symmetry[26,29]. The basics of crystal field theory, or ligand field theory is in Appendix C.

By doping Ag as co-activators, a peak emission shift from 480 to 430 nm was reported by Sun, S.-S[31]. He explained that this peak emission shift was attributed to an energy transfer from Cu^+ to Ag^+, but Li, W.-L. *et. al.*[32] did not find evidence for the energy transfer from Cu^+ to Ag^+. In this experiment, although Ag^+ ion's blue emission band was lower than that of Cu^+ ion, the PL emission spectra showed Ag^+ blue emission effect. Unfortunately, in EL emission, the device's major peak was at around 520 nm[31] (see Figures 6-14 ~ 18). It might be related to laser annealing, but the reasons in PL and EL emission of SrS:Cu,Ag are not fully understood and still need to be investigated.

6.4.2.4 Driving Voltage Dependence

By inserting the barrier layer, the device driving voltage can be increased, which has been observed in EL devices with ZnS-based phosphor[22]. However, the results show that laser annealing can be used to reduce the driving voltage. From Figure 6-21, reducing the device turn-on voltage was made in a low fluence treatment. On average, the low fluence device turn-on voltage was observed at around < 400 V(pk-pk). Through the laser annealing treatment, the turn-on voltage was improved in thick barrier layer devices. In addition, higher brightness was obtained at lower driving voltage under low laser fluence. For the high fluence, an equivalent brightness could be obtained at around 100 V(pk-pk) higher driving voltage, but the saturated brightness from the device in high fluence was much less than the counterparts in overall trend.

6.4.2.5 Transient Response and Decay Time

Typically, ZnS-based EL devices have only a luminance peak at the leading edge(LE) when a voltage pulse is applied, but SrS:Ce and SrS:Cu,Ag are known to show another peak at the trailing edge(TE)[33]. Through transient measurements, peaks at the leading and trailing edge were identified in this experiment. In addition, the average decay time of the luminance peaks is displayed in Figure 6-23. Regardless of the number of pulses, all devices have the same trend that at the trailing edge average decay time of luminance peak is longer than that at the leading edge. With a low number of pulses, however, there is a longer decay time. Under the low fluence, decay time of both leading and trailing edge were stable around 9 and 14 μ sec, respectively, while for high fluence, a range of change in decay time was relatively large. To understand internal properties of phosphor layer more in detail from transient measurement, additional measurements need to be carried out.

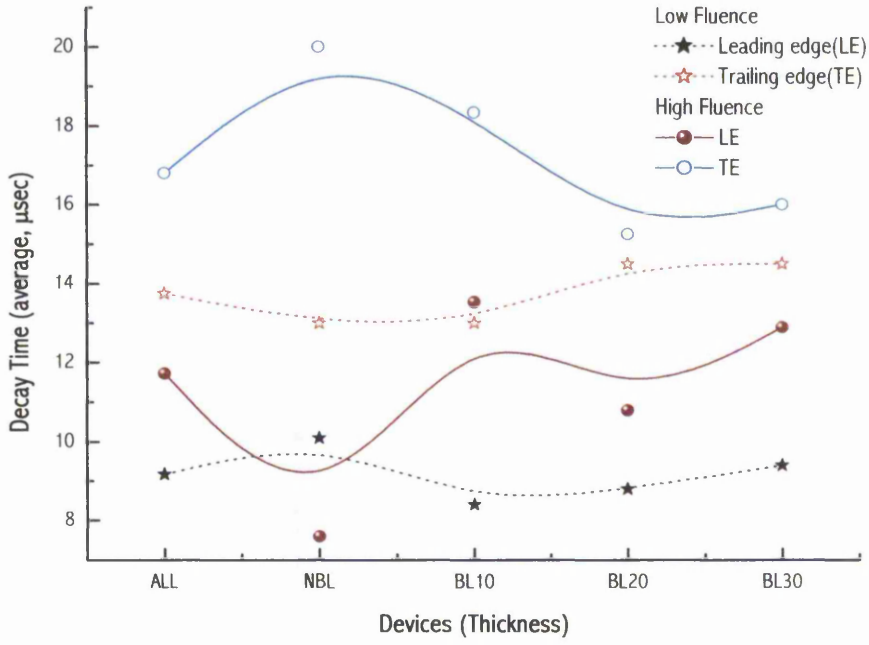


Figure 6-23 Average decay time (μsec) from transient response measurements

6.5 Summary and Conclusions

ZnS:Mn with BST thin film layer

High k dielectric thin film – barium strontium titanate – was introduced for the insulating layer of TFEL devices. This ZnS:Mn-based TFEL devices (BZB, BZY, and YZY structure) were evaluated by various characterisation techniques such as transferred charge-voltage(Q-V), dynamic capacitance –voltage (C_D-V), internal charge-phosphor field (Q-F_p), luminous efficiency, electroluminescence (EL), and brightness (or luminance).

Through the electro-optical characterisation of TFEL devices with high-κ dielectric layer, the feasibility of using barium strontium titanate material of perovskite solid solution in TFEL display applications has been demonstrated to drop the turn-on voltage and enhance overall L-V (or B-V) characteristics of the LETFEL devices significantly. Threshold voltage was reduced by approximately 50 V in BZY devices (BZY and BZB ~ 135 V; YZY ~ 180 V). In particular, in luminance intensity at L_{40} (brightness at turn-on voltage + 40 V), BZY EL devices showed four times the brightness than the conventional TFEL device with a medium dielectric constant material (ie., Y_2O_3). EL emission spectrum of ZnS:Mn EL devices show a typical yellowish-orange peak of 580 nm wavelength, which has the coordinate of $x = 0.519$ and $y = 0.498$.

In this study, it is found that BZY EL devices showed better device performance in brightness and stability while BZB EL devices had serious problem in device stability which resulted in device breakdown finally. BZB device instability in operation was observed in both of lateral and surface emission. Therefore, it can be understood that BZY EL devices are more effective in device structure.

Total charges delivered to the EL device externally is calculated from transferred charge – voltage (Q-V) curve. Though analysis of Q-V curve, leakage charge density at the interface between BST and ZnS:Mn was 0.26 μC/cm2 at 250 V, while by dynamic capacitance-voltage characterisation, interface charge density(Q_{ss}) at the interfaces of ZnSMn/BST and ZnSMn/Y_2O_3 are 2.04 x 10^{12} cm^{-2} (avg.) and 1.73 x 10^{12} cm^{-2} (avg.), respectively. Conduction charge density during the positive half cycle was 1.3 μC/cm^2, which is obtained easily from internal charge-phosphor field(Q-F_p) loop. In addition, a field

clamping effect in phosphor layer was observed. The field clamping takes place at phosphor field of 1.6 MV/cm.

Luminance depends on a signal frequency large and luminous efficiency (η) of the devices was maintained approximately 1 (lm/W), which is lower than other luminous efficiency of ZnS:Mn-based EL devices [5 (1m/W)][19].

SrS:Cu,Ag with Y_2O_3 layer, Laser annealing and barrier layer effect

In order to improve phosphor's emission characteristics and device performance, barrier layer and pulsed laser annealing methods as device and material engineering effects was applied. Therefore, SrS-based blue emitting EL devices- SrS:Cu, Ag (Cu 0.4 at.% and Ag 0.6 at.%) - are characterised.

With the barrier layer structure, the devices showed high correlation with the barrier layer thickness. From the experiment, 10 nm thickness of the barrier layer(see Figure 6-23) was the optimum condition to enhance SrS:Cu,Ag blue EL emission intensity and device stability.

For pulsed laser annealing effects, the optimum parameters were determined for laser energy density (fluence) and the number of laser irradiation pulses; on average, 1.8 J/cm^2 and 5-time laser pulse, respectively. Regarding the lower laser fluence dependence, it might be predicted that the higher laser fluence and irradiation can cause degradation of the bottom phosphor layer due to laser ablation. In other words, after the annealing, the phosphor layer started to get into multiple re-growing regimes[34]so that in low fluence, crystallinity of the phosphor layer can be improved due to having fine grain layer. In laser irradiation, the lower numbers of the laser pulse can be considered one of the critical factors which are affecting EL emission properties. With the laser irradiation, the insulator-semiconductor interface states as a major carrier injection source could be favourable or detrimental.

In device structure and material engineering, a combination of the barrier layer and pulsed laser annealing(PLA) was introduced. It was confirmed that the barrier layers and pulsed laser annealing in alkaline-earth sulfides have feasibility to improve EL characteristics. As

it is mentioned earlier, particularly, the device performance depended strongly on the barrier layer thickness and laser fluence. For laser annealing, low laser fluence and low numbers of laser irradiation are effective in improving the device performance whether the device has the barrier layers or not.

REFENCES

[1] Cranton W. M., et al., Materials Processing and Device Engineering for Laterally Emitting Thin Film Electroluminescent Miniature Displays, SID Digest of Technical Papers, Microdisplay, 4.10, 2002

[2] Stevens, R. et al., Enhancing the brightness of thin-film electroluminescent displays by improving the emission process, IEEE Electron Device Letters, Vol. 15, No. 3, p. 97, 1994

[3] Sethu, Murugesan, ***PhD Thesis***, Nottingham Trent University, UK 2003

[4] Baukol, Beau, ***PhD Thesis***, Oregon State University, US, 2002

[5] Smith, D. H. Modeling a.c. thin-film electroluminescence devices, Journal of Luminescence, Vol. 23, No. 1-2, pp. 209-235, 1981

[6] Chen, Y. S. and Krupka, D. C. Limitation imposed by field clamping on the efficiency of high-field ac electroluminescence in thin films, Journal of Applied Physics, Vol. 43. No. 10, pp. 4089-4096, 1972

[7] Munasinghe, Chanaka, et al., High Brightness ZnS and GaN Electroluminescent Devices Using PZT Thick Dielectric Layers, IEEE Transactions on Electron Devices, Vol. 52, No. 2. pp. 194-203, 2005

[8] Ono, Yoshimasa A. Electroluminescent Displays, p. 35, World Scientific, 1995 (references therein)

[9] Jona, Franco and Shirane, G. Ferroelectric Crystals, Ch 1. Dover, 1993 (Original publication by Pergamon Press in 1962)

[10] Sawyer, C B and Tower, C H., Rochelle Salt as Dielectric, Physical Review, pp. 269-273, Vol. 35, No. 3, 1930

[11] Ono, Yoshimasa A. et al, Transferred Charge in the Active Layer and EL Device Characteristics of TFEL Cells, Japanese Journal of Applied Physics, Vol. 26, No. 9 Part 1, pp. 1482-1492, 1987

[12] Rack, Philip D. and Holloway, Paul H, The structure device physics, and material properties of thin film electroluminescent displays, Materials Science and Engineering, Vol. R21, pp. 171-219, 1998

[13] Chaichimansour, Mohammad ***PhD Thesis***, Georgia Institute of Technology, USA, 2000

[14] McAthur, R. C. et al., Capacitance-voltage characteristics of alternatinv-current thin-film electroluminescent devices, Applied Physics Letters, Vol. 56 No. 19, pp. 1889-1891, 1990

[15] Kitai, A. H. (Ed.) *Solid State Luminescence – Theory, Materials and Devices*, Chapter 5 (by Mueller, G. O), Chapman & Hall, 1993

[16] Nalwa, Hari Singh, and Rohwer, Lauren Shea (Eds.) *Handbook of Luminescence, Display Materials, and Devices*, Display Devices (Vol. 3) (from Chapter 2, Inorganic Electroluminescent Displays by Rack, Philip D. et al), American Scientific Publishers, 2003

[17] Korea Research Institute of Standards and Science website: http://www.kriss.re.kr/

[18] Ono, Yoshimasa A. et al., Transferred Charge in the Active Layer and EL Device Characteristics of TFEL Cells, Japanese Journal of Applied Physics, Vol. 26, No. 9, pp. 1482-1492, 1987

[19] Rack, Philip D. et al., Inorganic Electroluminescent Displays (from *Handbook of Luminescence, Displays Materials, and Devices. Vol. 3. Display Devices*, Nalwa, H.S. and Rohwer, L. S. Eds.), p. 35, American Scientific Publishers, 2003

[20] Liew, S.C. PhD Thesis, Nottingham Trent University, UK 2003

[21] Liew, S. C. Private Communication

[22] Cranton, W. M., ***Ph.D. Thesis***, Bradford University, UK 1995

[23] Nakanishi, Y. et al. Luminescent Properties of Blue-Emitting SrS:Cu, F Thin Film EL Devices, Phys. Stat. Sol. (b) 229, No. 2 pp. 1011-1014, 2002

[24] Watanabe, H., et al, Crystallization Process of Polycrystalline Silicon by KrF Excimer Laser Annealing, Japanese Journal of Applied Physics, vol. 33 (1-8), pp. 4491-4498, 1994

[25] Mastio, E.A., ***Ph.D. Thesis***, The Nottingham Trent University, UK 1999

[26] Yamashita, N. Photoluminescence properties of Cu^+ centres in MgS, CaS, SrS and BrS, Japanese Journal of Applied Physics, vol. 30 (12A), pp. 3335-3340, 1991

[27] Yamashita, N. et al, Luminescence from the Aggregated Cu^+ Centers in SrS:Cu^+, Japanese Journal of Applied Physics, vol. 1(9A), pp. 3846-3850, 1993

[28] Smet, P. et al, Influence of sintering on photoluminescent emission of SrS:Cu,Ag powders and e-beam evaporated phosphor layers, Solid State Communications, vol. 118, p.59-62, 2001

[29] Park, W. et al, A spectroscopic study on SrS:Cu,Ag two-component electroluminescent phosphors, Journal of Luminescence, vol.87-89, p. 1267-1270, 2000

[30] Park, W. et al., Optical properties of SrS:Cu,Ag two-component phosphors for electroluminescent devices, Applied Physics Letters, vol.74(13), p. 1785, 1999

[31] Sun, S.-S. A new blue emitting TFEL phosphor:SrS:Cu, Displays, vol. 19, p. 145-149, 1999

[32] Li, W.-M., et al, Photo- and electroluminescence of SrS:Cu and SrS:Ag,Cu,Ga thin films, Journal of Applied Physics, vol. 86(9), p. 5017, 1999

[33] Singh, V. P., et al, Modeling of Electron Transport and Luminance in SrS:Cu,Ag ACTFEL Display Device, IEEE Transaction on Electron Devices, vol. 48(10), p. 2242, 2001

[34] Watanabe, H., *et al*, Japanese Journal of Applied Physics, Vol.33, No. (1-8), pp. 4491-4498, 1994

Chapter 7
Conclusions and Remarks for Further Work

Overview

The important factors of the work are reviewed and conclusions drawn with reference to the suggested problems of high driving voltage, device reliability, and blue emitting phosphor material in inorganic TFEL devices. An outline is given of the continuing and planned work produced by this study, and some ideas are presented for further research which might deal with more of the matters relating to growth of high quality perovskite high-κ dielectric ($Ba_{0.5}Sr_{0.5}TiO_3$) thin film and more enhanced TFEL devices.

7.1 Conclusions

The aim of this research was to investigate methods of improving the performance of TFEL devices via material and device engineering. This was addressed via a study of the use of perovskite high-κ dielectrics, laser process, and barrier layer effects in ZnS:Mn and SrS:Cu,Ag based TFEL devices.

Barium Strontium Titanate thin film and TFEL devices

In this project, an optimum growth conditions for r.f.-sputtered BST thin film were established. The substrate temperature, sputtering pressure, oxygen ratio and rf power were 300 ~ 350 °C, 10 mTorr, 10% O_2 mixture and 100 W, respectively. Additional post-thermal annealing process (500 ~ 700 °C) was necessary to improve crystallinity and optical properties of BST thin films.

When BST thin film deposited on Si substrate, it showed (111) orientation preference, which can suggest rotation(45°) of BST thin film during the growth. By this rotation, internal distortion by lattice mismatch between BST thin film and Si substrate can be reduced effectively.

The refractive index of rf sputtered-BST thin film was demonstrated to depend on the substrate temperature (~ 700 °C). It was also found that a laser annealing treatment affected the thickness of the BST thin film, which was reduced by up to 40 nm (1~10 pulses at 300

mJ/cm^2). In addition, a new colour chart of BST thin film was suggested from this study. This was tentatively correlated to a removal of the SiO_2 interface layer which also resulted in a higher dielectric constant for the film.

In electrical and dielectric properties, BST thin film showed high dielectric constant (up to 62.4). The existence of negative fixed oxide charge at the interface between BST layer and Si substrate was confirmed by a rigid parallel shift to the positive voltage in *C-V* characteristic curve. In addition, BST thin film showed frequency dependence in the range of 1 k ~ 1 MHz. Therefore, the flatband voltage of BST MIS capacitor was changed from positive (10k ~ 1 MHz) to negative (1 kHz). Leakage current density of BST thin films was as low as 1.58 μA/cm^2 at 80 V. A conduction current in BST thin film was controlled by electrode-limited at lower electric field and a bulk-limited current mechanism is dominant at higher electric field.

Theoretically, a high-κ dielectric thin film can reduce EL device turn-on voltage effectively. In this study, TFEL devices with perovskite BST layer (BZB and BZY) reduced the threshold voltage by approximately 50 V compared to Y_2O_3-based ZnS:Mn EL devices (YZY). In particular, BZY devices showed far better performance in turn-on characteristics, luminance and device reliability. BZB and BZY devices were four times brighter than YZY devices with a sharp turn-on characteristic while YZY devices only showed a monotonous increase in brightness. The BZB EL devices had similar performance initially in luminance, but their device stability was lower than BZY devices. It may be understood that this instability problem of BZB devices originates from the interface between the top Al electrode and BST thin film top layer. Probably, a low dielectric dead layer (for instance, Al_xO_y layer) was created and thus, degradation of the device seemed to be accelerated as applied voltage increased. Therefore, the BST thin films had a promising feasibility in turn-on characteristics, brightness and device stability for the insulating layer of TFEL device due to the benefit of high dielectric constant material, but the choice of upper insulating layers and electrode interface is evidently critical. For charge storage capacity of BST thin films, the figure is 22.95 μC/cm^2, which is comparable to charge storage capacity of $SrTiO_3$ thin films.

By dynamic capacitance-voltage(C_D-V) characterisation, the interface state density(D_{it}) at ZnS:Mn/BST and ZnS:Mn/Y_2O_3 are obtained as: 2.04 × 10^{12} cm^{-2} for ZnS:Mn/BST and 1.73 × 10^{12} cm^{-2} cm^{-2} for ZnS:Mn/Y_2O_3. This is the key parameter that would help to explain the

performance results. The BZ interface produces a higher density of traps and hence a higher concentration of electron to act as the source of electroluminescent excitation when tunnel injected into the ZnS conduction band. This corroborates the earlier work by the group that indicated that control of this interface is critical for high performance. Hence this research has demonstrated a clear link between measured D_{it} and EL performance.

Blue emitting phosphor, laser annealing, and barrier layer

Based on electro-optical characteristics of SrS:Cu,Ag (Cu 0.4 at.% and Ag 0.6 at%), the device performance had a high correlation with barrier layer thickness. In this study, a 100 Å-thick barrier layer was the optimum condition for improving blue EL emission characteristics of SrS:Cu,Ag. At the same time, it improved the device stability during the operation, which means the barrier layer inserted in the active layer can increase stability of the device.

A lower laser fluence (1.8 J/cm^2) was one of the critical parameters for good performance, because higher laser fluence (and irradiation) might cause overall degradation due to ablation effect. From this study, the optimum conditions for laser annealing on phosphor bottom layers are 1.8 J/cm^2 and 5-laser pulses. In general, the interface state between an insulating layer and a phosphor layer is a major carrier injection source. By inserting the barrier layer and laser annealing treatment, an additional carrier injection source can be created within the phosphor layer. Therefore, overall improvement of EL emission could be achieved by combination of device and material engineering.

7.2 Remarks for further work

Laser annealing on BST thin films

By refractive index, thickness and X-ray diffraction pattern analysis, the laser annealing effects were partially identified as a modification of the crystalline structure and a possible removal of the SiO_2 layer. However, a more detailed structure and chemical analysis using, for example, high resolution TEM and other analytical experiments.

TFEL Devices

In general, ferroelectric or perovskite high-k dielectric materials heavily depend on their bottom electrode. As mentioned above, the BZB device's instability seems to be related to the electrode dependence. Hence, there can be two options for this matter: One is to investigate other metal electrodes including transparent conduction materials such as ITO. The other option is a multi-layer structure for Al electrode, looking at the use of interlayer to act as barriers.

Deposition technology for high quality dielectric material

As a solid solution material, it is one of the most important things to grow high quality high-κ dielectric thin film not only for TFEL device application, but also for universal applications. In order to achieve this requirement, pulse laser deposition (PLD) or atomic layer epitaxy (ALE) can be an alternative method for growth high quality BST thin film. In particular, PLD technique is already well known for a suitable deposition technology in complex multi-elementary materials such as BST or complex superconducting materials. Still it can give an opportunity to grow high quality thin films.

Finally, it would be interesting to study the combined benefits of the enhanced insulated/phosphor interface demonstrated here, in combination with the laser processed and barrier layer structure of blue emitters.

Appendix A $C(V_G)$ Curve

Typical capacitance-voltage (*C-V, or* $C(V_G)$) characteristic curves in high-frequency for p- or n-type semiconductors are already shown in Figure 3-10. To understand the observed patterns of the *C-V* properties of the MIS capacitor, it is necessary to consider how the charge inside the MIS capacitor responds to the applied ac signal when the dc signal is changed from accumulation to inversion through depletion.

As stated previously, majority electron carriers build up at the oxide-semiconductor interface in accumulation condition (see Figure 4-2). Furthermore, the majority carriers - electrons - are the only one type of carriers participated in accumulation condition. The accumulation is the characteristics of the dc bias applied to the device. The MIS capacitor system in this accumulation condition normally changes very rapidly because there are no immobile ionized charges involved and the only majority electron carriers respond. The differential change in voltage(ΔV) across the MIS device causes a corresponding differential change(ΔQ) in charge on the metal gate and at the semiconductor surface by the capacitance of a device defined as $C = dQ/dV$. The internal charge distribution of the MIS capacitor in accumulation is the same as that of the general parallel-plate capacitor as illustrated in Figure 4-2(B). This capacitance in accumulation shows the maximum capacitance in *C-V* characteristic curve. The capacitance of the accumulation condition (C_{acc}) can be expressed as the equation below:

$$C_{acc} \approx C_{oxide} = \frac{\varepsilon_{ox}\kappa_o A}{t_o} \quad \text{or} \quad C^*_{acc}\left(=\frac{C_{acc}}{A}\right) = \frac{\varepsilon_{ox}\kappa_o}{t_o} \qquad \textbf{Equation A-1}^{\circ}$$

where A, κ_o, and t_o are the area of the MIS capacitor, permittivity in vacuum (8.854×10^{-14} F/cm), and thickness of the oxide, respectively.

Once the capacitance in accumulation condition is measured, the dielectric constant of the oxide thin film (i.e., Y_2O_3, or BST) can be calculated by using Equation A-1. Figure A-1 shows a typical *C-V* curve of the MIS capacitor with 160nm thick BST layer. Thus, for an example, the calculated dielectric constant of 160 nm-thick BST layer is approximately 62.5 by Equation A-1.

In depletion region, the charge per unit area due to uncompensated ionized donors is + qN_dW [C/cm²] (see Figure 4-2(C)). Furthermore, the negative charge, $-Q_m$, on the metal gate should be balanced by the positive charge, $+Q_s$ in the semiconductor in magnitude. Therefore, this condition has the same configuration of series connected two parallel-plate capacitors conceptually (see Figure A-2 (b)). The capacitance of the semiconductor (i.e., the depletion layer capacitance) is $\frac{\varepsilon_s \kappa_0 A}{W}$. The total capacitance in depletion condition ($C_{depletion}$) is

$$C_{depletion} = \frac{C_{oxide} \cdot C_s}{C_{oxide} + C_s} = \frac{C_{oxide}}{1 + \frac{\varepsilon_{ox} W}{\varepsilon_s t_o}} \qquad \textbf{Equation A- 2}$$

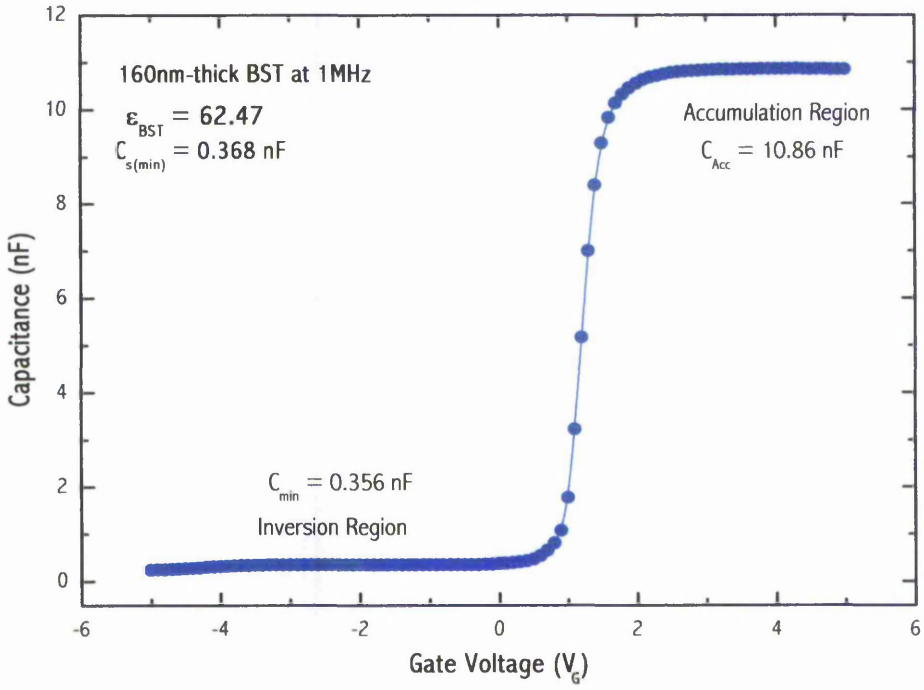


Figure A-1 A real MIS capacitor *C-V* curve from Si/BST/Al structure at 1MHz.

From Equation A-2, as the depletion region width increases, the depletion capacitance decreases correspondingly when the depletion bias ($V_G < 0$) increases because the thickness of the oxide layer remains constant. Once the oxide capacitance is obtained, the depletion

° Often, capacitance has double meanings in practice so that it can be used as capacitance per unit area(C/A) for convenience.

capacitance becomes a function of the depletion region width. The total depletion capacitance ($C_{depletion}$) is normally less than the oxide capacitance, C_{oxide}. It is confirmed in the *C-V* characteristic curve of the MIS devices.

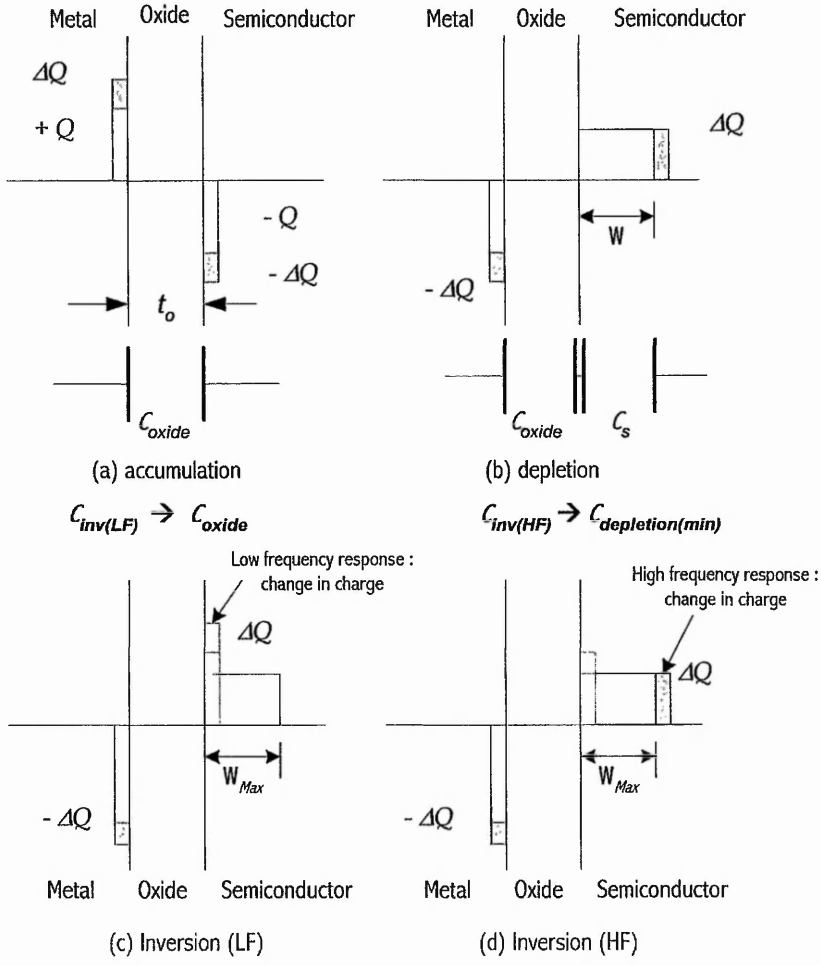


Figure A-2 The block diagram and its equivalent circuits of the internal charge distribution in response to the gate dc bias(V_G) and ac probe signal:(a) accumulation $C_{total} = C_{oxide}$, (b) depletion $C_{total} = (C_{oxide}\ C_s)/(C_{oxide} + C_s)$, (c) inversion in low frequency $C_{total} = C_{inv(LF)} = C_{oxide}$, and (d) inversion in high frequency $C_{total} = C_{inv(HF)} = C_{depletion(min)}$.[1]

With the gate bias sufficiently increased negatively, the MIS device goes into the inversion condition. At this situation, the negative charge on the metal gate and the positive charge in the semiconductor must be balanced in their magnitude ($|-Q_m| = +Q_s$) like the depletion case. However, inside the semiconductor, total charge consists of the uncompensated ionized donor carrier charge($Q_d = qN_dW$) in the depletion layer and the hole charge(Q_p) due to inverted region

[1] Pierret, R. F., Field Effect Devices, 2nd Ed., Ch 2. Addison-Wesley, 1990

(p-channel). In addition, the width of the depletion region will be maximised at W_{max}.

$$Q_s = qN_d W_{max} + Q_p = |-Q_m| \qquad \textbf{Equation A-3}$$

From Equations A-3 and 4-10, the charge per unit area(C/cm^2) in the depletion region at true inversion condition is

$$Q_{d(inv)} = qN_d W_{max} = 2[\kappa_o \varepsilon_s q N_d \phi_B]^{1/2} = 2\left[\kappa_o \varepsilon_s N_d kT \ln(\frac{N_d}{n_i})\right]^{1/2} \qquad \textbf{Equation A-4}$$

In the operation condition of the inversion, there are two different differential changes in charge(ΔQ) in response to the differential change in applied bias(ΔV) on the metal gate: (a) a differential charge change in the inversion layer and (b) a differential charge change in the depletion layer. In particular, the differential charge change in the inversion region is due to the minority hole carrier diffusion across the depletion region from the bulk n-type semiconductor and thermally generated EHPs(electron-hole pairs) within the depletion region.[2] These two processes can supply holes at a given specific rate. Therefore, it might be impossible that the charge density in the inversion region can change immediately in respect with ac signal. If the frequency of the applied ac small signal is high frequency, the charge in the inversion region can not respond to that high frequency. As a result, the charge in the depletion region can respond to the change instead. The frequency dependence of the differential change in charge in inversion condition is illustrated in Figure A-2 (c) and (d). Remind that the MIS device capacitance is the property of ac signal so that the unchanged charge density can not contribute to the dynamic capacitance of the device.

Within the range of low-frequency (usually ~ 100kHz), the inversion capacitance will be the same as that of the accumulation: $C_{(inv)LF} \approx C_{acc}$ while the inversion capacitance at high frequency will have the minimum value of the depletion capacitance($C_{depletion(min)}$) when the depletion region width is in the maximum(W_{max}):

[2] Nicollian, E.H. and Brews, J.R., MOS Physics and Technology, John Wiley, 1982

$$C_{total} = C_{inv(HF)} = \frac{C_{oxide} \cdot C_s(W_{max})}{C_{oxide} + C_s(W_{max})} = \frac{C_{oxide}}{1 + \frac{\varepsilon_{ox} W_{max}}{\varepsilon_s t_o}} \quad \text{(HF)} \qquad \textbf{Equation A-5}$$

$$\cong C_{depletion(min)} \big|_{\omega \to \infty}$$

or

$$\frac{C_{total}}{C_{oxide}} = \frac{1}{1 + \frac{\varepsilon_{ox} W_{max}}{\varepsilon_s t_o}} \qquad \textbf{Equation A-6}$$

To create the depletion region and the surface inversion layer, the applied bias should be large enough. The critical voltage to create this condition is called the *threshold* voltage. When a potential V_G is applied to the device, the potential is dropped across the oxide layer and the depletion region, respectively. Therefore, from the Equation 4-13, the relationship between the applied voltage and the internal potential drop will be

$$V_G = V_{oxide} + \phi_{s(depletion)} = -\frac{Q_d}{C_{oxide}} + \phi_{s(depletion)} \qquad \textbf{Equation A-7}$$

where V_{oxide} and $\phi_{s(depletion)}$ are the potential drops across the oxide layer and the semiconductor depletion region, respectively.

By using the Equation A-3, A-4, and A-7, the *threshold* voltage(V_T) can be rewritten as following:

$$V_T = \phi_s(inv.) + \frac{Q_s}{C_{oxide}} = -2\phi_B - \frac{Q_{d(inv)} + Q_p}{C_{oxide}}$$

$$\cong -2\phi_B - \frac{Q_{d(inv)}}{C_{oxide}} \left(Q_{d(inv)} >> Q_p \right) \text{ (ideal MIS)} \qquad \textbf{Equation A-8}$$

$$= -2\phi_B - \frac{qN_d W_{max}}{C_{oxide}}$$

By the Equations 4-8 and A-7, another different format of the depletion width can be obtained:

$$W = \frac{\varepsilon_s \kappa_o}{C_{oxide}} + \left[\left(\frac{\varepsilon_s \kappa_o}{C_{oxide}} \right)^2 - \frac{2\varepsilon_s \kappa_o}{qN_d} V_G \right]^{1/2} \qquad \textbf{Equation A-9}$$

According to the surface potential (ϕ_s), space charge density(Q_s, C/cm^2) variation is shown in Figure A-3, which is showing the general properties. The space charge density on the left side region is positive when the negative surface potential is applied for depletion and inversion regions. The surface potential is positive, negative space charge density on the right means the surface potential is positive and the device is under the accumulation condition.

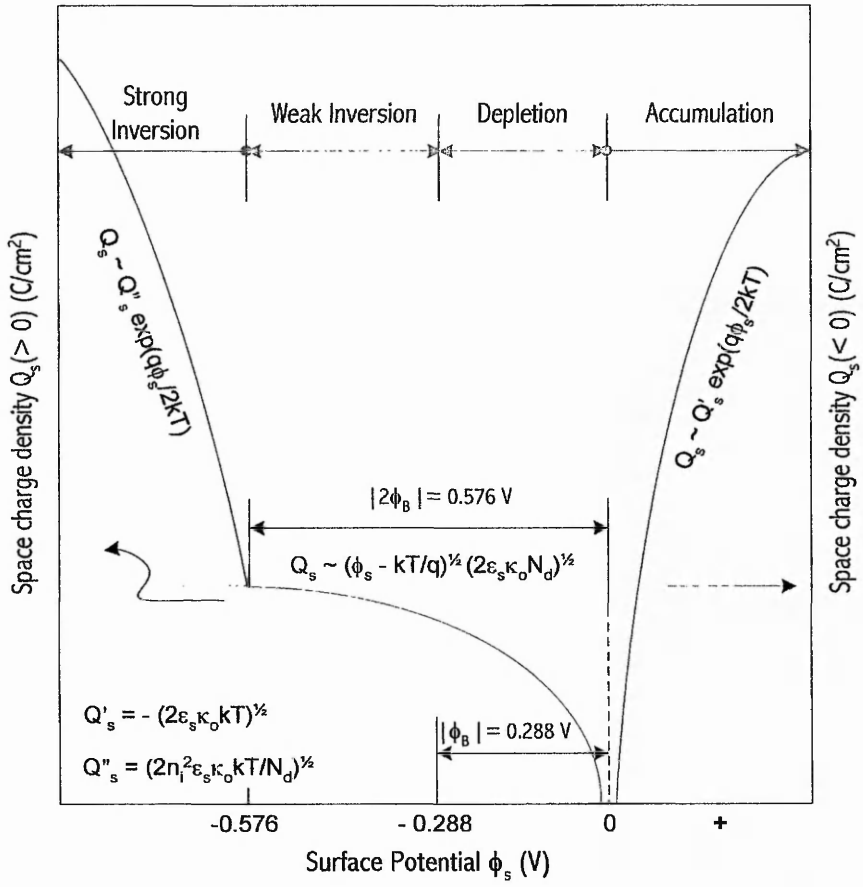


Figure A-3 The space charge density variations with applied surface potential condition for n-Si[1,2,3, 4].

The exact equation of the space charge density as a function of the surface potential can be

[3] Sze, S.M. Physics of Semiconductor Devices, 2nd Ed. Ch 7., John Wiley, 1981

obtained easily from the literatures [1,2,5]. Substituting Equation A-9 into the Equation A-6 results in

$$\frac{C'_{total}}{C'_{oxide}} = \frac{1}{\left(1 - \frac{2C'_{oxide}V_G}{\varepsilon'_s q N_d}\right)^{1/2}} \qquad \textbf{Equation A-10}$$

$$C'_{total} = \frac{dQ_s}{dV_G};\quad C'_{oxide} = \frac{\varepsilon'_{ox}}{t_o}$$

This equation can be applied over the range from $V_G = 0$ to $V_G = V_T$.

[4] Streetman, Ben G., Solid State Electronic Devices, 5th Ed. Prentice-Hall, 1990
[5] Greve, D. W., Field Effect Devices and Applications, Prentice-Hall, 1998

Appendix B Work function, flat band Voltage, and additional charges

In the case of the real MOS devices, the work function of the gate metal (Al) and the semiconductor substrate (e.g., n-type silicon) is not the same. Unfortunately, there are inevitably some charges at the interface between the oxide and the semiconductor. Furthermore, within the oxide the oxide layer is not perfect insulator so that it has some charges inside. These real situations as non-ideal general cases should be taken into account.

In general, assumed that there is no work difference between the gate metal and the semiconductor in the ideal MIS structure ($\phi_{ms} = \phi_m - \phi_{si} = 0$). (See Figure 4-2) From the Figures 4-2, 4-3, and 4-4, the relationship of the work difference in ideal MOS device will be arrived

$$\phi_m = \phi_{si} = \chi_{si} + (E_c - E_{Fs})_{bulk} = \chi_{si} + (\frac{E_g}{2q} - \phi_B) \quad \text{(ideal case, for n-type)} \quad \textbf{Equation B-1}$$

where ϕ_m and ϕ_{si} are the work functions of metal electrode and semiconductor, respectively. E_g and χ_{si} are the electron affinity and the energy band gap of the semiconductor, respectively.

Although the work function of the semiconductor depends on its doping profile, the actually work function difference in the Al - Si system is varied accordingly. Therefore, the work function potential difference (ϕ_{ms}) can be positive or negative according to the semiconductor doping profile. The ideal case should be modified to account for the real work function (potential) difference between the gate metal and the semiconductor material.

In the case of metal-semiconductor devices, due to the negative work function difference, the electrons move toward the semiconductor region to maintain the Fermi level throughout the device at thermal equibrilium state. However, MIS devices have the oxide layer between the metal and semiconductor so that actual charge transfer does not take place. Instead of that, the band bending at the semiconductor surface occurs to sustain the Fermi energy level within the entire device. Therefore, the surface is negatively charged at equilibrium. The oxide layer can reduce the actual surface potential (i.e., barrier) so that the modified work function equation can be obtained:

$$\phi_{ms} = \phi_m - \phi_{si} = \phi'_m - \chi' - (E_c - E_{Fs})_{bulk} = \phi'_m - (\chi' + \frac{E_g}{2q} - \phi_B) \quad \textbf{Equation B-2}$$

where $\phi'_m = \phi_m - \chi_{oxide}$, and $\chi' = \chi_{si} - \chi_{oxide}$.

The potential difference (V_{bi}) across the oxide layer and the semiconductor surface like the built-in potential difference in a *p-n* junction is created and is equal to the work function potential difference ($V_{bi} = \phi_{ms} = -(V_{oxide}|_{surface} + \phi_s|_{surface})$). The flat band voltage is literally defined as the externally applied voltage to prevent the band bending and achieve the flat energy band in the semiconductor ($V_{FB} = \phi_{ms}$). In the flat band condition, the semiconductor surface potential (ϕ_s) is zero. In ideal MIS devices, the flat band voltage (V_{FB}) is zero, but the zero flat band voltage in real devices is not the case due to the work function difference, and existence of various charges within the oxide layer and at the interface between the oxide and the semiconductor. When the gate voltage is applied, the potential drops across the oxide layer and the semiconductor surface will change (Eq. 4-13):

$$\begin{aligned} V_G = \Delta V_{oxide} + \Delta\phi_s &= (V_{oxide} - V_{oxide}|_{surface}) + (\phi_s - \phi_s|_{surface}) \\ &= V_{oxide} + \phi_s + \phi_{ms} \quad (\leftarrow \phi_{ms} = -V_{oxide}|_{surface} - \phi_s|_{surface}) \end{aligned} \quad \textbf{Equation B-3}$$

In non-ideal MIS devices, in general there are four types of charges which can give contribution in metal-insulator-semiconductor system: ① oxide fixed (or fixed oxide) charges(Q_f); ② mobile ionic charge (Q_m), ③ oxide trapped charge(Q_{ot}), and ④ interface trapped charges(Q_{it}). These standard terminologies were established by B. E. Deal[1] for charges based on the thermally-grown oxidized silicon, but now their definitions are extended to general cases. Due to these charges, the flat band voltage is affected. As a result, the threshold (or turn-on) voltage should be modified. Of course, other instabilities exist within the MIS capacitor devices, but in this section, the four charges will be discussed mainly. The schematic diagram for various charges within the oxide and at the interface between the oxide and semiconductor is given in Figure B-1 and they can be distinguished as followings:[2]

Q_f - Fixed oxide charge: Due to the structural defects, these charge exist in the oxide layer less than 2 ~ 2.5 nm from the Si-SiO_2 interface.

---

[1] Deal, B. E. Standardized Terminology for Oxide Charges Associated with Thermally Oxidized Silicon, IEEE Trans. Electron Devices, 27(3), p. 606, 1980

[2] Barbottin, G. and Vapaille, A., *Instabilities in Silicon Devices - Silicon Passivation and Related Instabilities*, ch. 4., Elsevier, 1986

Q_m - ***Mobile ionic charge***: These mobile ionic charges originate from common contaminating agents (impurities) such as alkali-metal elements - Na^+, K^+, and others during the process of sample preparation or handling. They present in the bulk of oxide layer

Q_{ot} - ***Oxide trapped charge***: They can be positive or negative due to holes or electrons which are trapped in the bulk of oxide region. One of the trapping mechanisms is Fowler-Nordheim tunnelling.

Q_{it} - ***Interface trapped charge***: They are also positive or negative due to various defeats, impurities and other processes. The important point of these charges is their location. Interface trapped charges are located at the oxide-semiconductor interface and exists within the silicon-forbidden gap by the discontinuity of the periodic lattice structure at the surface of a crystal. In addition, they can be charged or discharged by the semiconductor surface potential. Once, these charges have been called surface states, fast states or interface states.

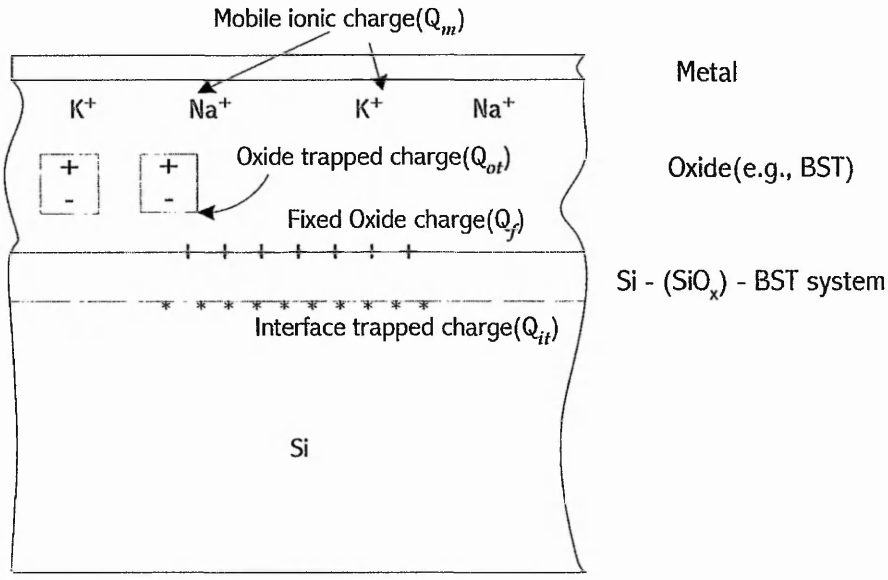


Figure B-1 Visualized the various charges and their locations within the oxide layer and at the oxide-semiconductor interface[3]

Thus, the flatband voltage (V_{FB}) is determined by the metal-semiconductor work function difference(ϕ_{ms}) and the various oxide charge effect which described above. The general

[3] Sze, S.M. Physics of Semiconductor Devices, 2nd Ed. Ch 7., John Wiley, 1981

flatband voltage has an equation as Equation B-4[4] below.

$$V_{FB} = V_G = \phi_{ms} - \frac{1}{C_{oxide}}(Q_f + \gamma Q_m + \gamma Q_{ot} + Q_{it}(\phi_s)) \qquad \textbf{Equation B-4}$$

Assumed that the location of the fixed oxide charge (Q_f) can be considered at the interface and the other two charges - mobile and oxide trapped - are distributed throughout the entire oxide region. When these charges are located at the oxide-semiconductor interface, the greatest effect is possible. If the distributed charges might be located at the metal-oxide interface, they do not any effect on the flatband voltage. Therefore, it is necessary to introduce a factor (γ) which can account for possible charge distribution. The factor is defined by

$$\gamma = \frac{\int_0^{t_o} (x / t_o)\rho(x)dx}{\int_0^{t_o} \rho(x)dx} \qquad \textbf{Equation B-5}[4]$$

where $\rho(x)$ is oxide trapped or mobile ionic charge per unit volume and one dimensional function in respect with x-axis and t_o is the width of the oxide region. If the charges are at the oxide-semiconductor interface($x = t_o$), γ is 1 and $\gamma = 0$ when the charges at the metal-oxide interface ($x = 0$). Assumed that Q_m and O_{ot} have the constant value throughout the oxide region.

The total effective oxide charge distributed in the oxide layer simply can be considered as $Q_i = Q_f + Q_{ot} + Q_m + Q_{it}$. The total positive charge* in the oxide can induce the negative charge in the semiconductor. As a result, these charges in the oxide and at oxide-semiconductor interface can increase further band bending without external bias. Normally, this effect is undesirable so that it should be removed by applying external negative bias with the same magnitude and the flat band condition must be achieved effectively. Therefore, using the total effective oxide charge concept, the simplified form for the modified flat band voltage in real MIS devices can be rewritten, as given in Equation B-6 below.

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_{oxide}} \qquad \textbf{Equation B-6}$$

---

[4] Schroder, Dieter K., Semiconductor Material and Device Characterisation, Ch 6., John Wiley, 1990

* The sign of the charges can be positive or negative, but generally it has positive value.

The voltage to achieve the flat band condition is added to the threshold voltage equation (Eq. A-8) in ideal MIS devices:

$$V_T = \phi_{ms} - \frac{Q_i}{C_{oxide}} - \frac{Q_{d(inv)}}{C_{oxide}} - 2\phi_B$$ **Figure B-7**[5,6]

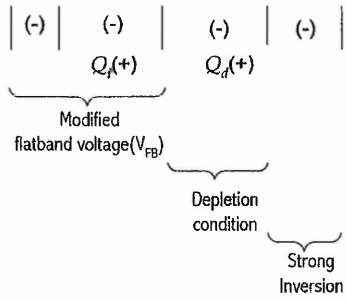


Figure B-2 The threshold voltage equation(V_T) and the signs of its components in the case of n-type Si semiconductor[6] (The Fermi level(E_{Fs}) is used as potential reference for ϕ_B, which is positive always in n-type semiconductor)

For the p-channel MIS device (n-type semiconductor), the first two terms in Figure B-7 mean the modified flatband voltage and its value is generally negative. The third and last terms show the potential in depletion and strong inversion condition, respectively. The final term is negative*. In fact, the resultant value of the equation is negative as expected for the MIS capacitor with p-channel.

[5] Grove, A. S. Physics and Technology of Semiconductor Devices, Ch. 9 and 12, John Wiley & Sons, 1967
[6] Streetman, B. G. and Banerjee, S. Solid State Electronic Devices, 5th Ed. p. 255-285, Prentice-Hall, 2000
*ϕ_B is negative due to E_{Fs} as potential reference ($\phi_B = E_{Fs}-E_{i(bulk)}$).

Appendix C Crystal Field Theory in Phosphors

For a better understanding of the transition phenomenon in phosphor materials, it is necessary to have some background knowledge of crystal field theory. The host material, SrS, has rocksalt (often as it called NaCl structure) structures and at the same time, it has octahedral structure properties. ZnS crystal depends on its structures - zinc blende and Wurtzite. For the zinc blende structure, ZnS has the sulfur octahedral surroundings without Zn atom and Zn atom surrounded in tetrahedral structure by sulfur atoms[2]. Unlike ZnS, alkaline earth metal (Sr) has six sulfur atoms as the nearest neighbours, which is called a coordinate number (CN number). For activators (Cu, Ag) to remain in the octahedral environment, we need to understand crystal field theory, or ligand field theory (in fact, ligand field theory is more general; it includes crystal field theory and molecular orbital (MO) method). It is a general tool to understand a transition metal's spectroscopic properties - absorption and emission transition.

By orbital quantum number (l= n-1; n is the principal quantum number), a d-block transition metal element has microstates (m_l = - l ~ + l; total microstates are 2(l + 1)) and under the octahedral environment their five orbitals can experience splitting. Therefore free ion d-orbitals are splitting into higher states (d_{z^2} and $d_{x^2-y^2}$) and lower states (d_{xz}, d_{xy}, d_{yz}). The difference between two states is often expressed as $10Dq$ or Δ_o. $10Dq$ in O_h or Δ_t in T_d shows the strength of the crystal field. The higher states (e_g) are located at higher level by (3/5)Δ_o and the lower states(t_{2g}) can be lowered by (2/5)Δ_o from the free ion, respectively[1]. A typical diagram of crystal field splitting in octahedral and tetrahedral symmetry is shown in Figure C-1.

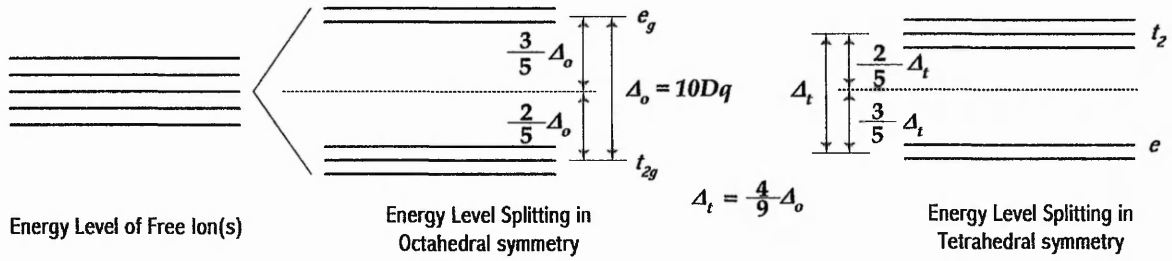


Figure C-1. Crystal field splitting diagram in octahedral or tetrahedral symmetry in d-block[1]

[1] Duffy, J.A., Bonding, Energy Levels & Bands in Inorganic Solids, Ch 1 and 2, 1990 Longman

ZnS(zinc blend) has tetrahedral symmetry structure, though it could have octahedral environment without the central metal ion[2], crystal field splitting is an opposite from the octahedral case. In this section only the octahedral symmetry will be discussed briefly.

Table C-1 Quantum numbers (QN) and Angular momentums (AM)
n = 1 , 2, 3, ~ ,infinite(∞), but only for 1, 2, and 3 (= n) for explanation

Principal QN	n	1	2			3					
Orbital QN	l	0	1			2					
Orbital		s	p			d					
Spin	s	± ½	± ½			± ½					
Orbital AM	m_l	0	-1	0	+1	-2	-1	0	+1	+2	
Spin AM	m_s	± ½	± ½			± ½					

The spin can couple with the orbital angular momentum (positive or negative) so that the spin-orbit coupling can give rise to two different energies. For the s orbital, there is no orbital angular momentum (see Table C-1), but for p orbital, there are two different energy levels by spin-orbit coupling, which is called j ($j = l \pm ½$)[1].

If a system has more than one electron, a new quantum number (J), which is analogous to j in one electron system, is introduced. It is called Russell-Sanders scheme, or coupling. J = (L-S), (L-S)+1, ~ , (L+S). L as spectroscopic term depends on orbital quantum number (l). Table C-1 and C-2 show summary of some quantum numbers, angular momentum, spectroscopic terms, and multiplicity.

For an example, d-block elements have basically l = 2 (d orbital is l (= 2)) so that the value of L is the vector sum of each orbital quantum number. For the Cu^+ ion its electron configuration is [Ar] $3d^{10}$. Five d-orbitals are filled with two electrons so L = 0 (S). Total spin, S°, is zero due to every microstate of five d-orbitals having two electrons, which are +½ and -½ , respectively. Therefore, $L = S = 0$. In general, 2S+1 is called the multiplicity and used instead of S. The meaning of the multiplicity is the sum of the number of unpaired electron(s) and 1[1]. If one

[2] Cullity, B.D., Elements of X-ray Diffraction, 2nd Ed. Ch 2., Addison-Wesley, 1978
° Total spin(S) and total orbital quantum number (L= 0 (S)) are different. The latter letter(S) is used instead of number zero as spectroscopic term.

element has various spectroscopic terms at the same time, the maximum value of the multiplicity (unpaired electron) is the ground state of the element (Hund's rule). In this case, the multiplicity (2S+1) of Cu^+ ion = 1. With obtained two values, the ground state of Cu^+ ion can be expressed in full spectroscopic terms $(^{2S+1}L_J)$[3] so that the ground state term is ^1S (see Table 2-11). Ag^+ ion has the same electron configuration with higher shell ($n = 4$) so Ag^+ ion has the same spectroscopic terms (^1S). The excited electron configurations of Cu^+ and Ag^+ ions are [Ar] $3d^94s^1$, and [Kr]$4d^95s^1$, respectively. Therefore, we need to think of just d^9 configuration. The d^9 configuration is the same as d^1 configuration in possible states. In this case, l has only one value; 2(D). As a result, L has the same value, too because there is only one electron. Total spin (S) from one electron is +½ and the multiplicity (2S+1) is 2. Therefore, the possible spectroscopic term is ^2D.

Table C-2 Total orbital quantum number, spectroscopic term, total spin quantum number, and multiplicity

Total Orbital QN	L	0	1	2	3	4	....
Spectroscopic terms		S	P	D	F	G	....
Total Spin QN	S	0 (paired)	½	1	3/2	2	....
Multiplicity	2S +1	1	2	3	4	5	...

More detailed meaning of the spectroscopic terms is that capital letter spectroscopic terms are orbital degenerate and multiplicity is spin degenerate so total degeneracy of a state is the product of its spin and orbital degeneracies. In degeneracy, A(singlet), E(doublet), and T(triplet) are used.

According to the strength of the crystal field, there are two types; strong field and weak field. Under these fields, electronic states of free ions give rise to much more detailed degeneracy states. Table C-3 shows the summary of electronic states of the ion in octahedral field.

The multiplicity (2S+1) is the same value in the octahedral field. Now we can estimate the emission transition of Cu^+ in SrS host materials by using the Table 2-11. One electron s orbital should be considered; ^3E_g (excited state; $3d^94s^1$) → $^1A_{1g}$ (ground state; $3d^{10}$). The transition has in agreement with some reports from others [4,5,6]. From the transition, the corresponding

[3] At the terms $(^{2S+1}L_J)$, often J can be omitted.

[4] Park, W., et al. A spectroscopic study on SrS:Cu,Ag two-component electroluminescent phosphors, J. Luminescence vol. 87-89, pp. 1267-1270, 2000

emission wavelength is 479 nm.[7]

Table C-3 Splitting states of free ion and in octahedral symmetry[8]

Electronic states of the free ion	Electronic states of the ion in Octahedral field
S	A_{1g}
P	T_{1g}
D	$E_g + T_{2g}$
F	$A_{2g} + T_{1g} + T_{2g}$
G	$A_{1g} + E_g + T_{1g} + T_{2g}$
H	$E_u + T_{1u} + T_{1u} + T_{1u}$

[5] Li, W.-M., et al. Photo- and electroluminescence of SrS:Cu and SrS:Ag,Cu,Ga thin film, Journal of Applied Physics, vol. 84(9), p. 5017, 1999 (reference therein)

[6] Tong, W., et al. In situ annealing studied of molecular-beam epitaxial growth of SrS:Cu, Applied Physics Letters, vol.74(10), p.1379, 1999

[7] Ohmi, K. et al. Blue SrS:Cu thin-film electroluminescent devices grown by hot-wall deposition using successive source supply, Applied Physics Letters, vol. 73(13), p. 1889, 1998

[8] Cotton, F.A., Chemical Application of Group Theory 3rd Ed., Ch 9, JohnWiley and Sons, 1990

Appendix D Transition of Mn^{2+} in ZnS:Mn phosphor

The luminescent wavelength of Mn^{2+} is sensitive to the intensity of the crystal field and various emission bands are observed due to Mn^{2+} sites in a host material. For a ZnS host material, luminescence properties and crystal field parameters for Mn^{2+} are summarised in Table D.1. Mn^{2+} ion is isovalent with the Zn^{2+}cation which is replaced and difference in ionic radius between two ions has only 8%. This lead to high Mn solubility in ZnS host material, uniform activator distribution, and a large cross-sectional impact excitation[1].

Table D. 1 Luminescence properties and crystal field parameters for Mn^{2+} in ZnS host crystal[1]

Crystal symmetry	Site	CN	Wavelength(nm)	Decay time
T_d	Zn	4	591 nm	0.25 msec
Dq (cm^{-1})	**B(cm^{-1})**	**C(cm^{-1})**	**Wavelength**	**Inversion symmetry**
520	630	4	591 nm	u

Dq is the crystal field energy and $10Dq$ (=Δ) is energy difference in crystal field B and C are Racah parameters. All parameters mean energy in unit of cm^{-1} (wavenumber = 1/wavelength). u means no inversion symmetry.

The ground state electronic configuration of divalent Mn ion (Mn^{2+}) is $3d^5$ (^6S for spectroscopic term or simply *Term*)†, in which the electrons can be strongly distorted by the crystal field (or ligand field) of ZnS host materials. Therefore, the $3d^5$ excited states must be considered by using the symmetry of the host material. The lowest excited state of $3d^5$ electrons in T_d(tetrahedral) symmetry site of ZnS is $^4G(^4T_1)$ level (See Figure D-1). In fact, all excited states from the d^5 configuration have lower multiplicity. As a result, they are quartets or doublets which the superscript on the left of the Term, 4, means. Energy level diagram for the d^5 ion in the weak crystal field for tetrahedral coordination is shown in Figure D-1[2]. In Figure D-1, the luminescent emission of Mn^{2+} corresponds to the transition of $^4G \rightarrow {}^6S$ ($^4T_1 \rightarrow {}^6A_1$) under the tetrahedral structure of ZnS host material. A transition between the initial and the final states having the same parity is forbidden (Laporte's rule)[1]. Thus, the transition in *d-d* intra-shell is

[1] Shionoya, S. and Yen W.M. Phosphor Handbook, CRC, 1998

† L= 0, S = 5/2, 2S+1 = 6, and L=5/2 for the ground state of Mn^{2+} ion. L must be the largest value when the orbital filled more than a half.

parity forbidden, but in tetrahedral coordination, there is no inversion symmetry. Therefore, *d-d* transition can be possible.

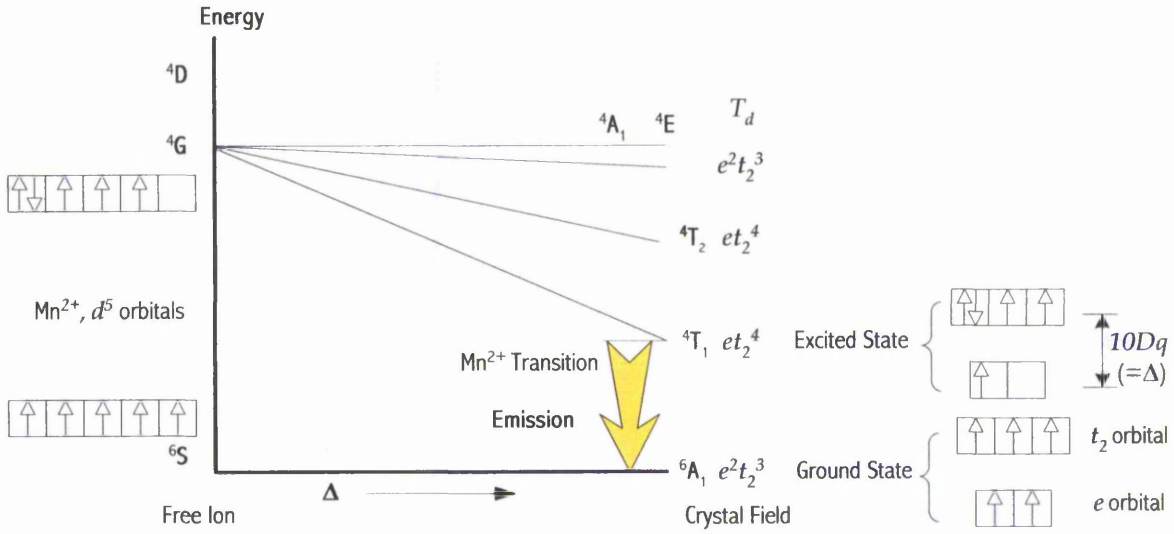


Figure D-1 Energy level diagram of Mn^{2+} ion in the crystal field for the tetrahedral coordination: corresponding transition is $^4T_1(^4G) \rightarrow {}^6A_1(^6S)$[2].

The energy level diagram which is called Tanabe-Sugano diagram in Figure D-1 explains important information about emission. The steep slope of the lowest excited level ($^4T_1$) suggests a broad emission, violation of selection rule, and the transition decay time of order of msec. The broad emission is originated from the different configuration between the ground and excited states (see Figure D-2). The broad emission from the excited energy to the ground state having the equilibrium distance is due to having offset distance in configurational coordinate diagram. The configurational coordinate diagram is given in Figure D-2. This decay time is getting shorter in the tetrahedral coordination due to no centre of inversion symmetry of the ZnS host material[1,2].

[2] Chaichimansour, M. PhD Thesis, Georgia Institute of Technology, 2000

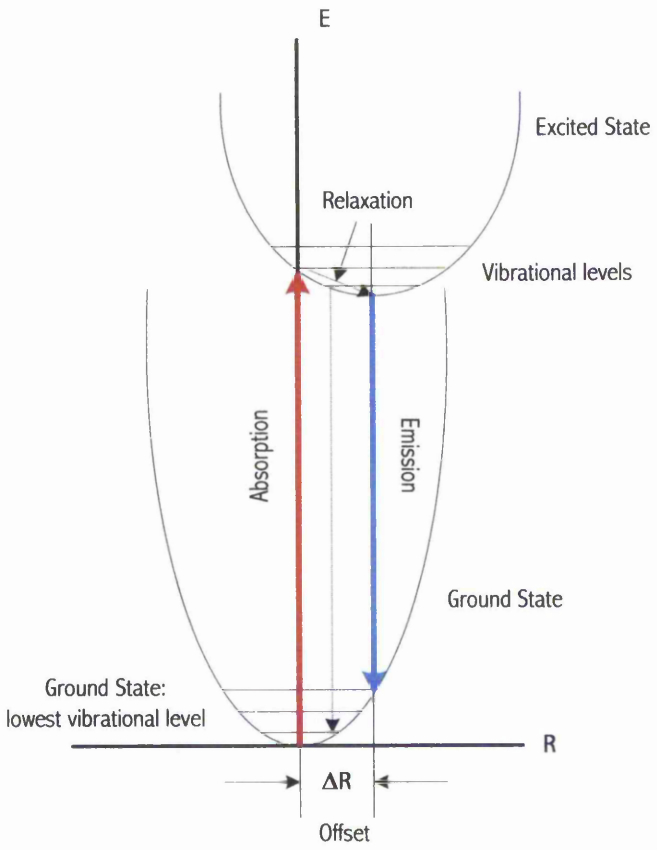


Figure D.2 A configurational coordinate diagram for Mn^{2+} broad emission transition band in ZnS host materials

Appendix E Definition and Unit of Luminance[1]

Candela (cd, SI unit)

The SI unit for luminance is candelas per square meter (cd/m^2) which is equivalent to (1/3.42626) foot-Lambert(fL), or 1 fL = 3.42626 cd/m^2. As a SI unit, the candela is the luminous intensity, in a give direction, of a source that emits monochromatic radiation of frequency 540 x 10^2 Hz and that has a radiant intensity in that direction of (1/683) watt per steradian.

Steradian (sr, SI unit)

The steradian is the solid angle which has its apex on the centre of a sphere, and cuts into this sphere surface an equivalent area of one square which has its side equal to the sphere radius. The space described by a solid angle could be the interior of a conical or pyramidal surface.

Lumen (lm)

The SI unit of luminous flux, defined as the luminous flux emitted by a uniform point source, of intensity one candela(cd), in a cone of solid angle one steradian. Thus, 1 lm = (1/4pi) cd.

1 foot-candle = 10.764 lx (lux)

1 phot = 10000 lx

1 cd/in^2 = 1550.003 cd/m^2

1 stilb = 10000 cd/m^2

1 lambert = 3183.10 cd/m^2 = (1/pi) cd/cm^2 = 1 $lumen/cm^2$

1 foot-lambert (ft.L) = 3.426 26 (3.4262591) cd/m^2 = [1/pi]cd/ft^2 = [1/144pi] cd/in^2 = 1.0764 mL

[1] Cohen, E. Richard, et al (Editors), Unit, Nomenclature, AIP Physics Desk Reference 3rd Edition, Springer-Verlag, New York, 2003; The penguin dictionary of Physics, 3rd Edition, Market House Book Ltd, 2000; Scientific Unit Conversion -A practical guide to metrication, Cardarelli, Francois, 2nd Edition, Springer, 1999

Appendix F Fundamental Constants

Table F-1 Fundamental Constants

Quantity	Symbol	Value and units
Speed of light	c	$2.997\,924\,58 \times 10^{8}$ m/s
Permittivity in vacuum	ε_o (κ_o)	$8.854\,187\,816 \times 10^{-12}$ F/m
Charge on proton (or electron)	q (or e)	$1.602\,176\,462 \times 10^{-19}$ C
Plank constant	h	$6.626\,068\,76 \times 10^{-34}$ Js
Boltzmann constant	k	$1.380\,650\,3 \times 10^{-23}$ J/K